Electronics for Particle Physics

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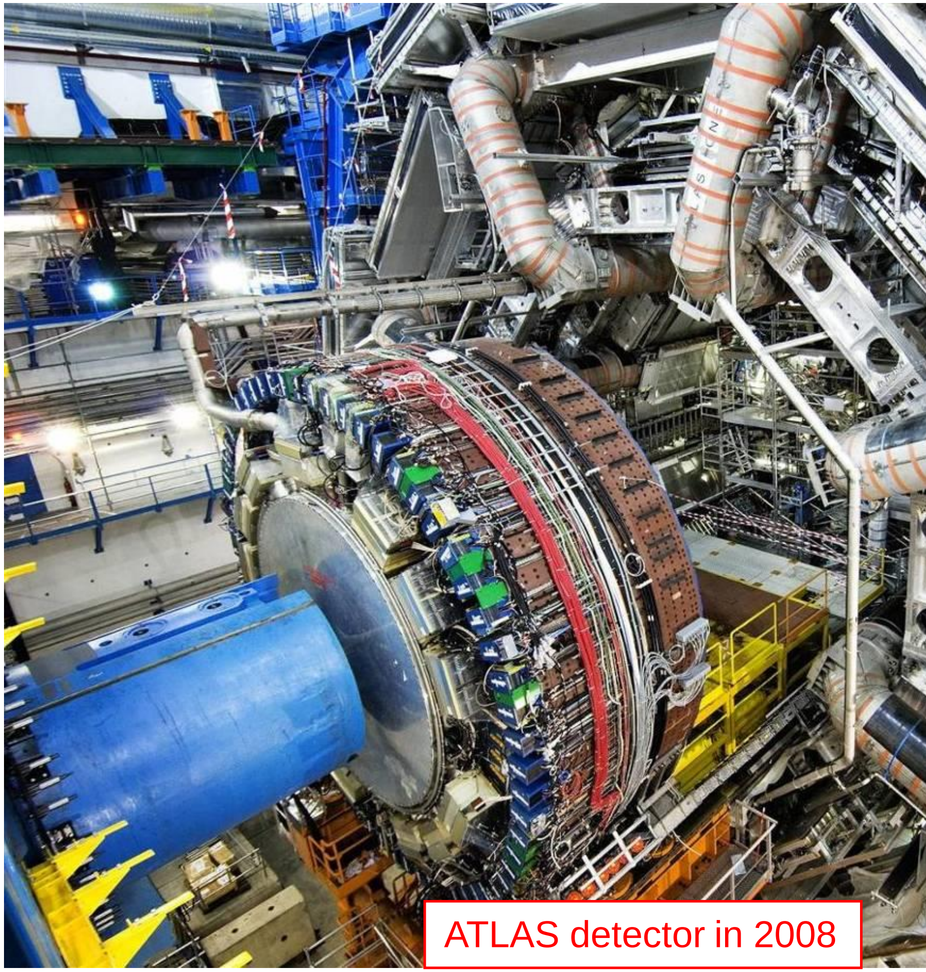
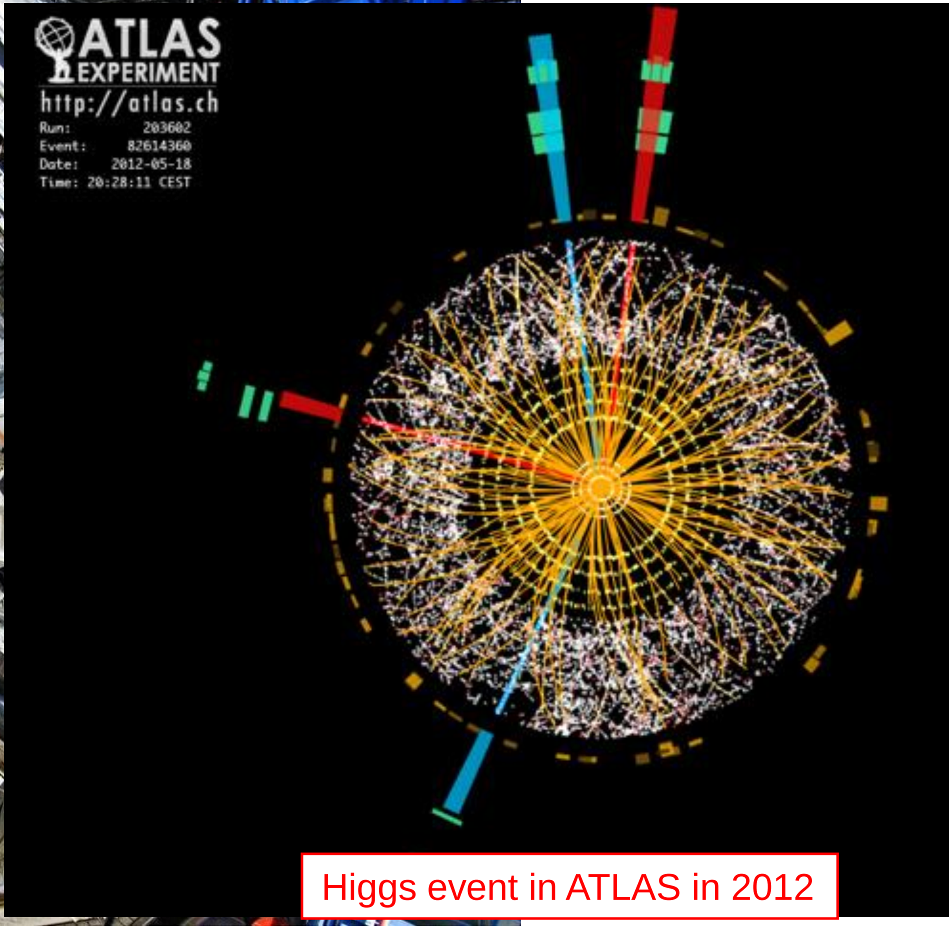
- A lot of electronics in the experiments…
  - The performance of electronics often impacts on the detectors
  - Analog electronics (V,A,A…) / Digital electronics (bits)



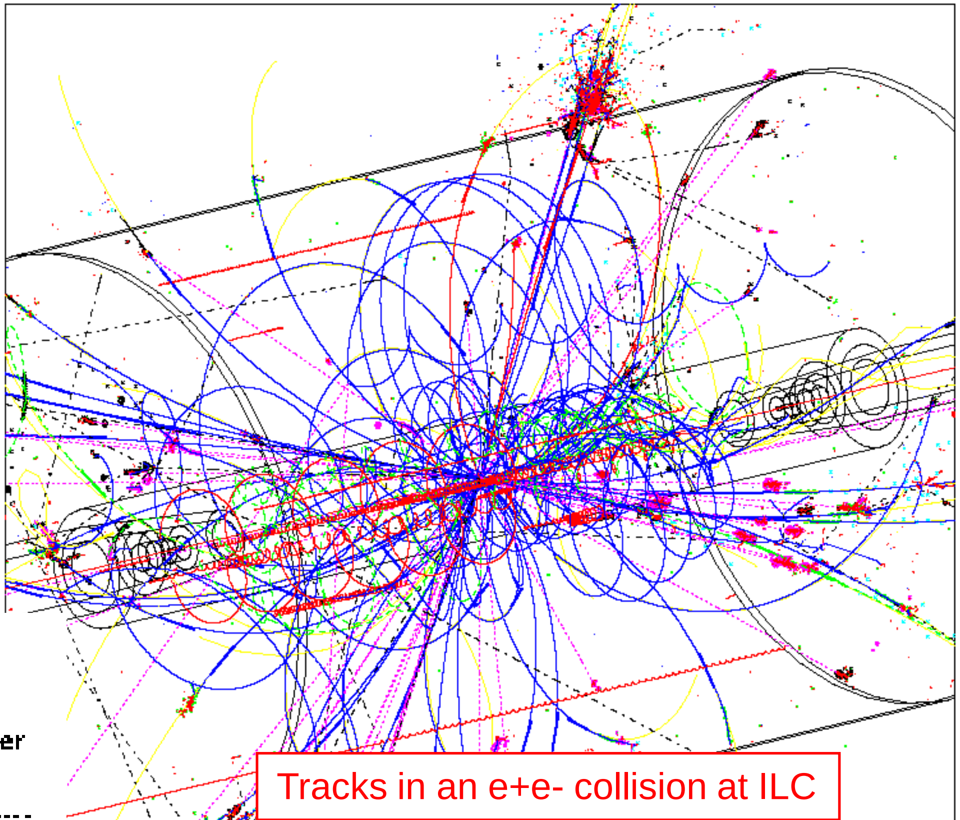
ATLAS detector in 2008



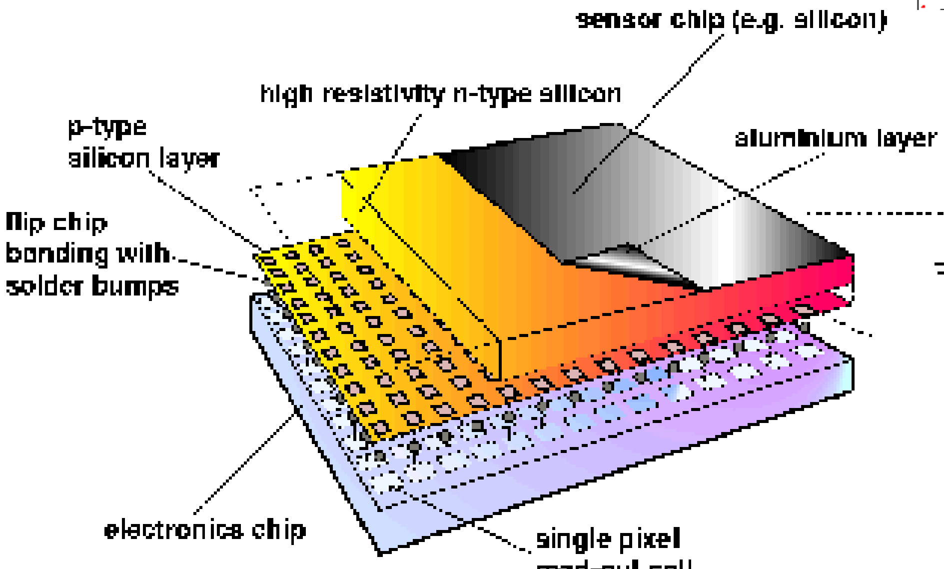
Higgs event in ATLAS in 2012

Electronics enabling new detectors : trackers

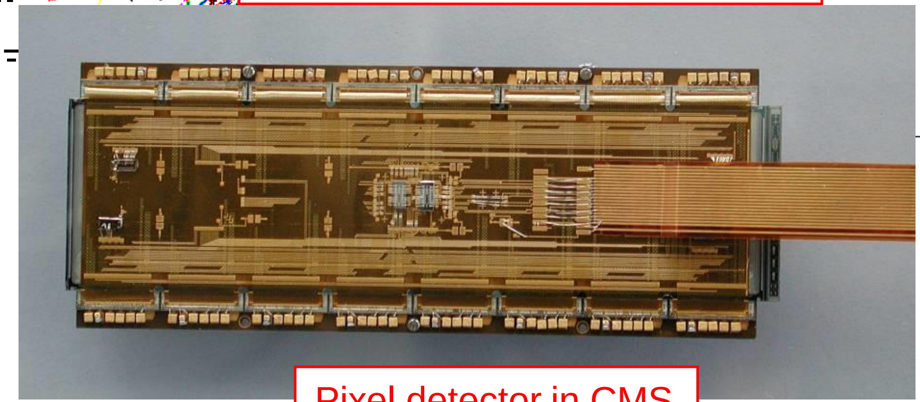
- Measurement of (charged) particle tracks
  - millions of pixels (~100 µm)
  - binary readout at 40 MHz
  - High radiation levels
  - Made possible by ASICs



Tracks in an e+e- collision at ILC



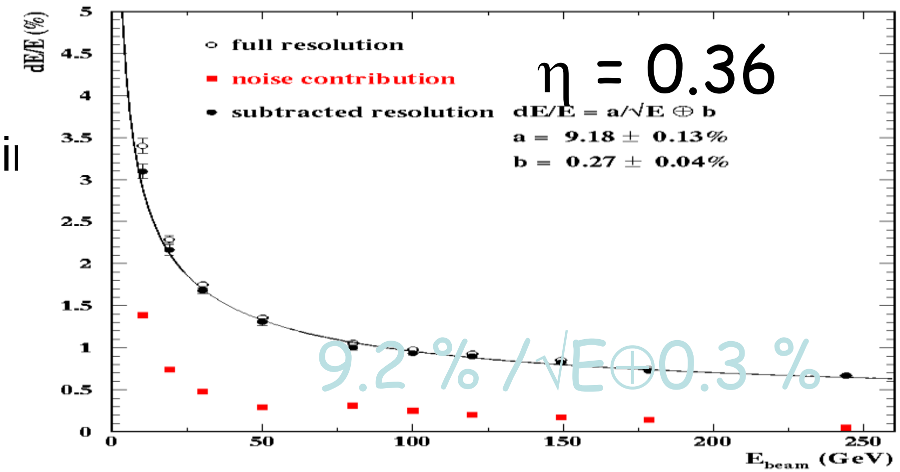
Pixel detector and readout electronics



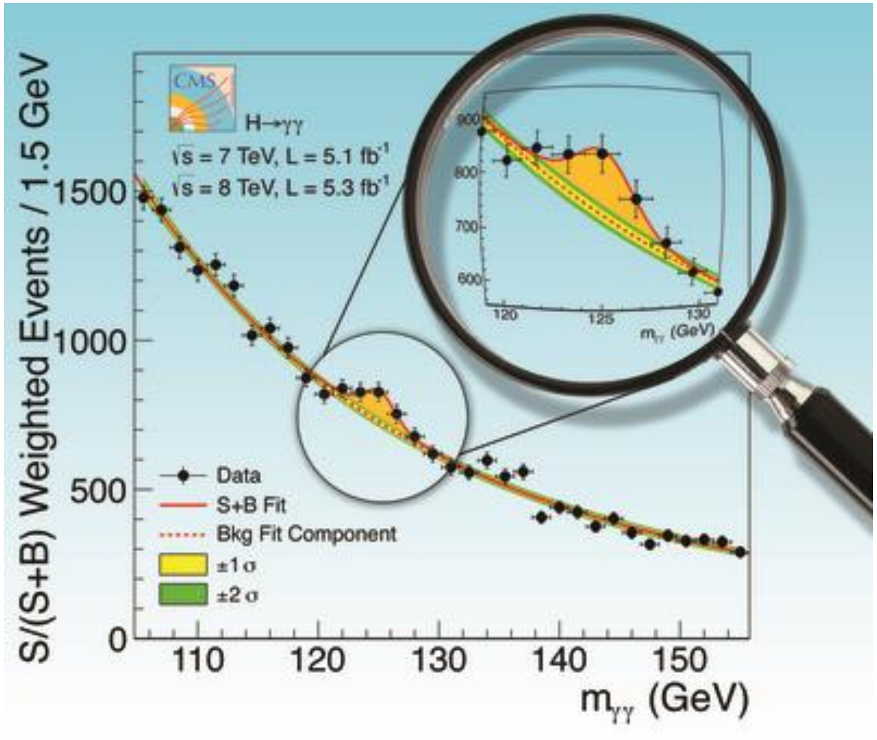
Pixel detector in CMS

Importance of electronics : calorimeters

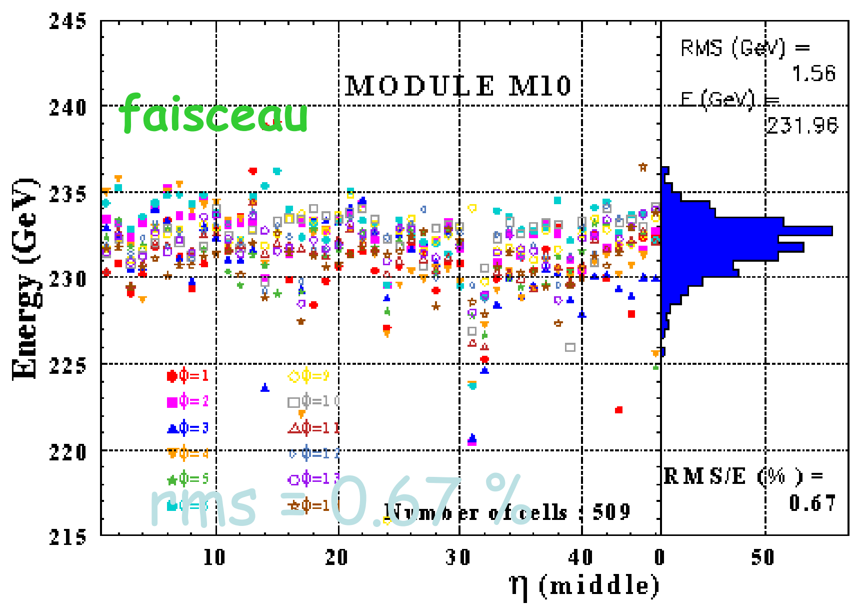
- Large dynamic range (10^4-10^5)
- High Precision ~1%
  - Importance of low noise, uniformity, li
  - Importance of calibration



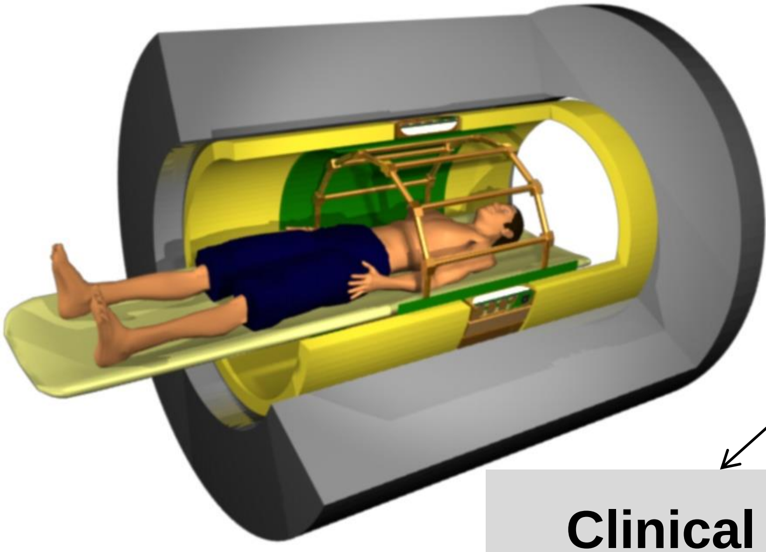
H -> γ γ in CMS calorimeter



Energy resolution and uniformity in ATLAS



Societal applications : PET



PET Ring / Scanner

Clinical PET
(Whole Body PET)

- For humans

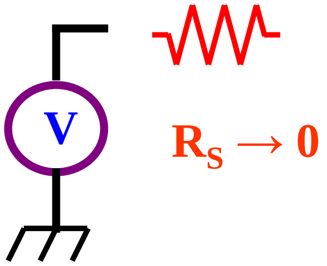
- large diameter FOV (>60 cm)
- spatial resolution: **few mm**
- time resolution CRT< **400 ps** for ToF
- high sensitivity (low dose) ➔ large area
- high total data rate

Preclinical PET
(Animal PET)

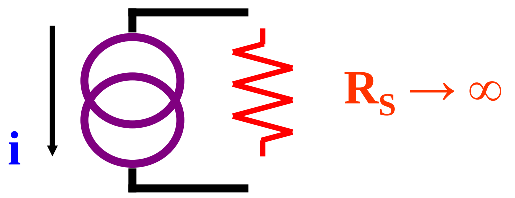
- For mice, rats, rabbits (& human brain)

- Small diameter FOV (4-15 cm)
- spatial resolution: **< 1 mm**
- time resolution only for coinc. (few ns)
- medium sensitivity
- Depth - of - Interaction desirable to fight parallax effect

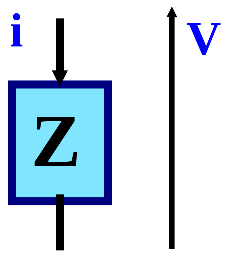
- **Voltage generators or source**
  - Ideal source : constant voltage, independent of current (or load)
  - In reality : non-zero source impedance R_S



- **Current generators**
  - Ideal source : constant current, independent of voltage (or load)
  - In reality : finite output source impedance R_S

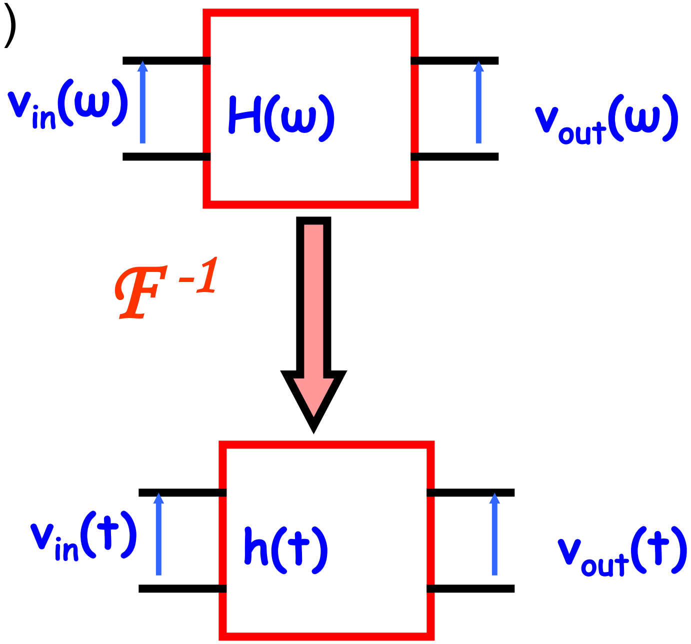


- **Ohms' law**
  - Z = R, 1/jωC, jωL
  - Note the sign convention



Frequency domain & time domain

- **Frequency domain** :
  - $V(\omega,t) = A \sin(\omega t + \varphi)$
    - Described by amplitude and phase (A, φ)
  - **Transfer function : $H(\omega)$** [or $H(s)$]
  - = The ratio of output signal to input signal in the frequency domain assuming linear electronics
  - $V_{out}(\omega) = H(\omega)\, V_{in}(\omega)$



- **Time domain**
  - Impulse response : $h(t)$
  - = the output signal for an impulse (delta) input in the time domain
  - The output signal for any input signal $v_{in}(t)$ is obtained by convolution : «*» :
  - $V_{out}(t) = v_{in}(t) * h(t) = \int v_{in}(u) * h(t-u)\, du$

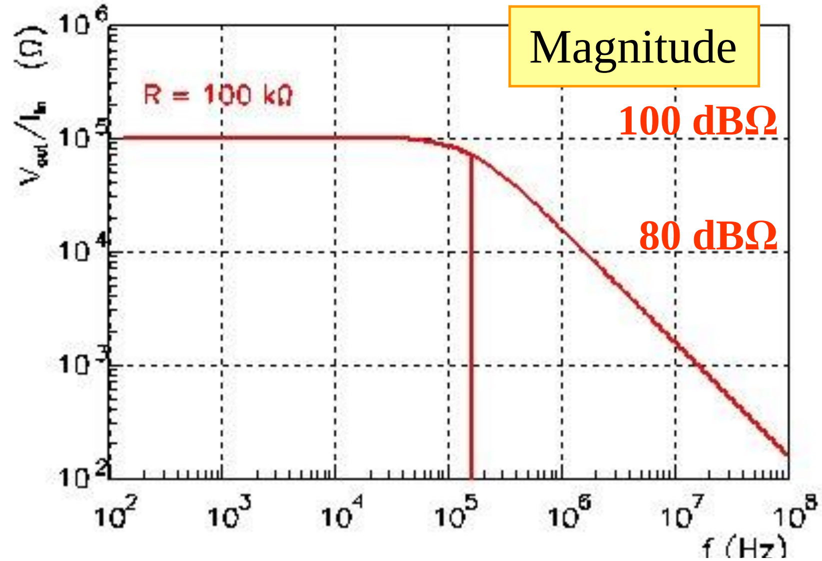
- Correspondance through Fourier transforms
  - $X(\omega) = \mathcal{F}\{x(t)\} = \int x(t) \exp(j\omega t)dt$
  - a few useful Fourier transforms in appendix

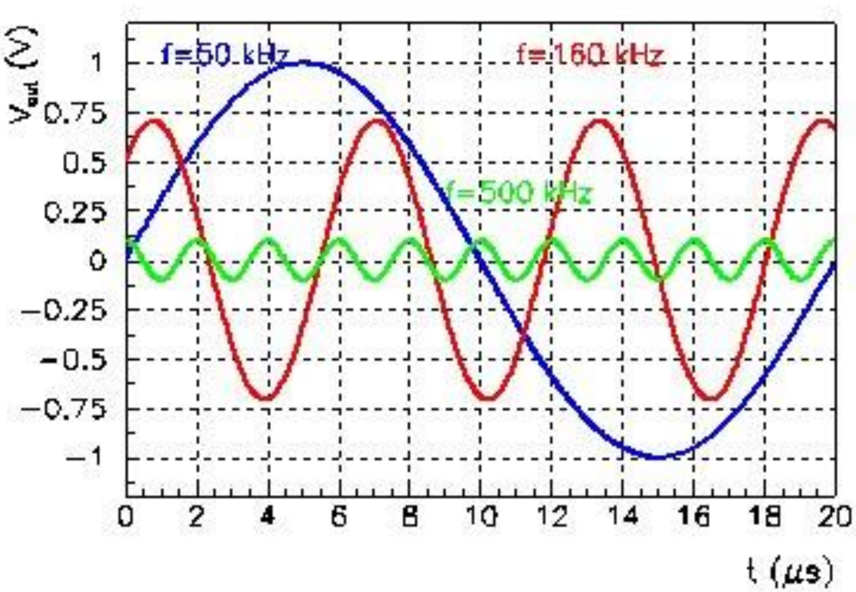
- $H(\omega) = 1$ -> $h(t) = \delta(t)$ (impulse)
- $H(\omega) = 1/j\omega$ -> $h(t) = S(t)$ (step)
- $H(\omega) = 1/j\omega\,(1+j\omega T)$ -> $h(t) = 1 - \exp(-t/T)$
- $H(\omega) = 1/(1+j\omega T)$ -> $h(t) = \exp(-t/T)$
- $H(\omega) = 1/(1+j\omega T)^n$ -> $h(t) = 1/n!\,(t/T)^{n-1} \exp(-t/T)$
- …

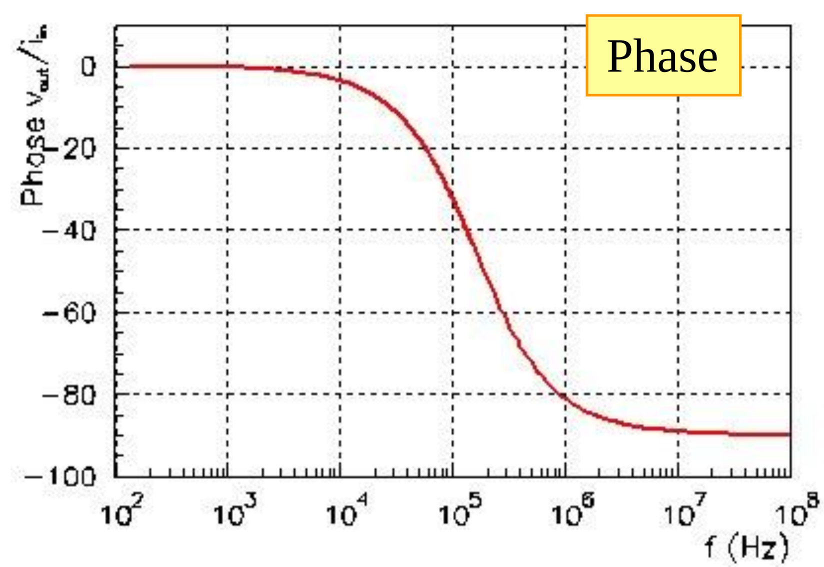
Frequency response

Ωmega

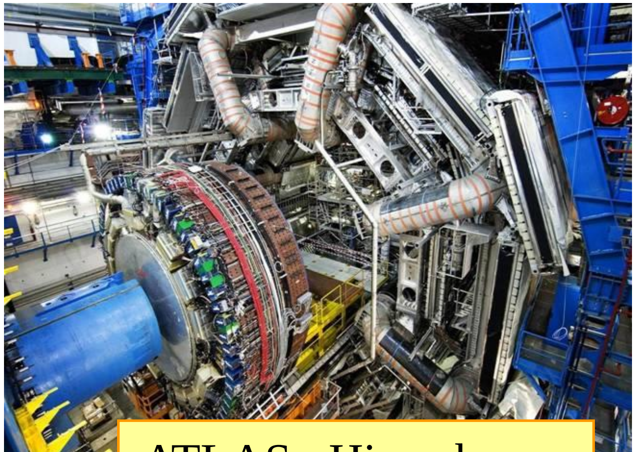
- **Bode plot**
  - Magnitude (dB) = 20 log |H(jw)|
  - -3dB bandwidth : $f_{-3dB} = 1/2\pi RC$
    - $R=10^5\Omega$, C=10pF => f_{-3dB}=160 kHz
    - At f_{-3dB} the signal is attenuated by 3dE $\sqrt{2}$, the phase is -45°
  - Above f_{-3dB} , gain rolls-off at 20dB/decade (or -6dB/octave)





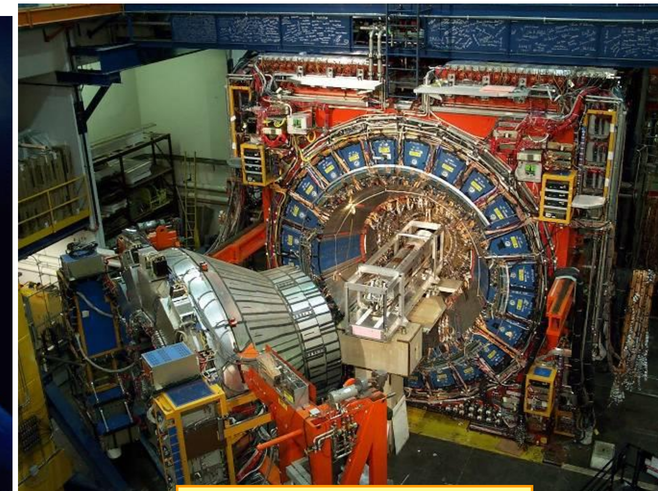


A large variety of detectors…

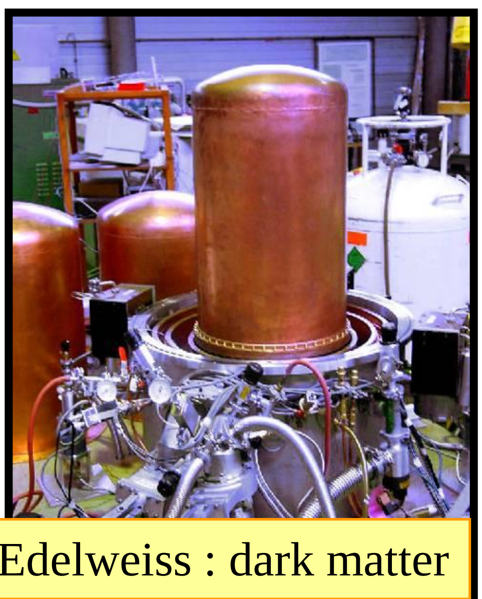


ATLAS : Higgs boson

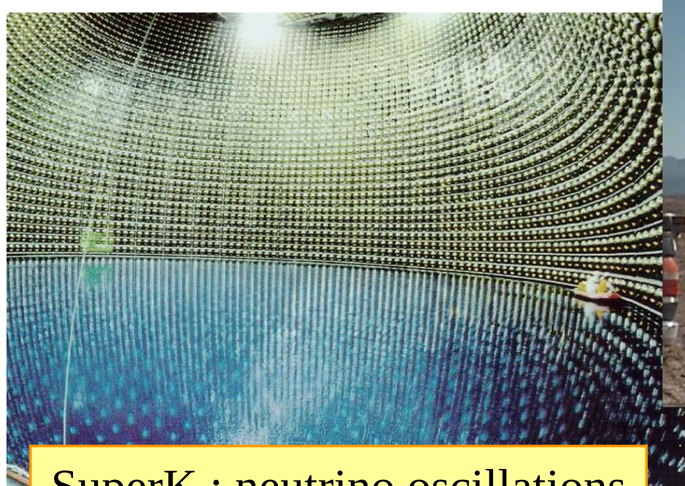
Planck : CMB



CDF : top quark



Edelweiss : dark matter

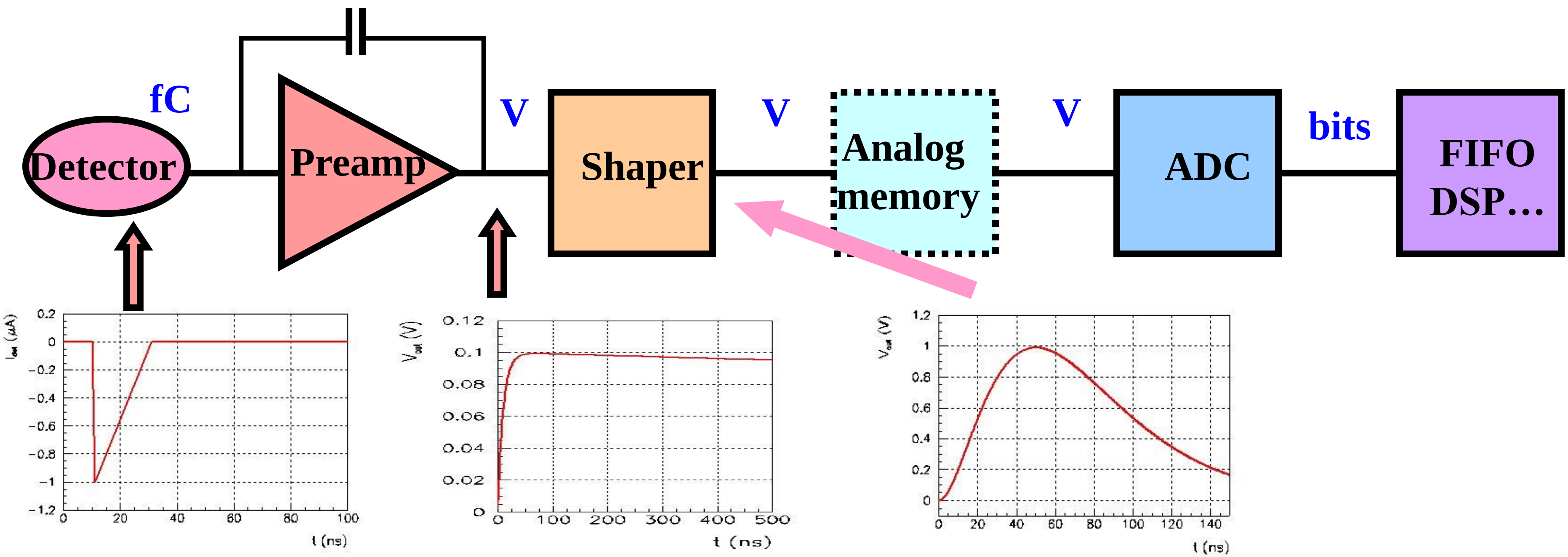


SuperK : neutrino oscillations

AUGER : cosmic rays 10^{20}eV

Overview of readout electronics

- Most front-ends follow a similar architecture



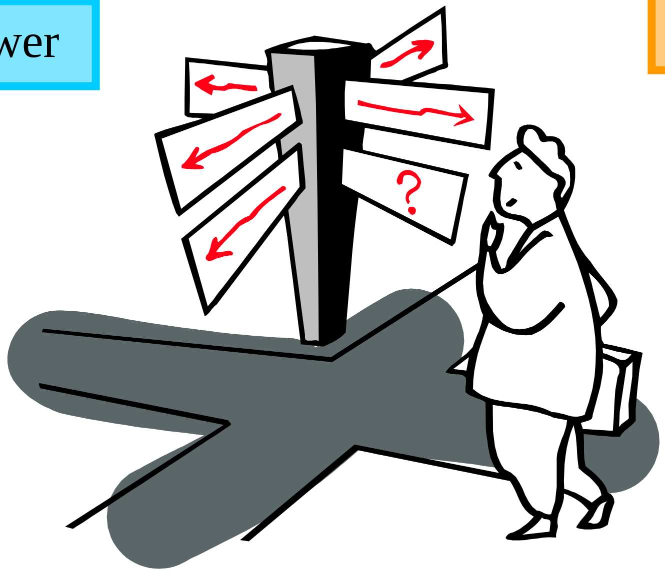
- **Very small signals (fC) -> need amplification**
- **Measurement of amplitude and/or time (ADCs, discris, TDCs)**
- **Several thousands to millions of channels**
- **Trends : high speed, low power**

Readout electronics : requirements

Low noise

Low power

High speed



High reliability

Large dynamic range

Radiation hardness

Low cost !

(and even less)

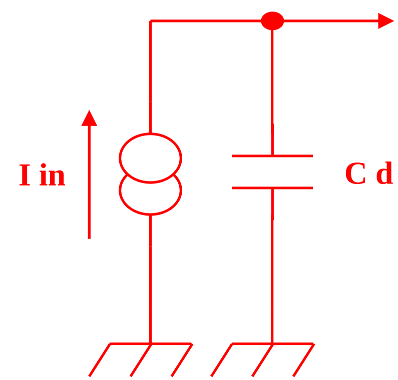
Low material

Detector modelization

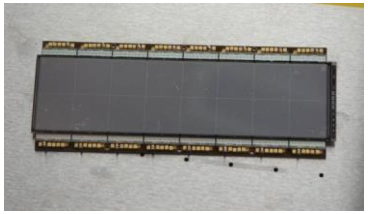
- Detector = capacitance Cd
  - Pixels/strips : 0.1-10 pF
  - PMs/SiPMs : 3-300 pF
  - Ionization chambers 10-1000 pF
  - Sometimes effect of transmission line

- Signal : current source
  - Pixels : ~100e-/µm
  - PMs : 1 photoelectron -> 10^5-10^7 e-
  - Modelized as an impulse (Dirac) : $i(t)=Q_0\delta(t)$

- Missing :
  - High Voltage bias
  - Connections, grounding
  - Neighbours
  - Calibration…



Detector modeilization



CMS pixel module

ATLAS LAr calorimeter

Signal & Source modelization (cf lecture 3)

Vacuum Photomultipliers

G = $10^5 – 10^7$

Cd ~ 10 pF

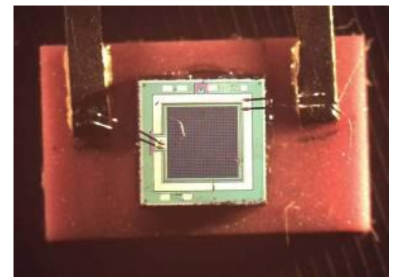
L ~ 10 nH

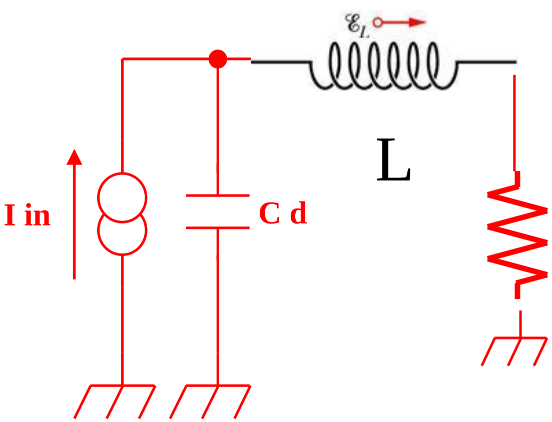
Silicon Photomultipliers

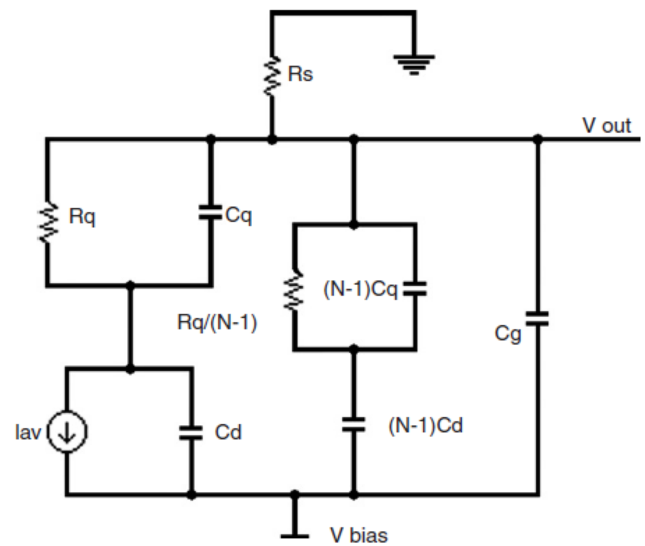
G = $10^5 – 10^7$

C = 10 - 400 pF

L = 1 – 10 nH







Optimizing signal shape for timing

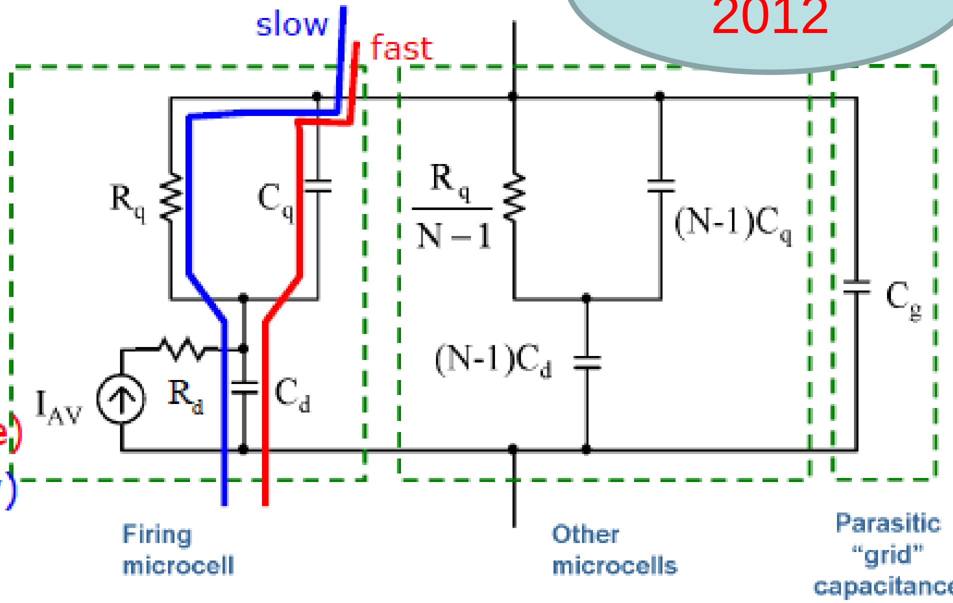
Collazuol 2012

Single cell model → $(R_d||C_d)+(R_q||C_q)$

SiPM + load → $(||Z_{cell})||C_{grid} + Z_{load}$

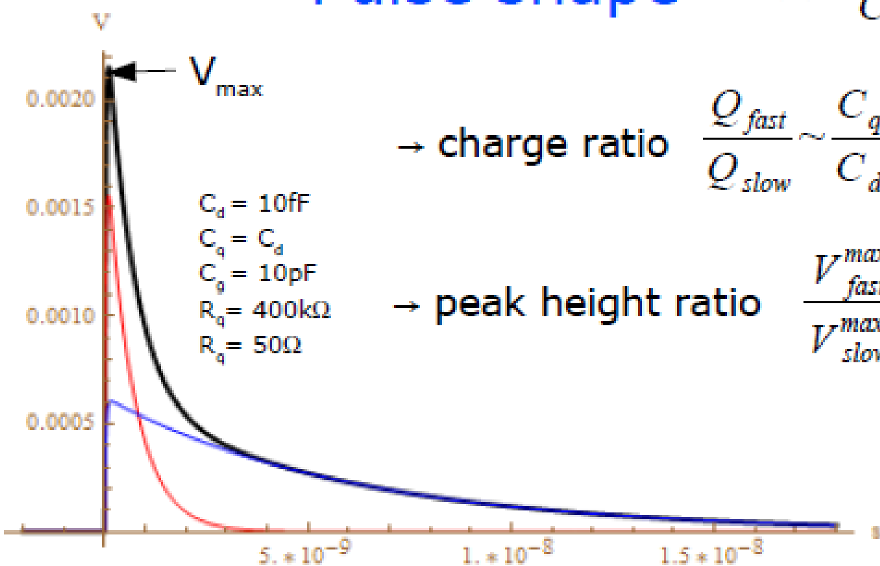
Signal = slow pulse ($\tau_{d\,(rise)}$, $\tau_{q\text{-slow (fall)}}$) +
+ fast pulse ($\tau_{d\,(rise)}$, $\tau_{q\text{-fast (fall)}}$)

- $\tau_{d\,(rise)} \sim R_d(C_q+C_d)$
- $\tau_{q\text{-fast (fall)}} = R_{load}\ C_{tot}$ (fast; parasitic spike)
- $\tau_{q\text{-slow (fall)}} = R_q\,(C_q+C_d)$ (slow; cell recovery)



Pulse shape

$$V(t) \simeq \frac{Q}{C_q+C_d}\left(\frac{C_q}{C_{tot}} e^{\frac{-t}{\tau_{FAST}}} + \frac{R_{load}}{R_q}\frac{C_d}{C_q+C_d} e^{\frac{-t}{\tau_{SLOW}}}\right)$$



→ charge ratio $\dfrac{Q_{fast}}{Q_{slow}} \sim \dfrac{C_q}{C_d}$

→ peak height ratio $\dfrac{V^{max}_{fast}}{V^{max}_{slow}} \sim \dfrac{C_q^2 R_q}{C_d\, C_{tot}\, R_{load}}$

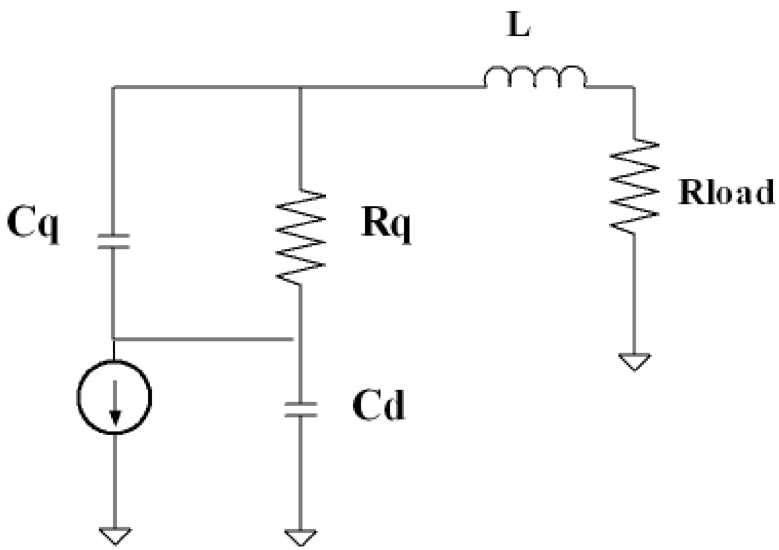
increasing with Rq and $1/R_{load}$ (and Cq of course)

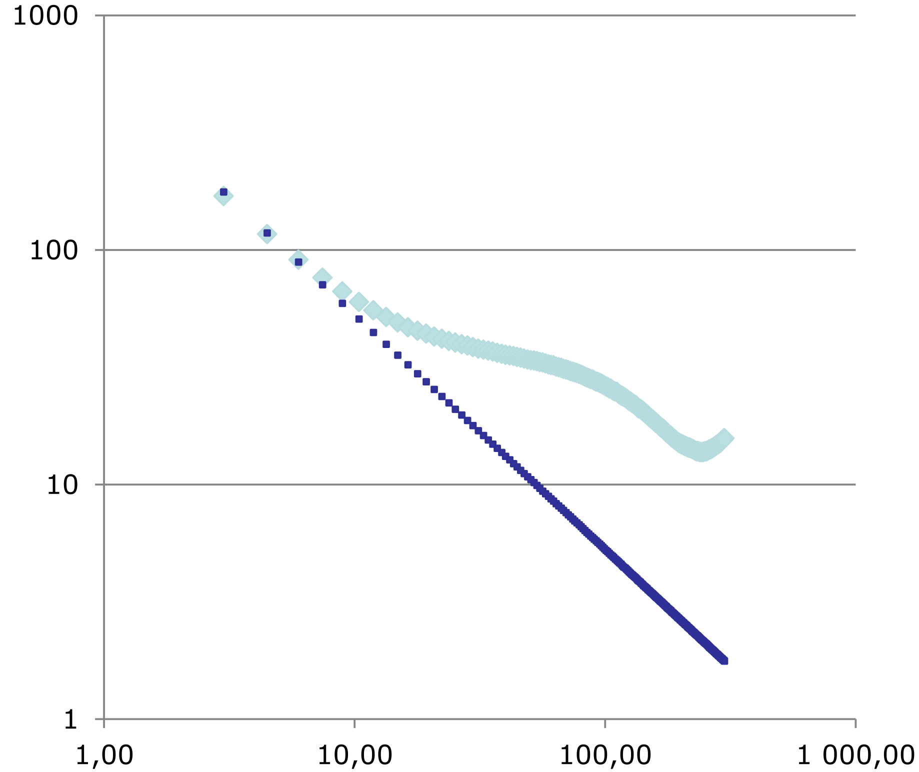
Increasing C_q/C_d or/and R_q/R_{load}
→ spike enhancement
→ better timing

G.Collazuol - PhotoDet 2012

SiPM impedance and model

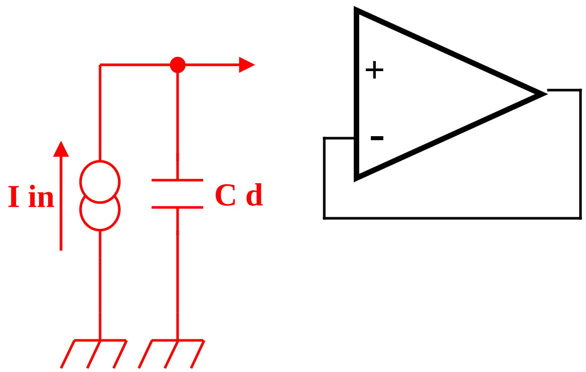
- RLC too simple, inaccurate at high frequency
- CdRqCqLR OK
  - May better explain HF noise behaviour





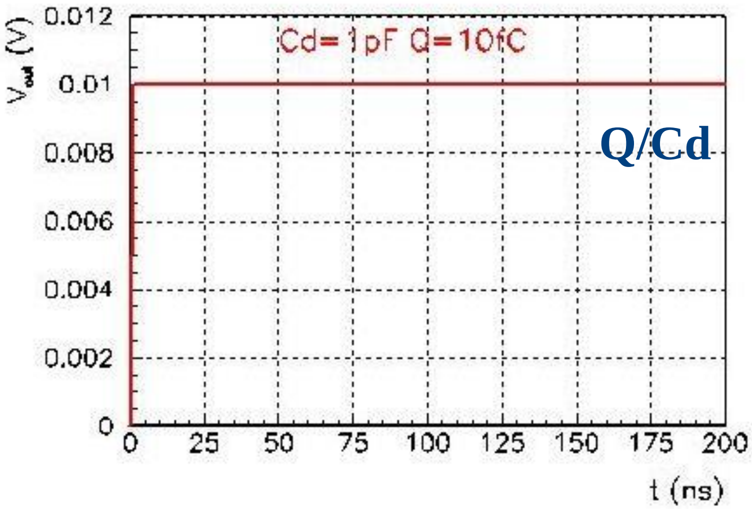
Measured impedance
MPPC HPK 3x3 mm
Line : C = 320 pF

- Signal
  - Signal = current source
  - Detector = capacitance C_d
  - Quantity to measure
    - Charge => integrator needed
    - Time => discriminator + TDC



Voltage readout

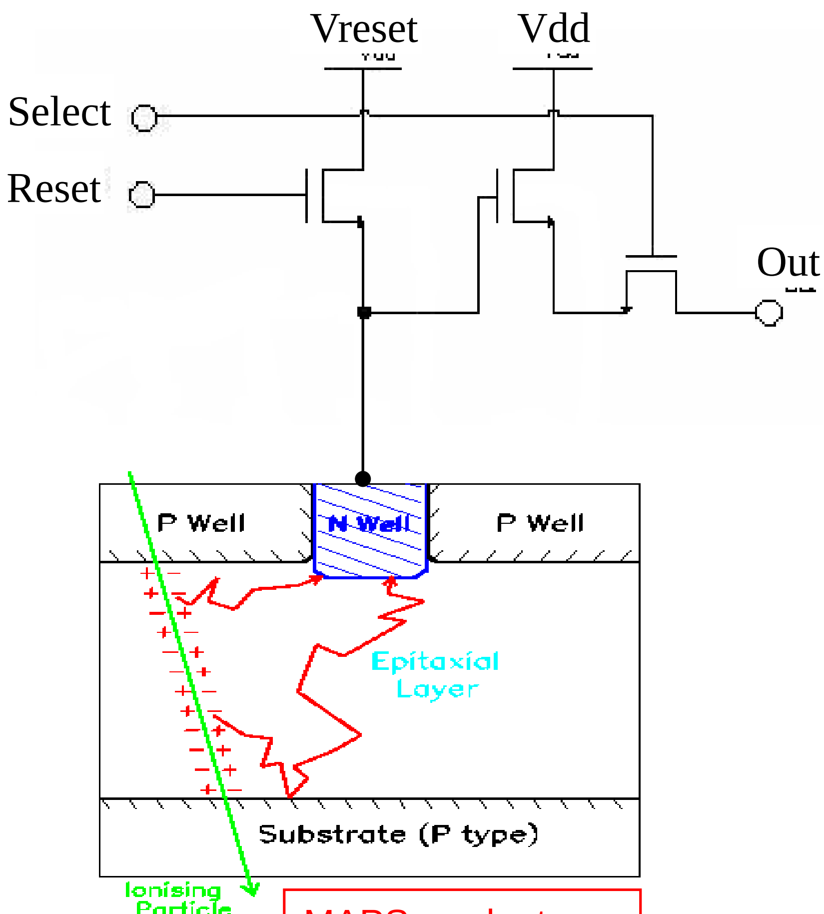
- Integrating on Cd
  - Simple : $V = Q/C_d$
  - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
  - Need a follower to buffer the voltage…
  - Gain loss, possible non-linearities
  - crosstalk
  - Need to empty Cd…



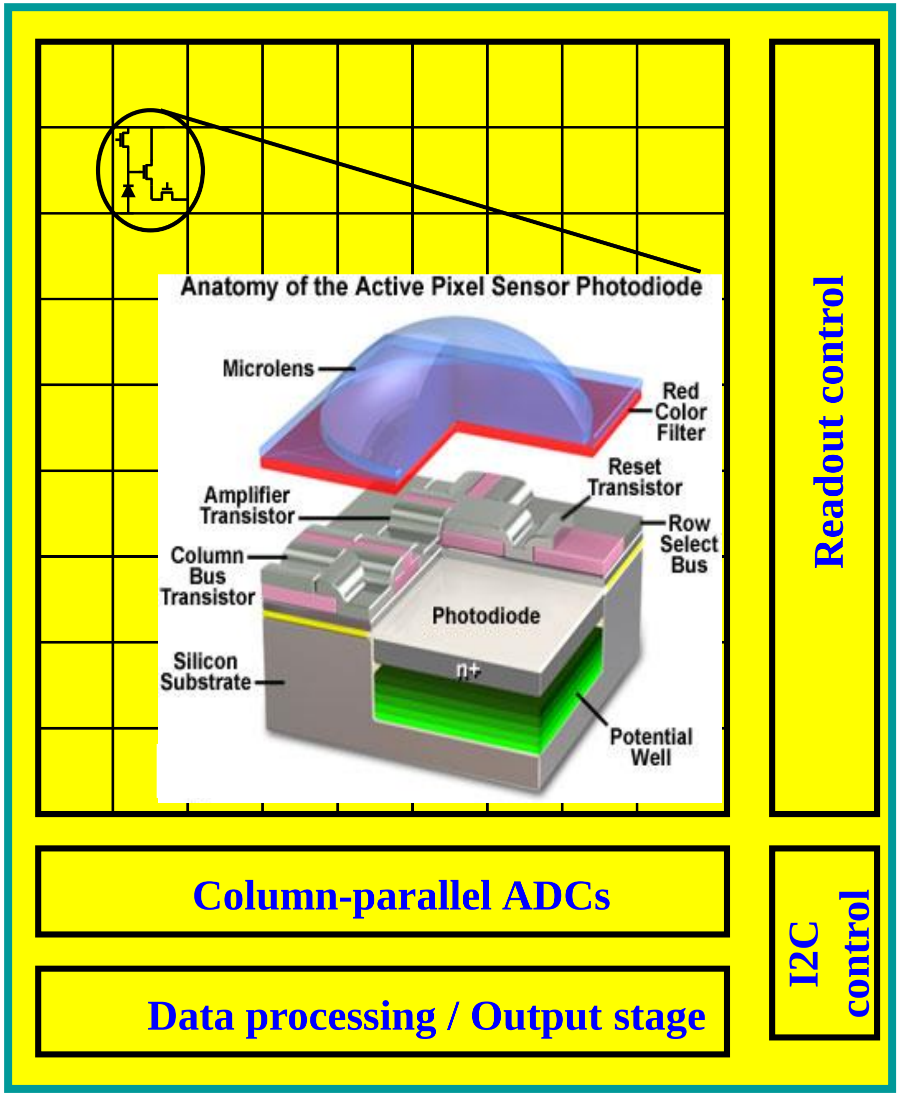
Impulse response

Example : Monolithic active pixels

- Epitaxial layer forms sensitive volume (2-20μm)
- Charge collection by diffusion
- Read ~100 e- on Cd~10fF = few mV



MAPS readout

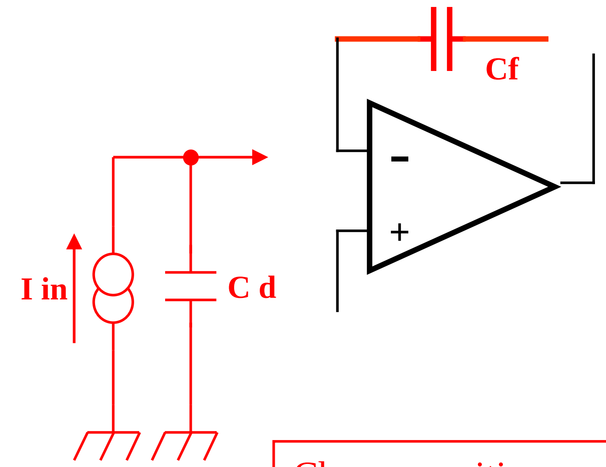


Ideal charge preamplifier

- ideal opamp in transimpedance
  - Shunt-shunt feedback
  - transimpedance : v_{out}/i_{in}
  - Vin-=0 => $V_{out}(\omega)/i_{in}(\omega) = - Z_f = - 1/j\omega C_f$
  - Integrator : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

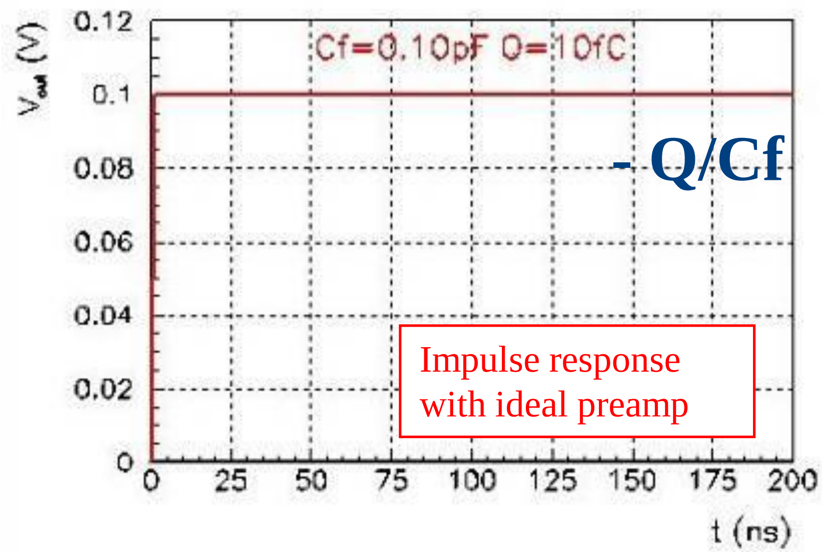
$$v_{out}(t) = - Q/C_f$$

  - « Gain » : $1/C_f$: 0.1 pF -> 10 mV/fC
  - C_f determined by maximum signal



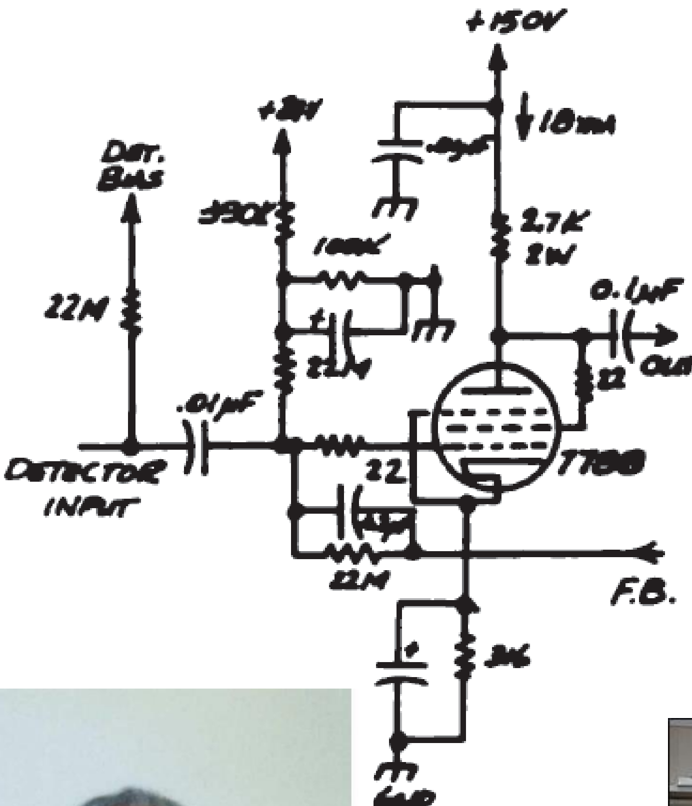
Charge sensitive preamp

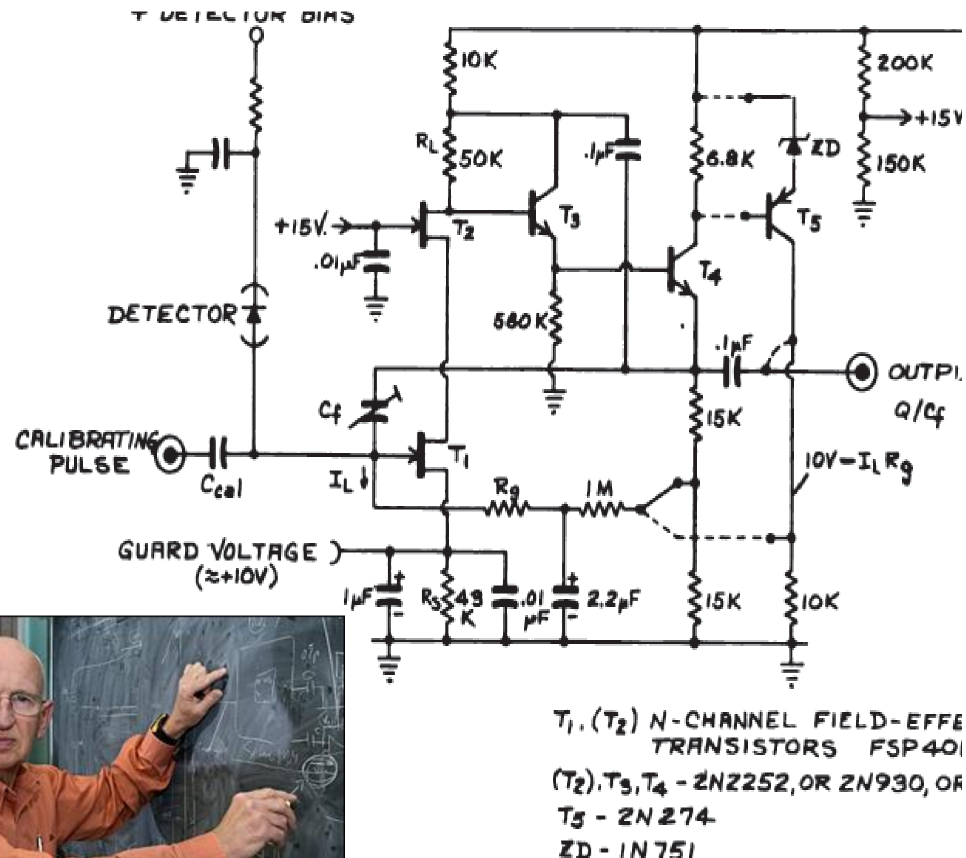
- Integration on Cf
  - Simple : $V = - Q/C_f$
  - Unsensitive to preamp capacitance C_{PA}
  - Turns a short signal into a long one
  - The front-end of 90% of particle physics
  - But always built with custom circuits…

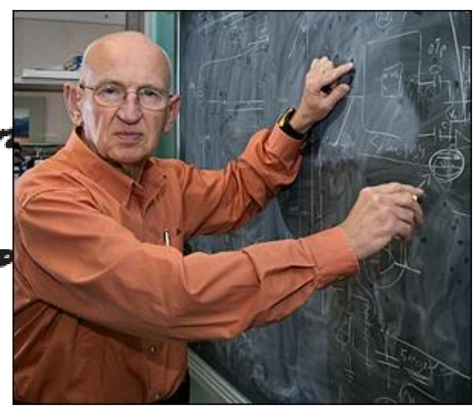


Impulse response with ideal preamp

New developments in charge preamps (1963)



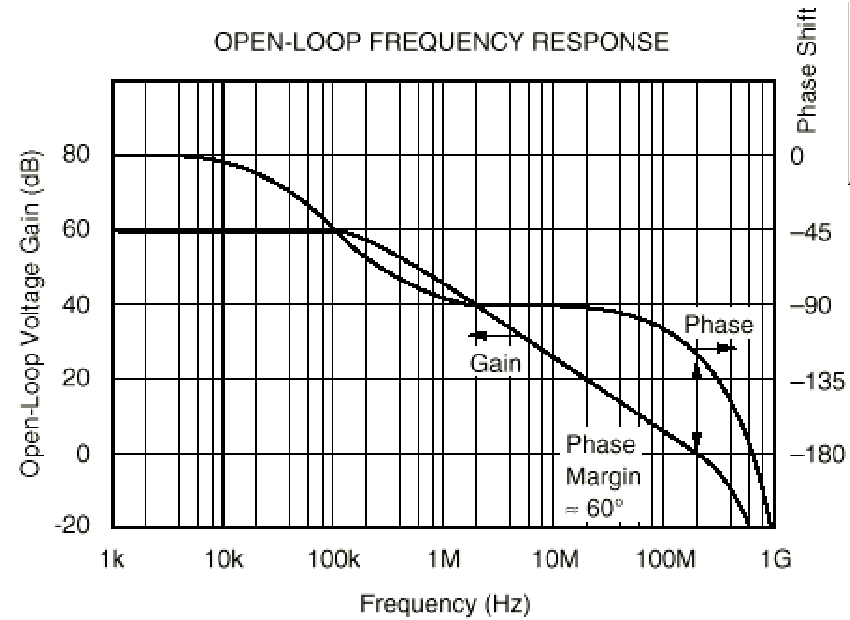


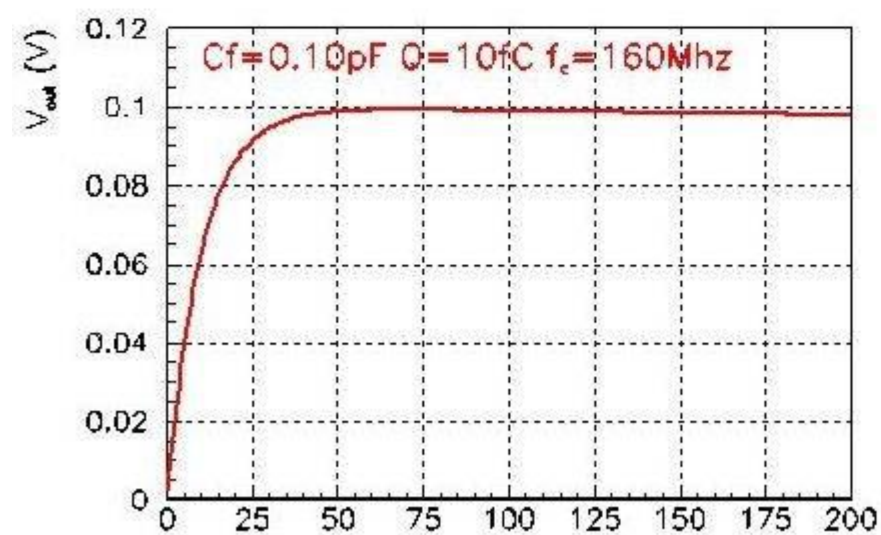


Radeka's preamp (Monterrey 63)

Preamp speed

- Finite opamp gain
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + C_d / G_0 C_f)$
  - Small signal loss in $C_d/G_0C_f \ll 1$ (ballistic deficit)
- Finite opamp bandwidth
  - First order open-loop gain
  - $G(\omega) = G_0/(1 + j\,\omega/\omega_0)$
    - G_0 : low frequency gain
    - $G_0\omega_0$: gain bandwidth product
- Preamp risetime
  - Due to gain variation with ω
  - Time constant : τ *(tau)*
  - $\tau = C_d/G_0\omega_0C_f$
  - Rise-time : $t_{10\text{-}90\%} = 2.2\,\tau$
  - Rise-time optimised with w_C or C_f



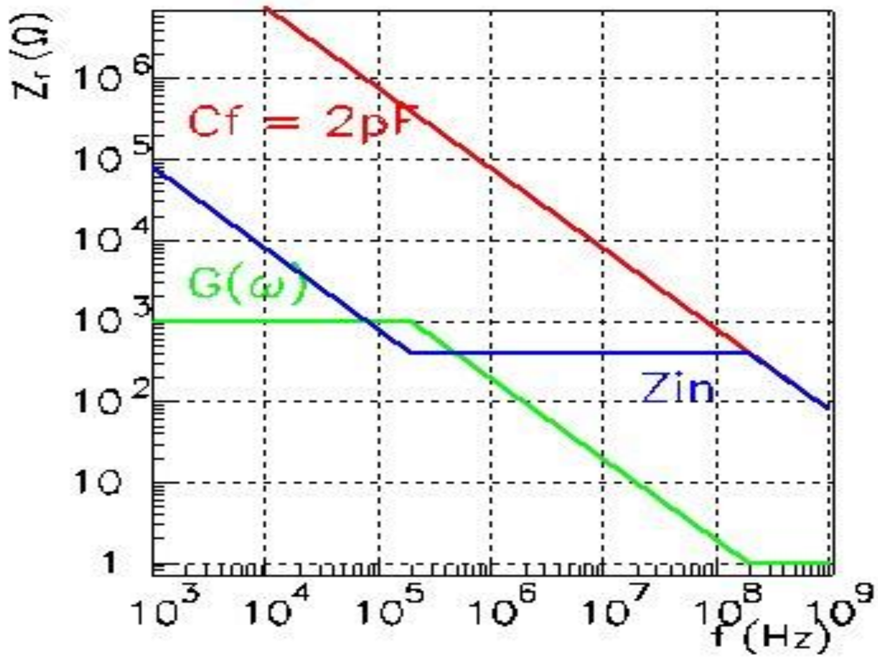


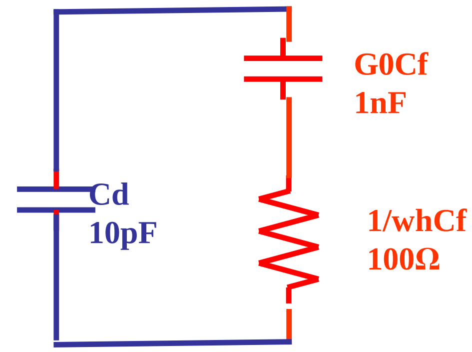
Impulse response with non-ideal preamp

Charge preamp seen from the input

- Input impedance with ideal opamp
  - Zin = Zf / G+1
  - Zin->0 for ideal opmap
  - « Virtual ground » : Vin = 0
  - Minimizes sensitivity to detector impedance
  - Minimizes crostalk
- Input impedance with real opamp
  - $Zin = 1/j\omega G_0 C_f + 1/ G_0 \omega_0 C_f$
  - Resistive term : $Rin = 1/ G_0 \omega_0 C_f$
    - Exemple : $w_C = 10^{10}$ rad/s C_f= 1 pF => Rin = 100 Ω
  - Determines the input time constant : $t = R_{eq} C_d$
  - Good stability= (…!)
  - Equivalent circuit :

Input impedance or charge preamp





Electronically cooled resistors [TNS 73]

SIGNAL, NOISE AND RESOLUTION IN POSITION-SENSITIVE DETECTORS*

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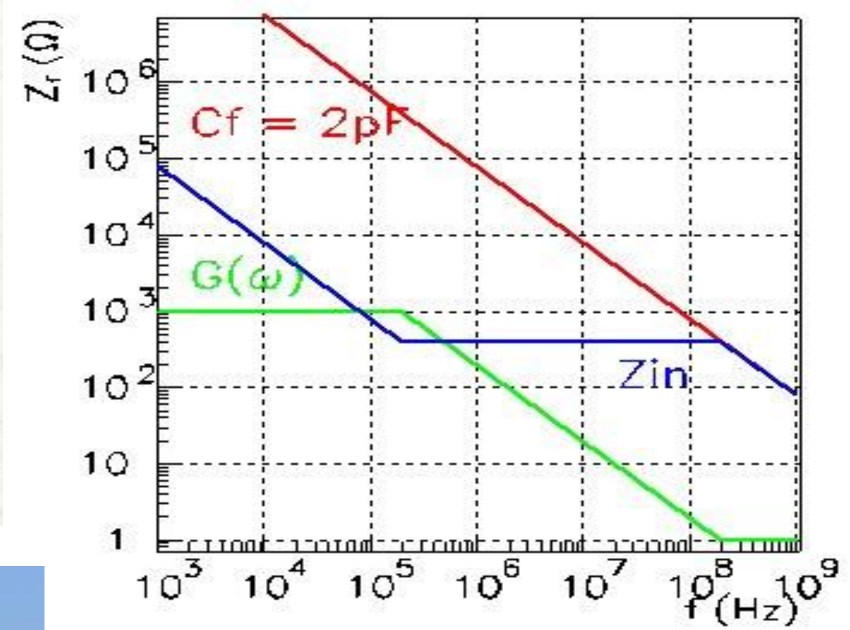
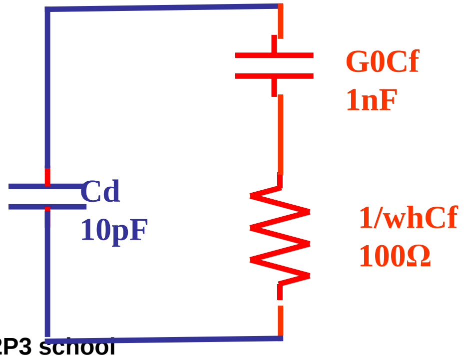
ABSTRACT

An analysis is presented of signal, noise and position resolution relations for some of the most interesting position-sensing methods. "Electronic cooling" of delay line terminations is introduced in order to reduce noise in the position-sensing with delay lines. A new method for terminating transmission lines and for "noiseless" damping which employs a capacitance in feedback is presented. It is shown that the position resolution for the charge division method with resistive electrodes is determined only by the electrode capacitance and not by the electrode resistance, if optimum filtering is used.

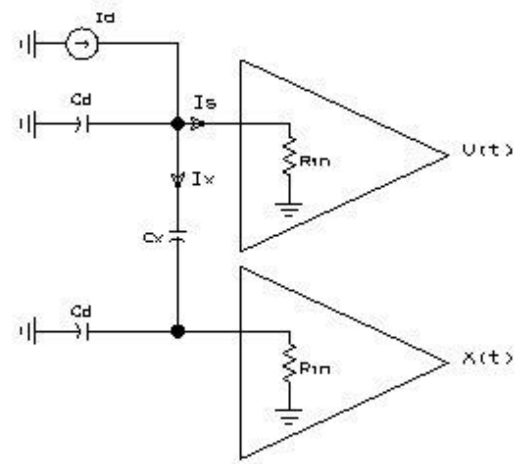


$$Z_{in} = 1/j\omega\, G_0 C_F + 1/\, G_0 \omega_0\, C_F$$

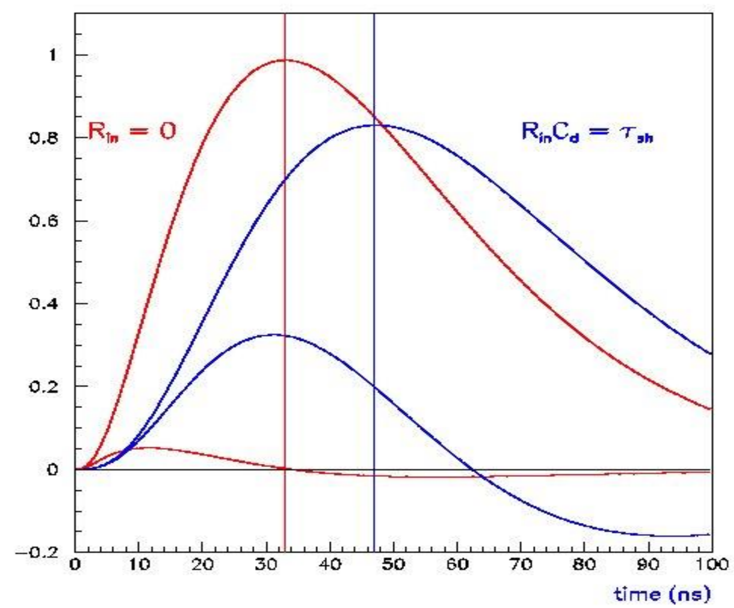


Crosstalk

- Capacitive coupling between neighbours
  - Crosstalk signal is differentiated and with same polarity
  - Small contribution at signal peak
  - Proportionnal to Cx/Cd and preamp input impedance
  - Slowed derivative if RinCd ~ tp => non-zero at peak
- Long distance crosstalk
  - Inductive/resistive common ground return
  - References impedance
  - Connectors : mutual inductance

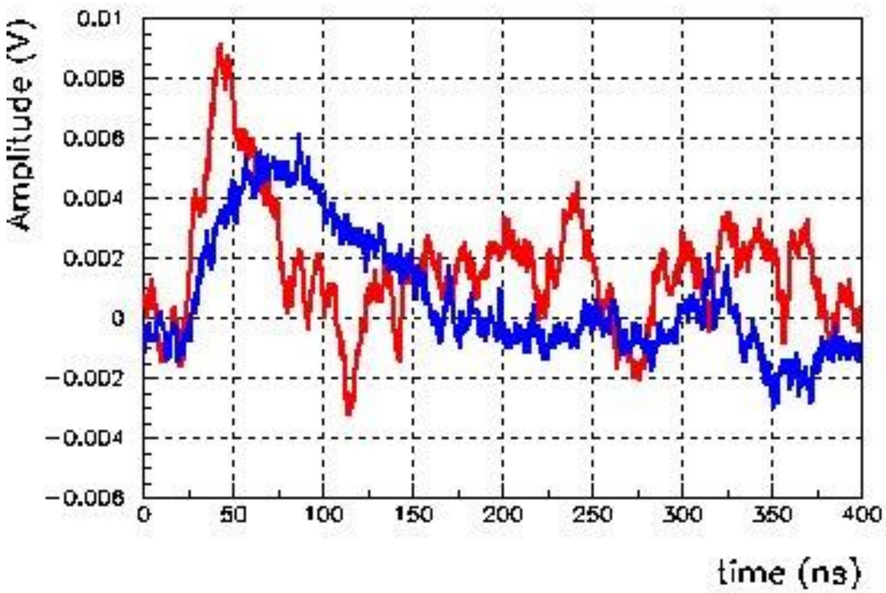


Crosstalk electrical modelization



- Definition of Noise
  - Random fluctuation superposed to interesting signal
  - Statistical treatment

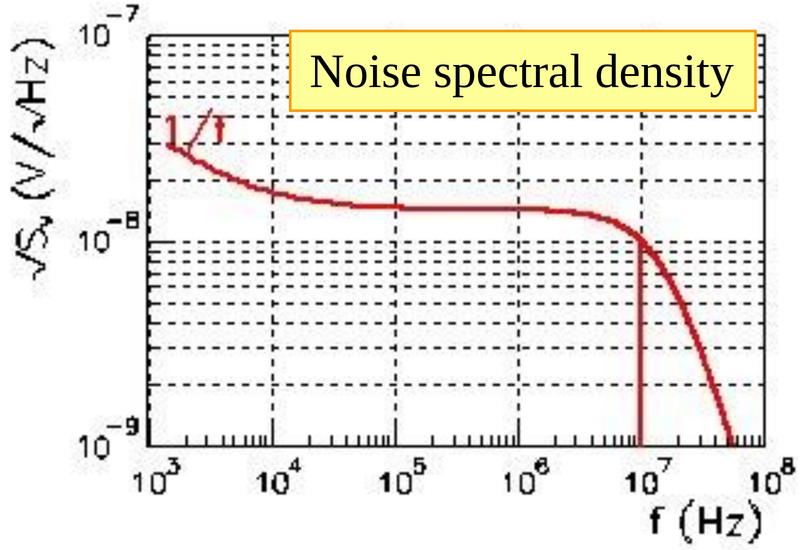
- Three types of noise
  - Fundamental noise (Thermal noise, shot noise)
  - Excess noise (1/f …)
  - Parasitics -> EMC/EMI (pickup noise, ground loops…)

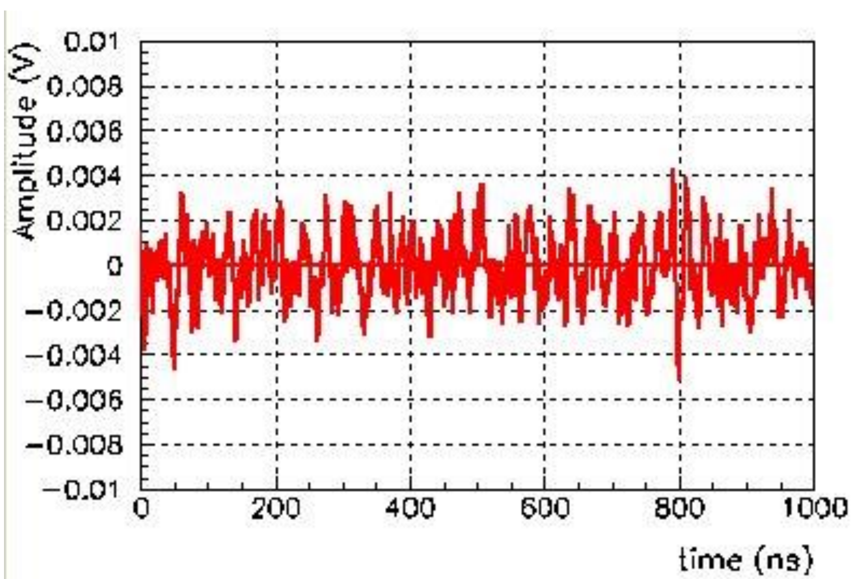


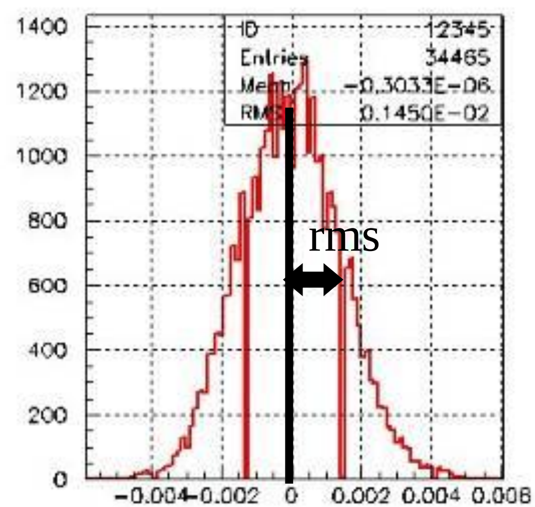
Omega

- Modelization
  - Noise generators : e_n, i_n,
  - Noise spectral density of e_n & i_n : $S_v(f$
  - $Sv(f) = | \mathcal{F}(e_n) |^2$ (V^2/Hz)

- *Rms* noise Vn
  - $V_n^2 = \int e_n^2(t)\,dt = \int Sv(f)\,df$
  - White noise (e_n) : $v_n = e_n \sqrt{\tfrac{1}{2}\pi f_{-3dB}}$



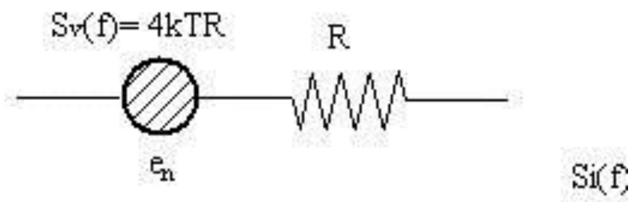




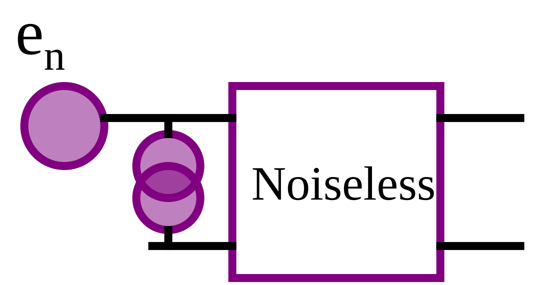
Rms noise vn

Calculating electronics noise

- Fundamental noise
  - Thermal noise (resistors) : Sv(f) = 4kTR
  - Shot noise (junctions) : Si(f) = 2qI



- Noise referred to the input
  - All noise generators can be referred to the input as 2 noise generators :
  - A voltage one e_n in series : series noise
  - A current one i_n in parallel : parallel noise
  - Two generators : no more, no less…



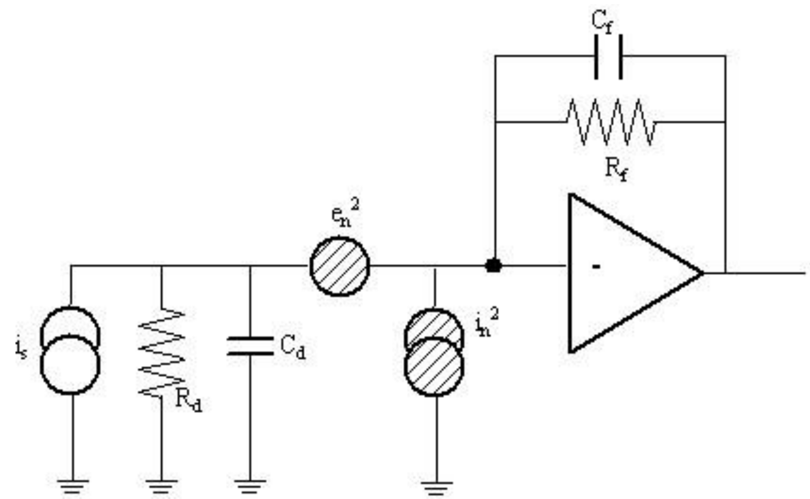
- **To take into account the Source impedance**

Noise generators referred to the input

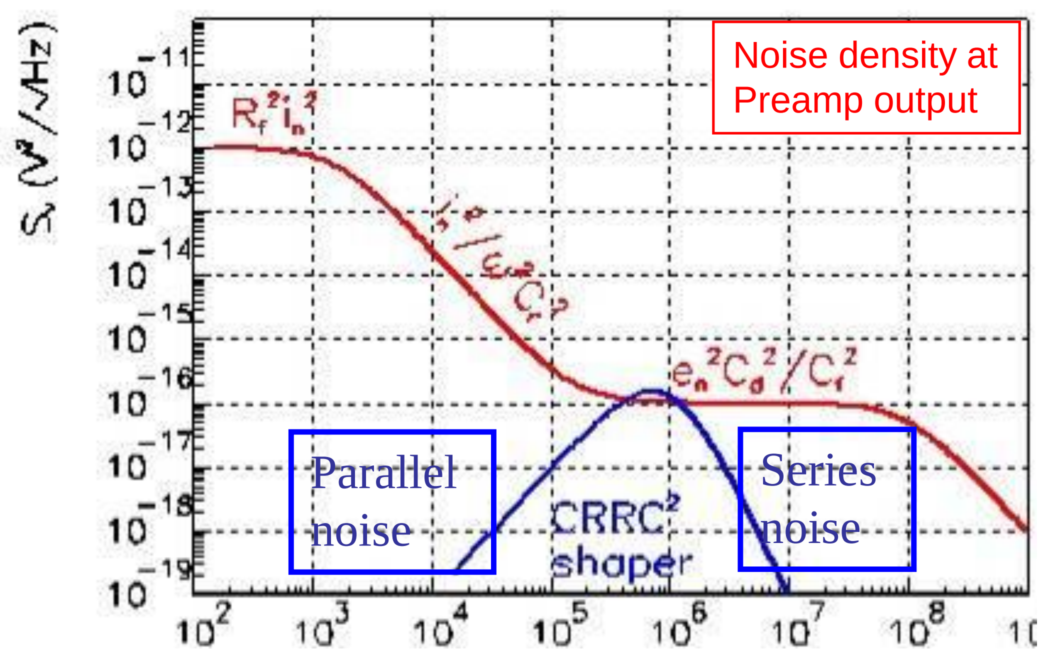
- **Golden rule :**
  - **Always calculate the signal before the noise what counts is the signal to noise ratio**

Noise in transimpedance amplifiers

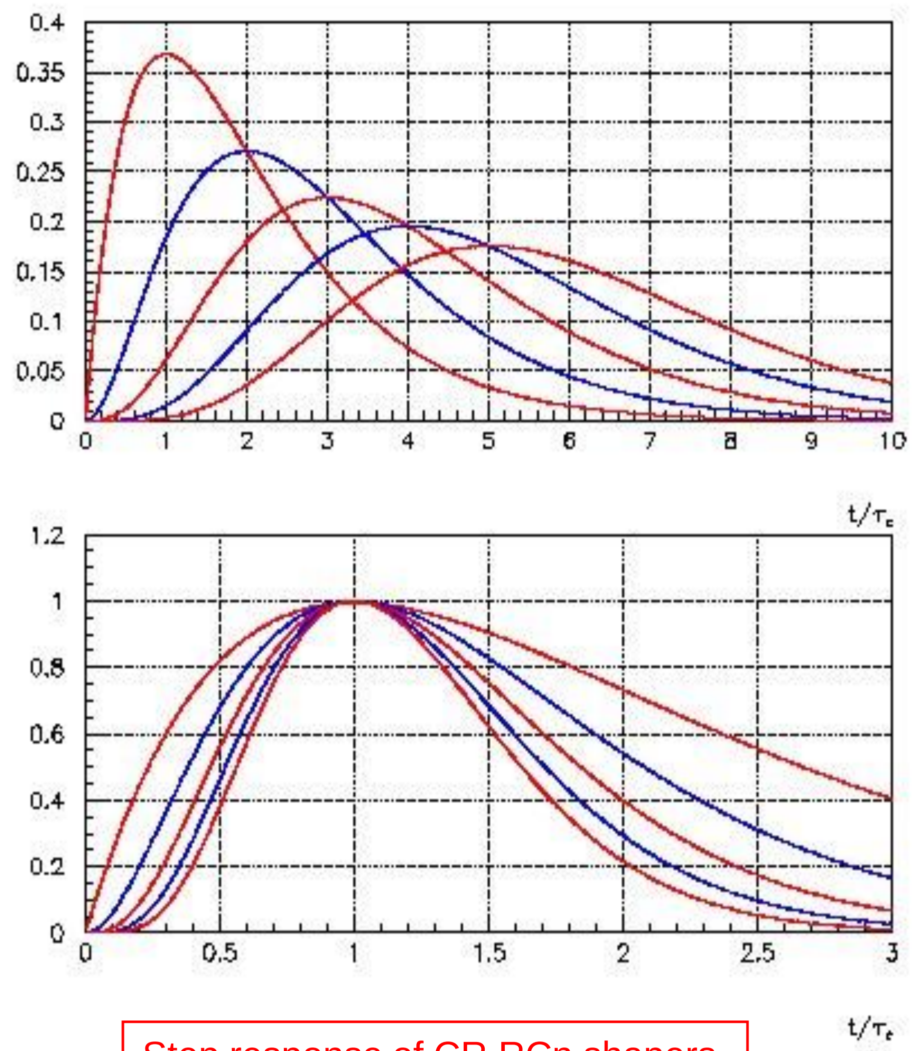
- 2 noise generators at the input
  - Parallel noise : (i_n^2) (leakage)
  - Series nosie : (e_n^2) (preamp)
- Output noise spectral density :
  - $Sv(\omega) = (i_n^2 + e_n^2/|Z_d|^2) * |Z_f|^2$
- For charge preamps
  - $Sv(\omega) = i_n^2 /\omega^2 C_f^2 + e_n^2 C_d^2/C_f^2$
  - Parallel noise in $1/\omega^2$
  - Series noise is flat, with a « noise gain » of C_d/C_f
- *rms* noise V_n
  - $V_n^2 = \int Sv(\omega) d\omega/2\pi \to \infty$
  - Benefit of shaping…



Noise generators in charge preamp



- Noise reduction by optimising useful bandwidth
  - Low-pass filters (**RC^n**) to cut-off high frequency noise
  - High-pass filter (**CR**) to cut-off parallel noise
  - -> pass-band filter CRRC^n
- Equivalent Noise Charge : ENC
  - Noise referred to the input in electrons
  - $ENC = Ia(n)\ e_n C_t/\sqrt{\tau} \oplus Ib(n)\ i_n^*\ \sqrt{\tau}$
  - Series noise in $1/\sqrt{\tau}$
  - Paralle noise in $\sqrt{\tau}$
  - 1/f noise independant of τ
  - Optimum shaping time $\tau_{opt} = \tau_c/\sqrt{2n-1}$

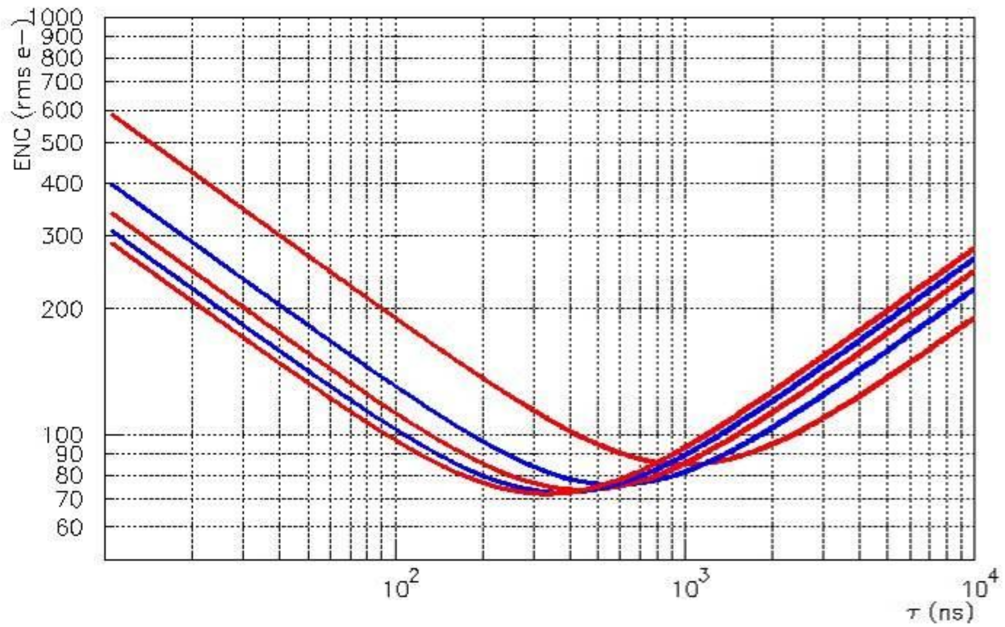


Step response of CR RCn shapers

Equivalent Noise Charge (ENC) after CRRC^n

- Peaking time tp (5-100%)
  - ENC(**tp**) independent of n
  - Also includes preamp risetime

- Complex shapers are obsolete :
  - Power of digital filtering
  - Analog filter = CRRC ou CRRC^2
  - antialiasing



ENC vs tau for CR RCn shapers

- A useful formula : **ENC (e- rms) after a CRRC² shaper :**

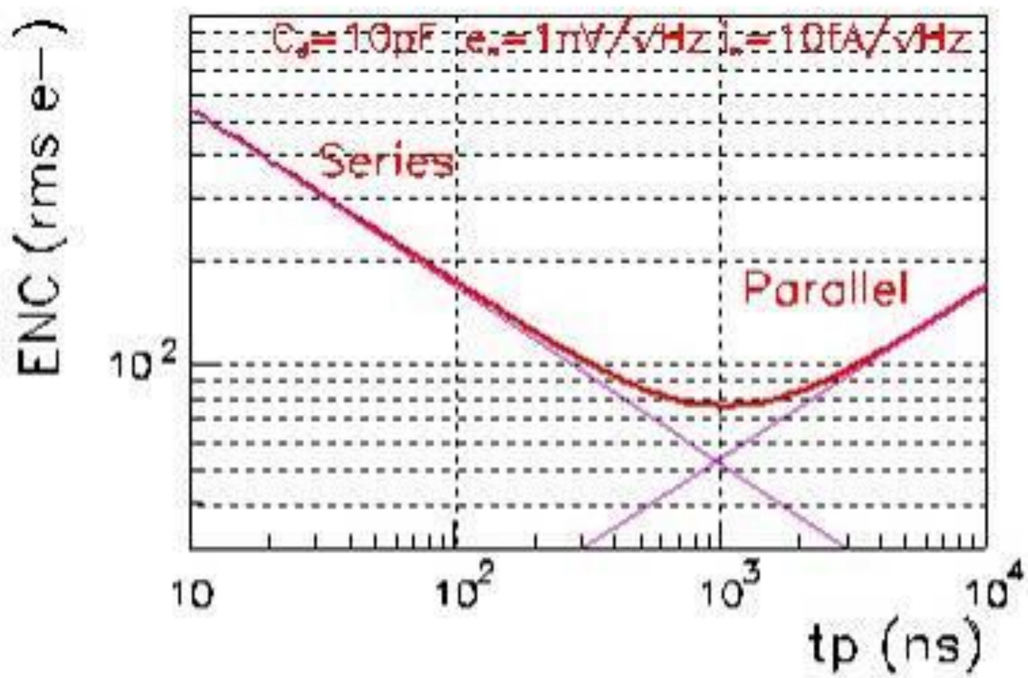
$$ENC = 174\, e_n C_{tot} / \sqrt{t_p}\, (\delta) \oplus 166\, i_n \sqrt{t_p}\, (\delta)$$

  - e_n in nV/ √Hz, i_n in pA/ √Hz are the preamp noise spectral densities
  - C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
  - t_p (in ns) is the shaper peaking time (5-100%)

Noise minimization

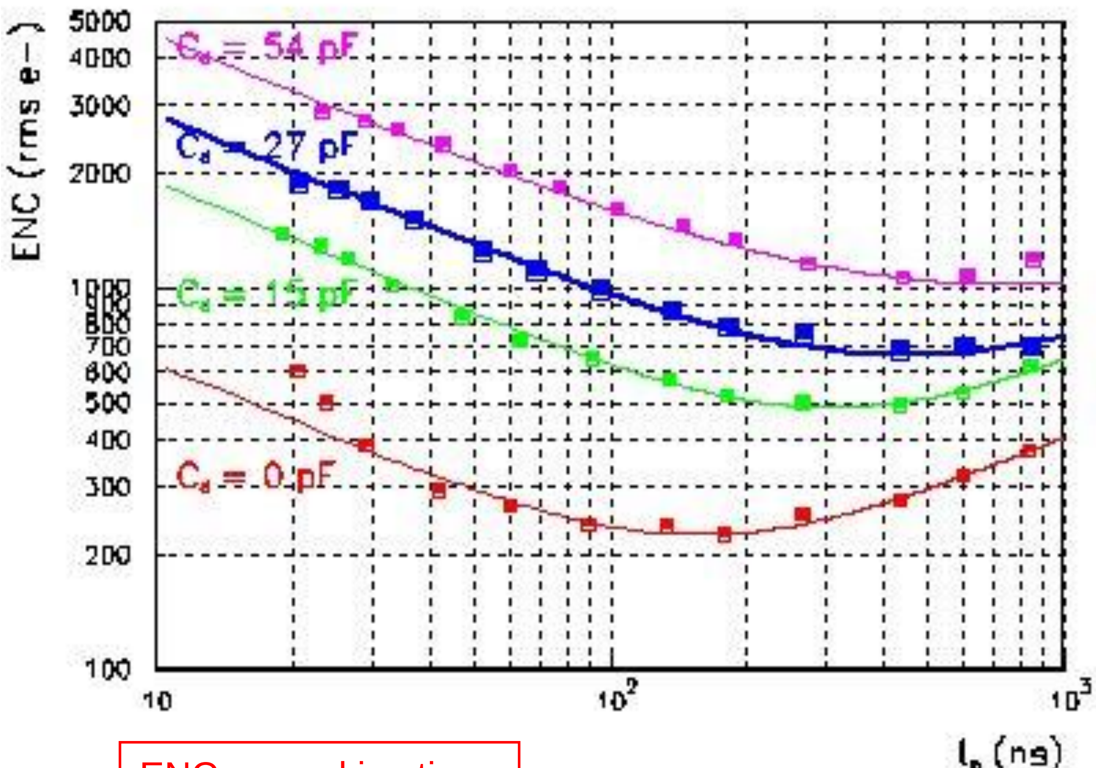
- Minimize source capacitance
- Operate at optimum shaping time
- Preamp series noise (en) best with high trans-conductance (g_m) in input transistor

  => large current, optimal size

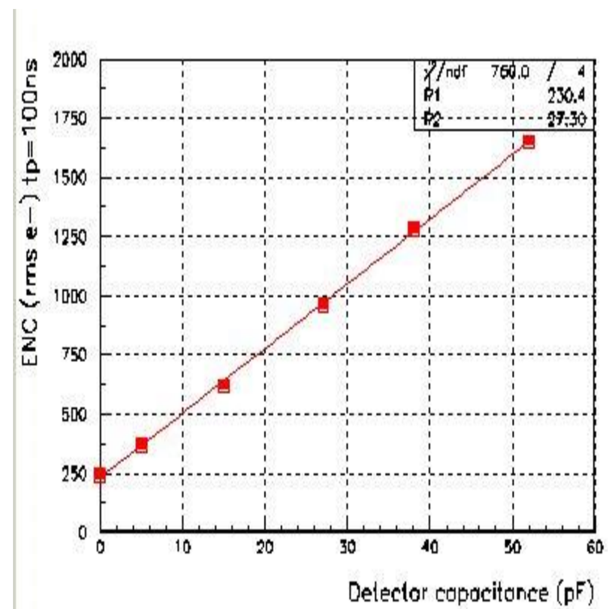


Example of ENC measurement

- 2000/0.35 PMOS 0.35µm SiGe Id=500 µA
  - Series : en = 1.4 nV/√Hz, C_{PA} = 7 pF
  - 1/f noise : 12 e-/pF
  - Parallel : in = 40 fA/√Hz

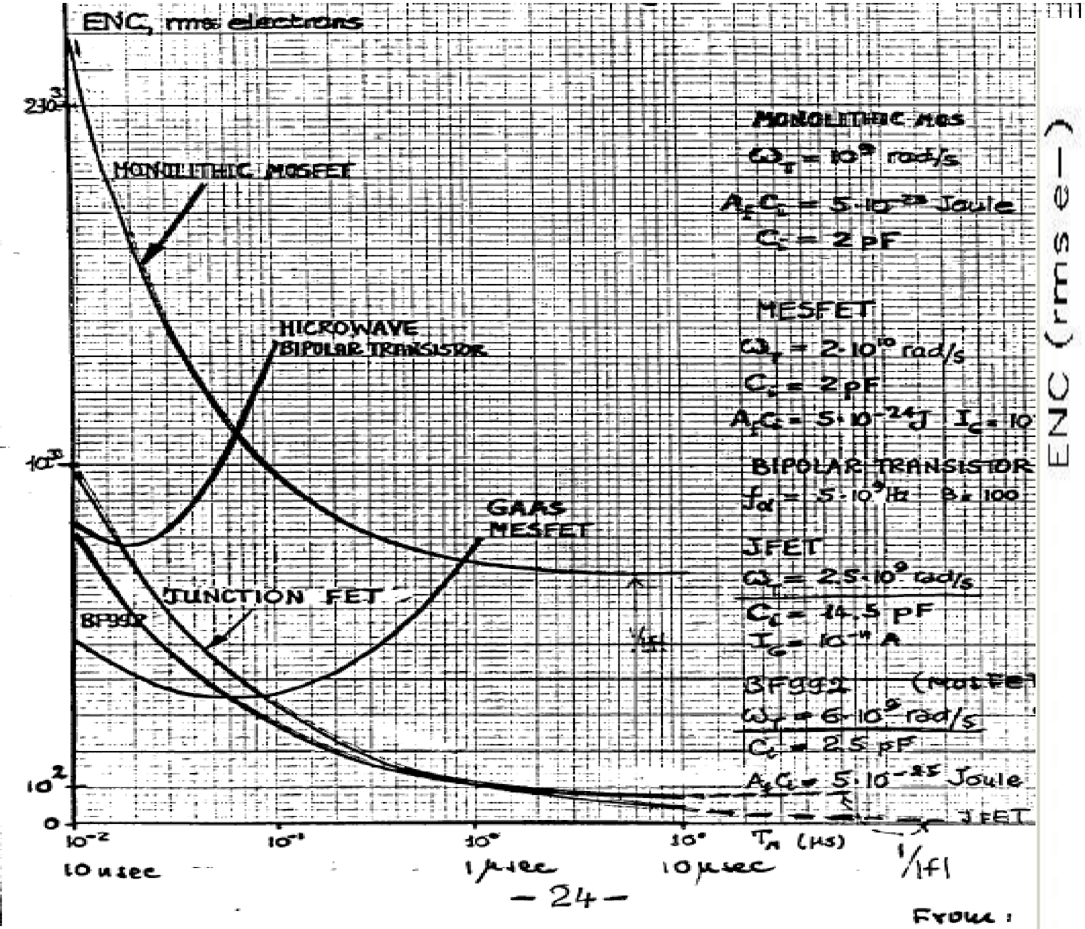


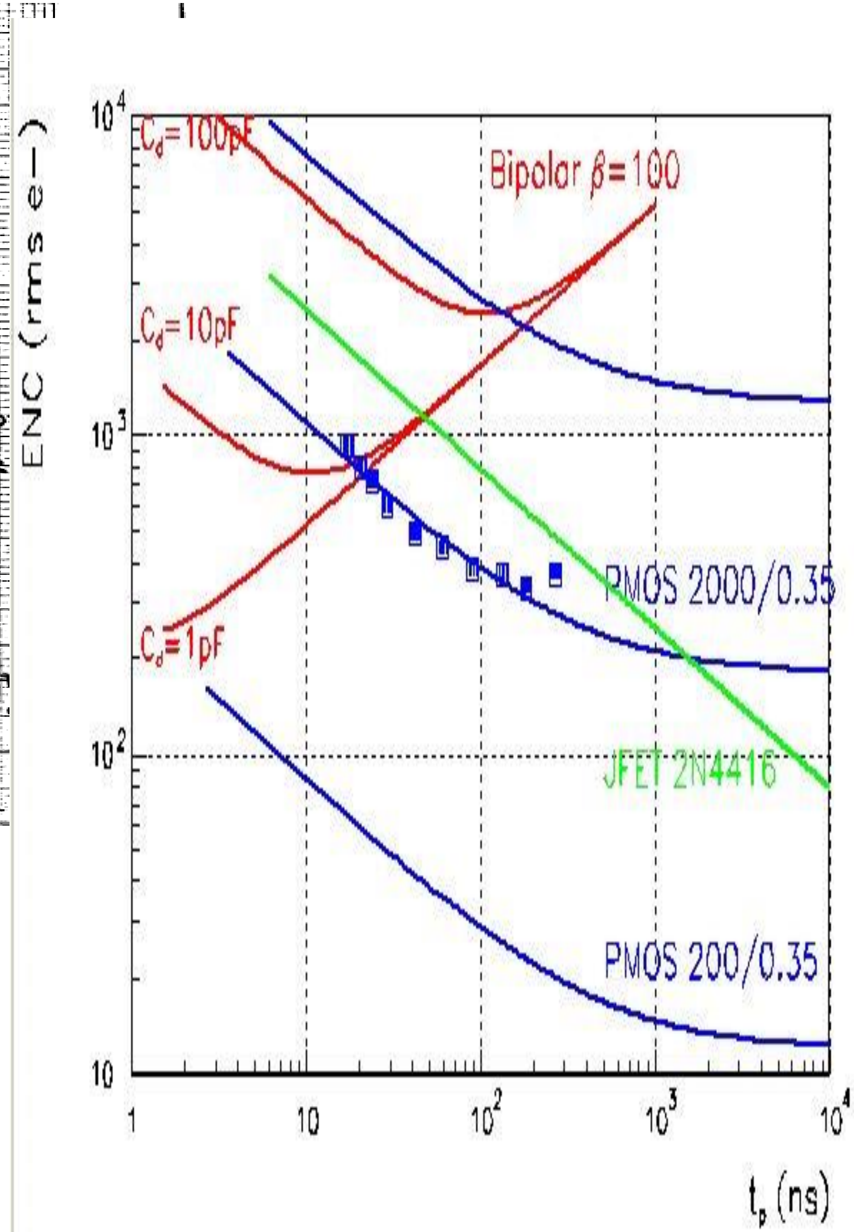
ENC vs peaking time



ENC vs Capacitance tp=100ns

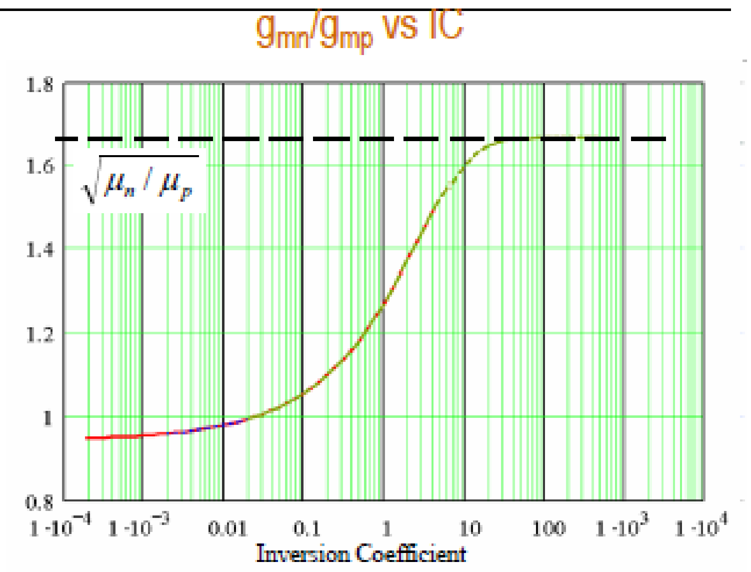
ENC for various technologies

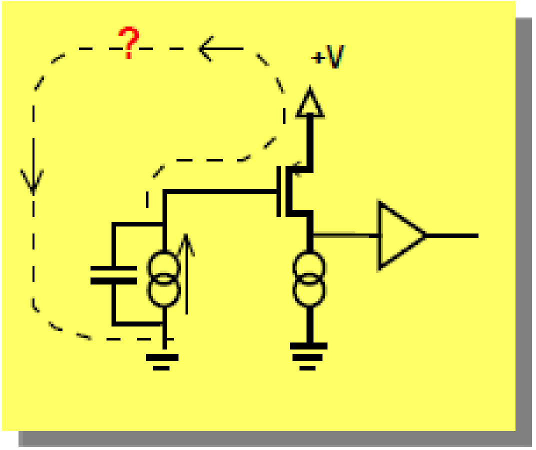


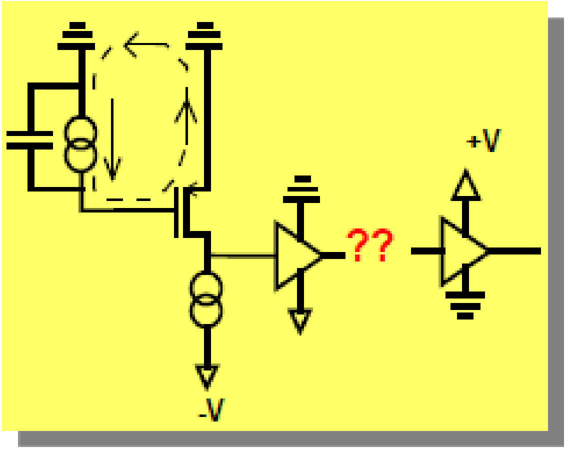


PMOS vs NMOS [Paul O'Connor BNL]

- *PMOS lower 1/f noise*
- *NMOS white series noise advantage over PMOS diminishes each generation*
- *PMOS can be operated at reverse V_{BS} to reduce bulk resistance noise*
- *PMOS lower tunneling current at ultra-thin t_{ox}*
- *Single-supply operation of PMOS-input preamp awkward:*



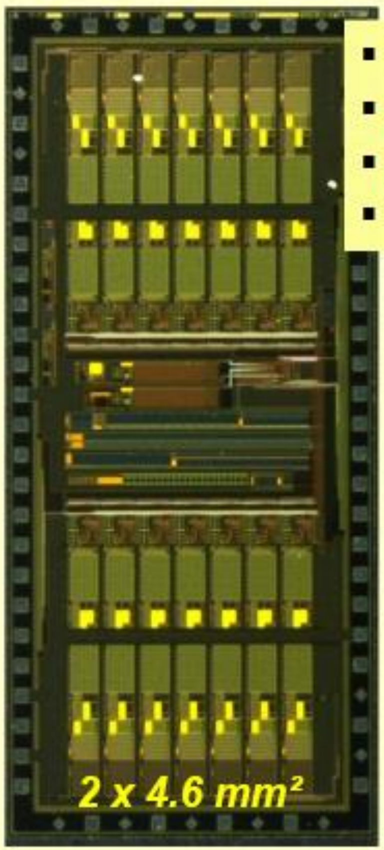




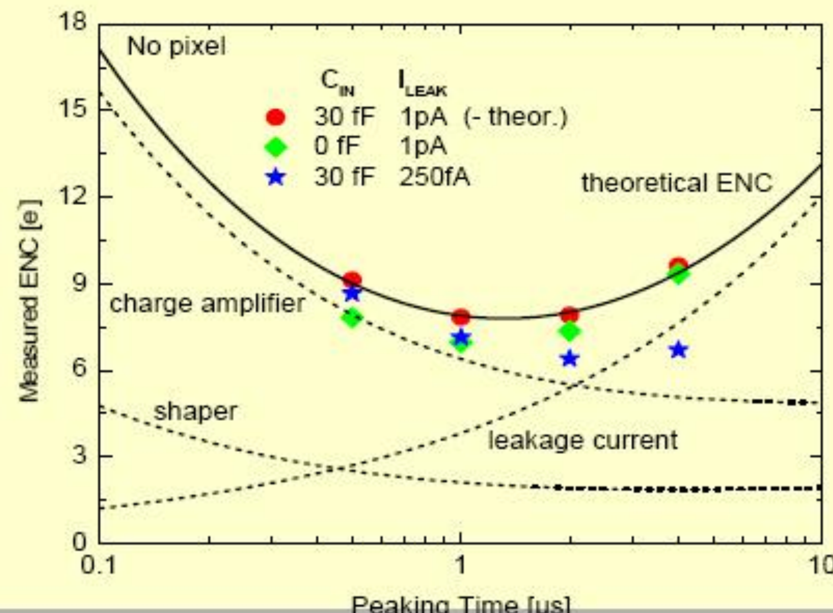
Ultra-Low Noise ASIC High Resolution X-Ray Spectroscopy

Collaboration with NASA at Moon Elemental Mapping

16 mm² Semiconductor Drift Pixels, 500 cm²



- 14 channels, 1.2 mW/channel
- sub-10 electrons resolution
- peak detection and sparse readout
- 30,000 transistors, dev. time: 15 months



G. De Geronimo et al., NSS (2007)

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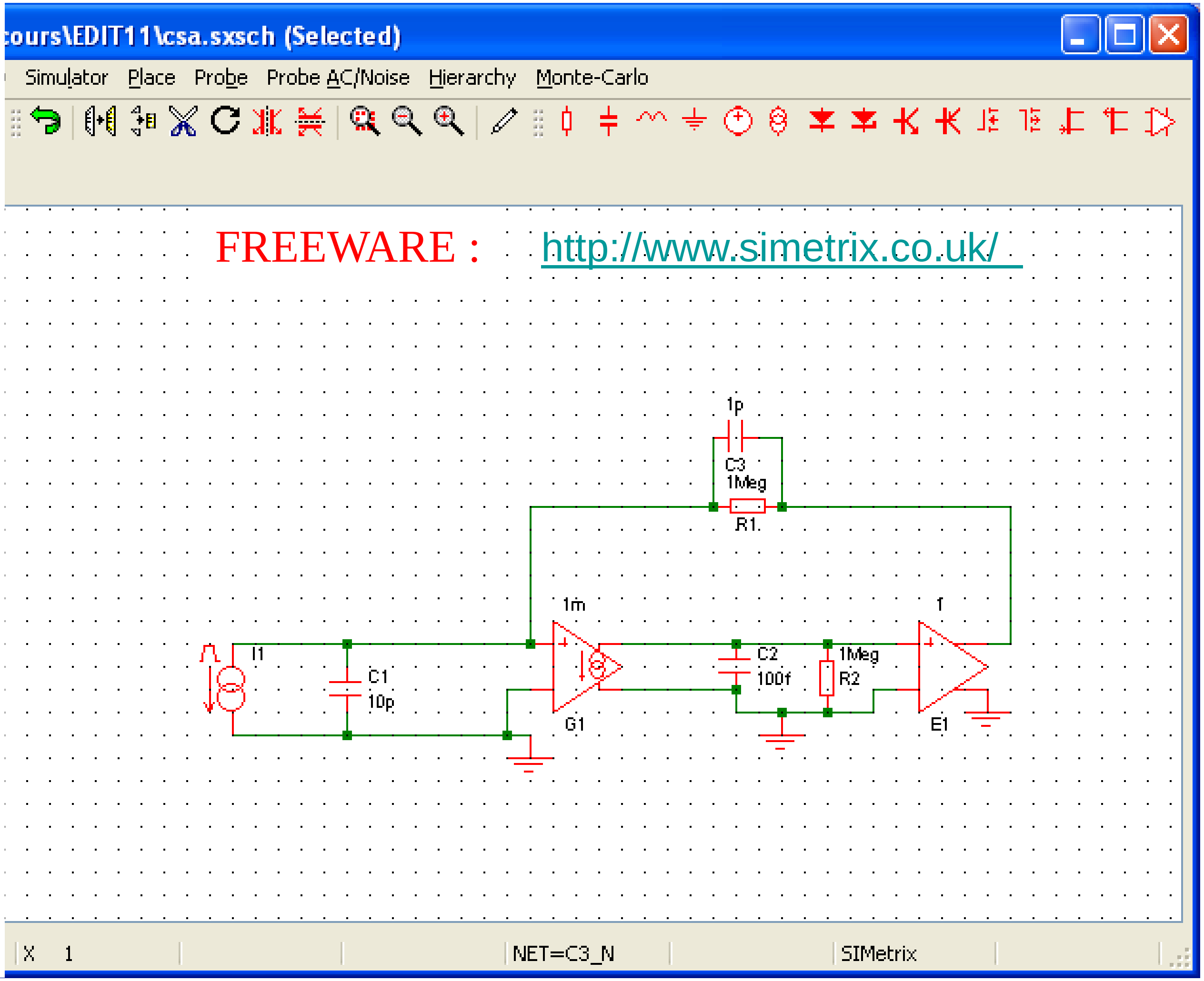
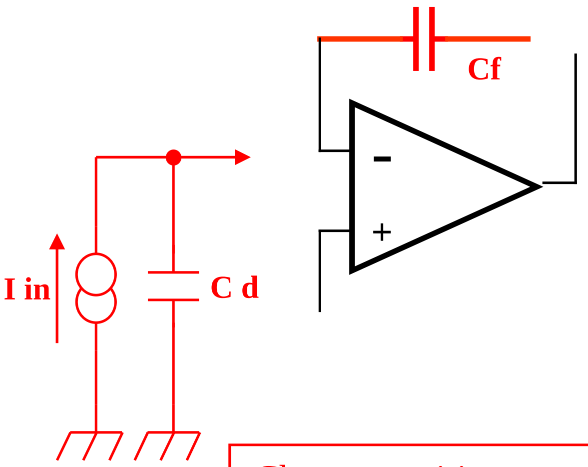
Example : bandwidth and EMC of simple charge preamp

- Simulate impulse response
- Frequency response
- Input impedance
- Ballistic deficit
- Effect of amplifier gain
- Effect of resistive feedback
- Test pulse injection
- Effect of input capacitance
- Parasitic inductance
- Capacitive crosstalk
- Resistive/Inductive ground return

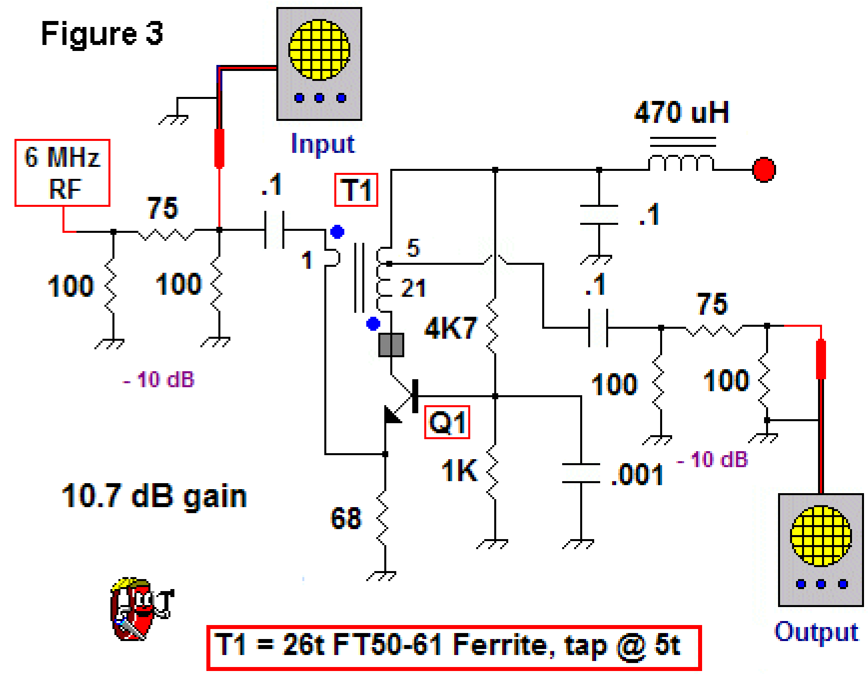


- Importance of front-end on electronics on physics performance
- Benefits of charge preamplifiers : low noise, low crosstalk
  - The front-end of 90% of particle physics detectors…
  - But always built with custom circuits…

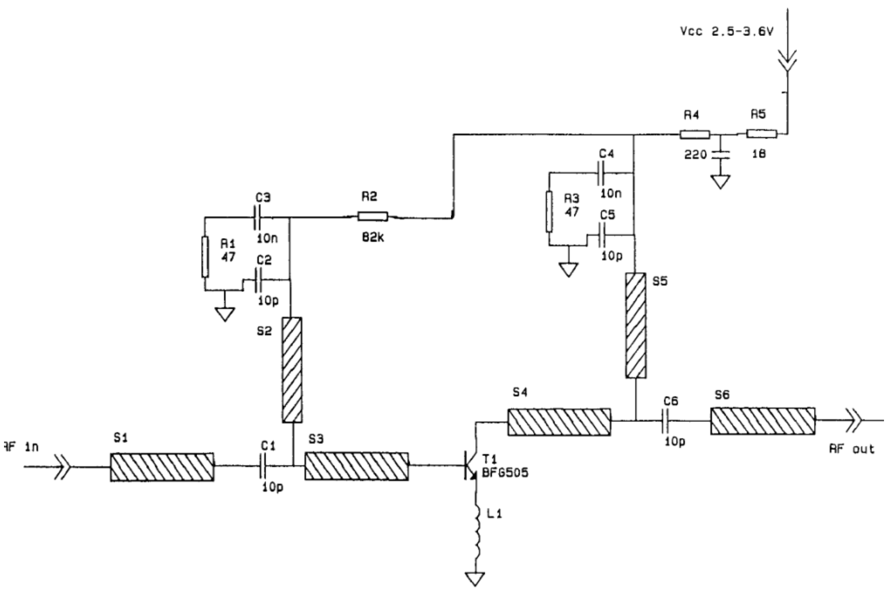


Charge sensitive preamp :
Vout = -Q/Cf

Figure 3



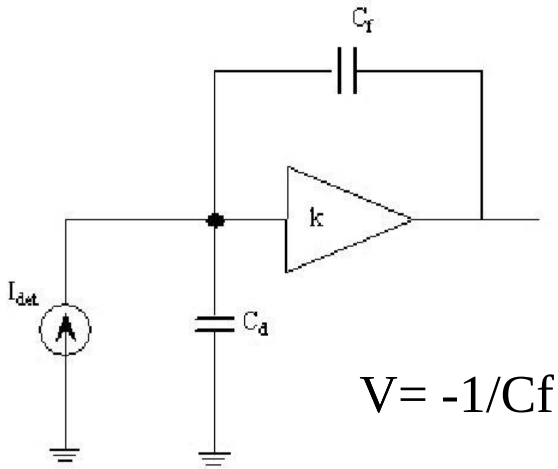
Input
6 MHz RF
75
.1
T1
100
100
1
5
21
4K7
470 uH
.1
.1
75
100
100
- 10 dB
Q1
1K
.001
- 10 dB
10.7 dB gain
68
T1 = 26t FT50-61 Ferrite, tap @ 5t
Output



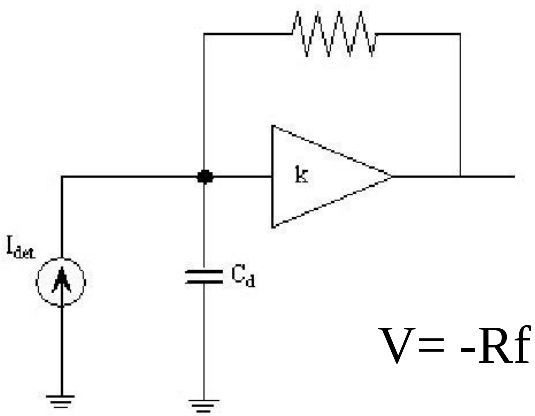
Vcc 2.5-3.6V
R4
R5
220
18
C4
10n
R3
47
C5
10p
C3
R2
R1
47
10n
C2
82k
10p
S2
S5
S4
C6
S6
S1
C1
S3
10p
10p
T1
BFG505
L1
RF out

- Charge preamp
- Capacitive feedback Cf
- Vout/Iin = - 1/jωCf
- Perfect integrator : vout=-Q/Cf∫
- Difficult to accomodate large SiPM signals (200 pC)
- Lowest noise configuration
- Need Rf to empty Cf

- Current preamp
- Resistive feedback Rf
- Vout/Iin = - Rf
- Keeps signal shape
- Need Cf for stability



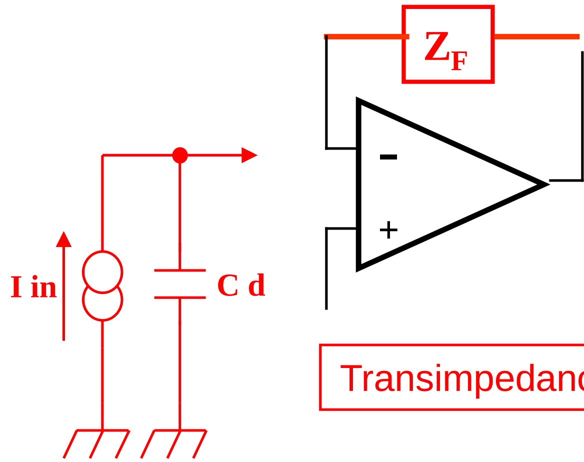
$$V = -1/Cf \int i(t)dt$$



$$V = -Rf\ i(t)$$

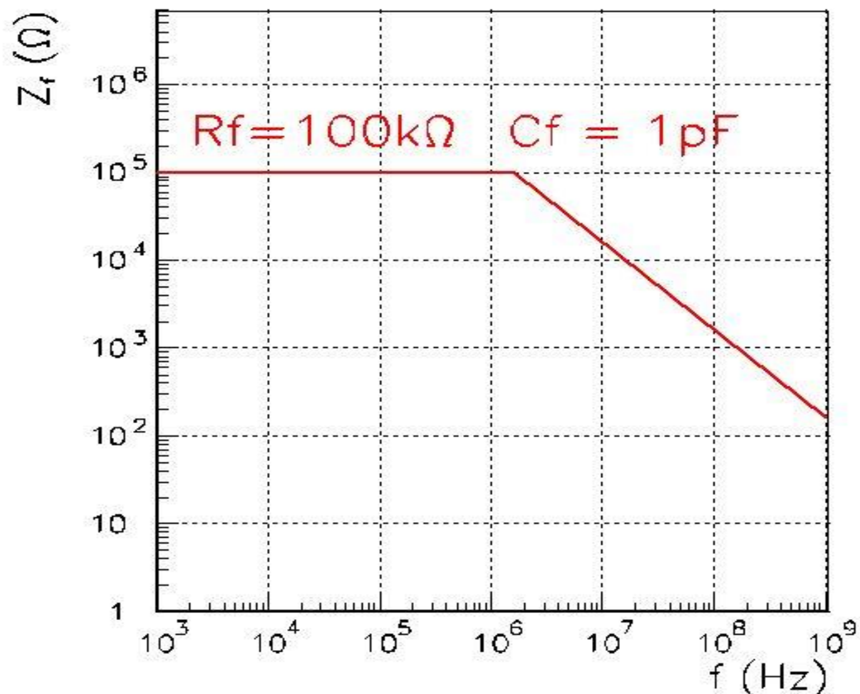
Transimpedance configuration

- Transfer function
  - Using a VFOA with gain G
    - $V_{out} - v_{in} = - Z_f \, i_f$
    - $V_{in} = Z_d \, (i_{in} - i_f) = - v_{out}/G$
  - $V_{out}(\omega)/i_{in}(\omega) = - Z_f / (1 + Z_f / G Z_d)$



Transimpedance amplifier

- $Zf = Rf / (1 + j\omega \, RfCf)$
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - R_f$
    current preamp
  - At $f << 1/2\pi RfCf$:
    $V_{out}(\omega)/i_{in}(\omega) = - 1/j\omega C_f$
    charge preamp



Transfer function

- Ballistic deficit with charge preamp
  - Effect of finite gain : G_0
  - Output voltage «only» Q $C_d/G_0 C_f$

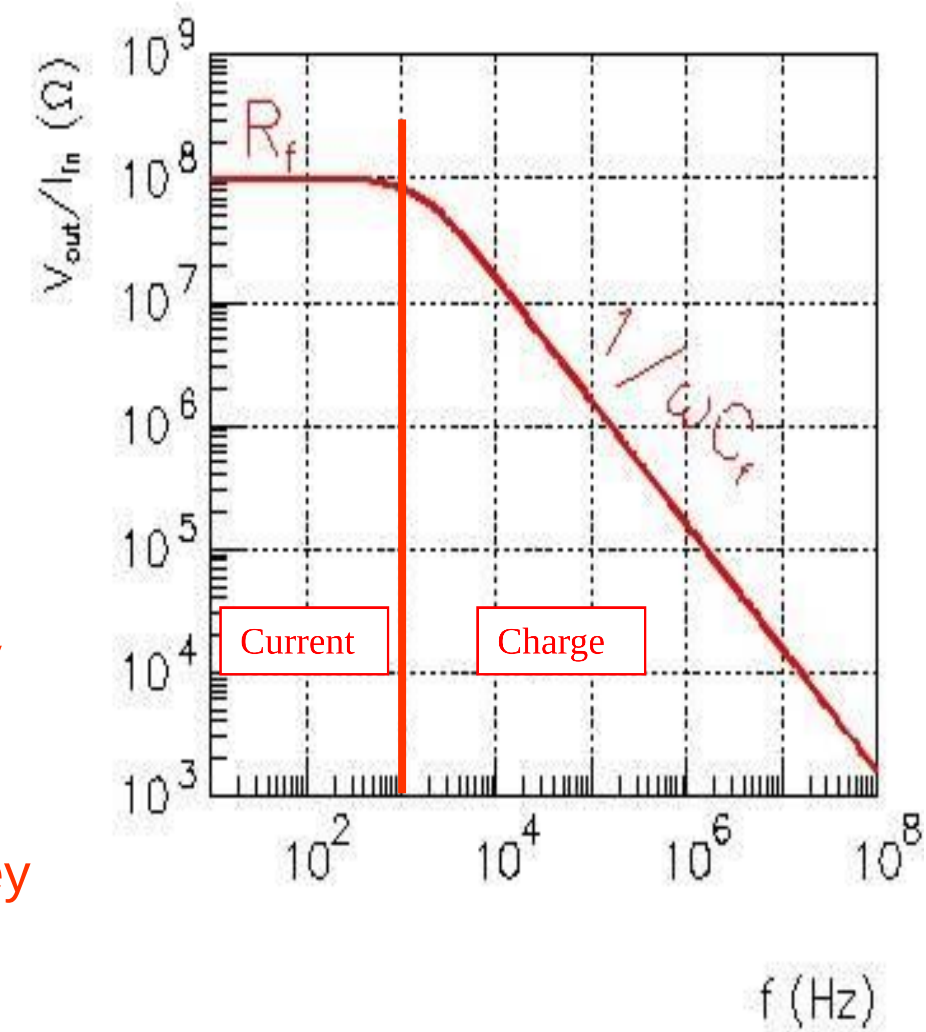
Charge vs Current preamps

- Charge preamps
  - Best noise performance
  - Best with short signals
  - Best with small capacitance

- Current preamps
  - Best for long signals
  - Best for high counting rate
  - Significant parallel noise

- Charge preamps are <u>not slow</u>, they are <u>long</u>

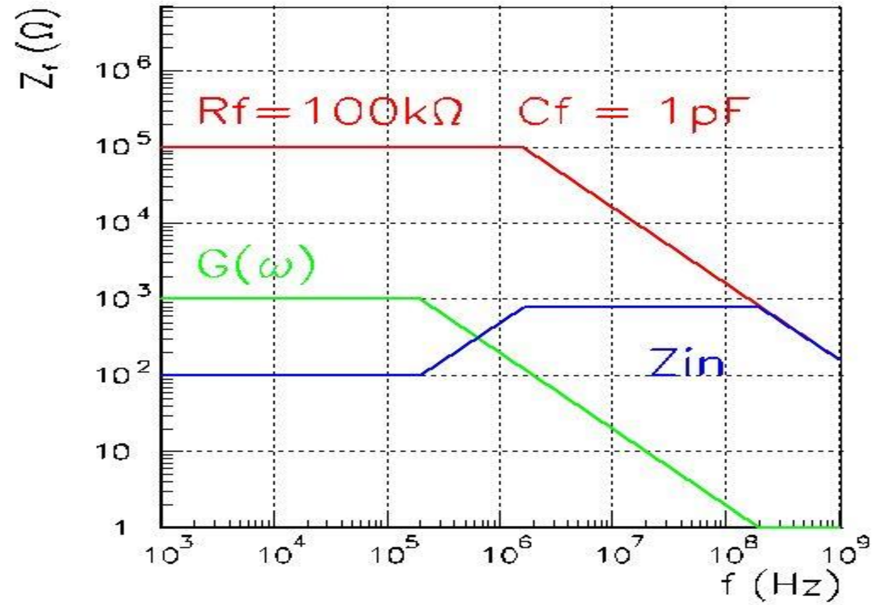
- Current preamps are <u>not faster</u>, they are <u>shorter</u> (but easily unstable)



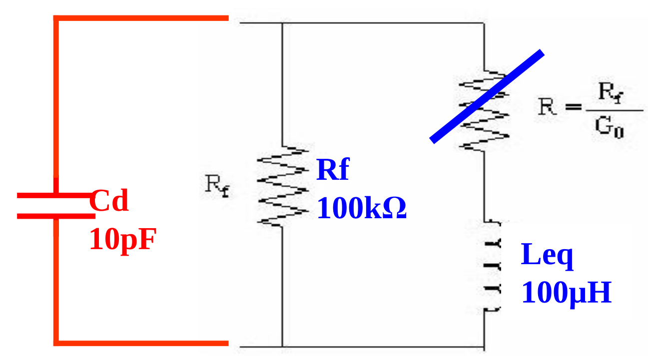
Input impedance

- Input impedance
  - Zin = Zf / G+1
  - Zin->0 virtual ground
  - Minimizes sensitivity to detector impedance
  - Minimizes crosstalk

- Equivalent model
  - $G(\omega) = G_0/(1 + j\,\omega/\omega_0)$
- Terms due to Cf
  - $Zin = 1/j\omega\, G_0C_f + 1/\, G_0\omega_0\, C_f$
  - Virtual resistance : $Req = 1/\, G_0\omega_0\, C_f$
- Terms due to Rf
  - $Zin = R_f/\, G_0 + j\,\omega\, R_f/\, G_0\omega_0$
  - Virtual inductance : $Leq = R_f/\, G_0\omega_0$
- Possible oscillatory behaviour with capacitive source

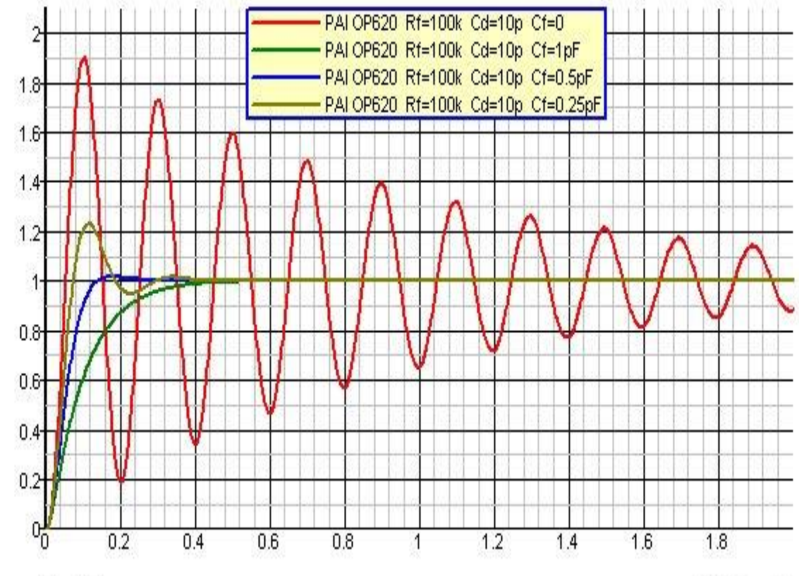


Input impedance or TZA

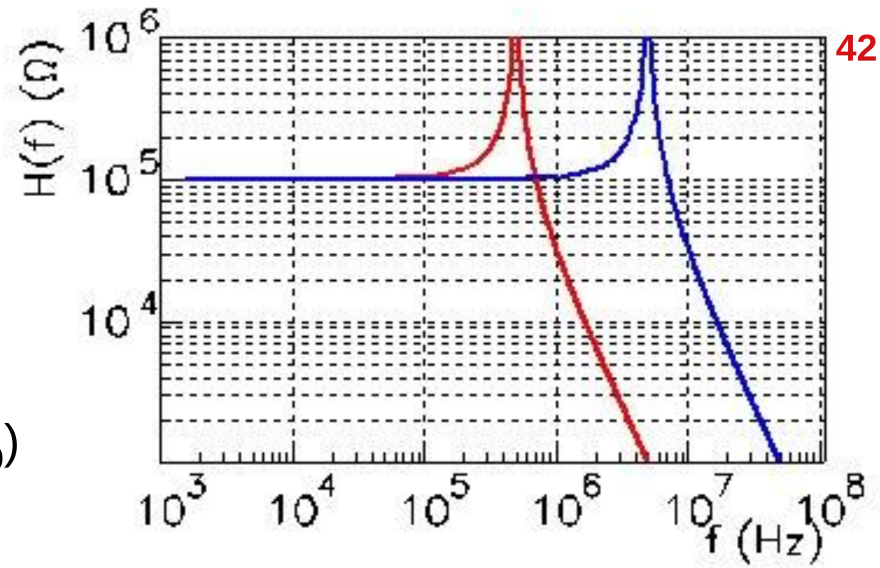


Equivalent circuit at the input

- Easily oscillatory
  - Unstable with capacitive detector
  - Inductive input impedance :
    $L_{eq} = R_f / \omega_C$
  - Resonance at : $f_{res} = 1/2\pi \sqrt{L_{eq} C_d}$
  - Quality factor : $Q = R / \sqrt{L_{eq}/C_d}$
    - $Q > 1/2$ -> ringing
  - Damping with capacitance C_f
    - $C_f = 2 \sqrt{(C_d / R_f\, G_0 \omega_0)}$
    - Easier with fast amplifiers



Step response of current sensitive preamp

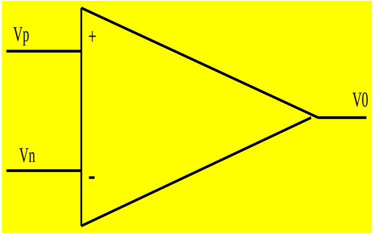


- In frequency domain
  - $H(j\omega) = -Rf / (1 + j\omega\, RfC_d/))$
  - $G(\omega) = G_0 / (1 + j\omega/\omega_0)$

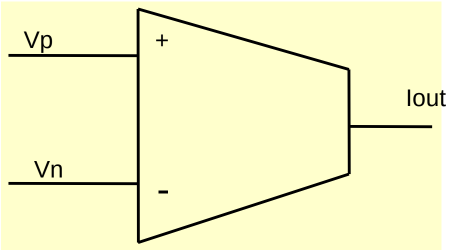
$H = - Rf / (1 + j\omega\, R_f C_d / G_0 - \omega^2 R_f C_d / G_0 \omega_0)$

Amplifiers : a large zoo

- Voltage feedback operationnal amplifier (VFOA)
- Voltage amplifiers, RF amplifiers (VA,LNA)
- Current feedback operationnal amplifiers (CFOA)
- Current conveyors (CCI, CCII +/-)
- Current (pre)amplifiers (ISA,PAI)
- Charge (pre)amplifiers (CPA,CSA,PAC)
- Transconductance amplifiers (OTA)
- Transimpedance amplifiers (TZA,OTZ)

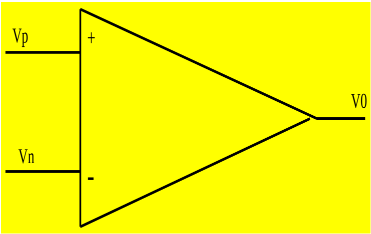


- Mixing up open loop (OL) and closed loop (CL) configurations !

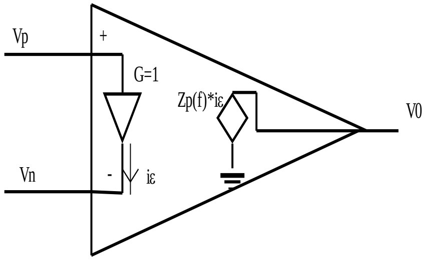


Only 4 open-loop configurations

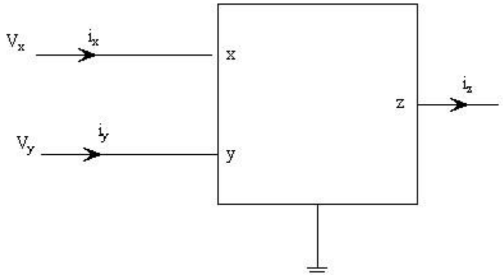
- Voltage operationnal amplifiers (OA, VFOA)
  - Vout = G(ω) Vin diff
  - Zin+ = Zin- = ∞   Zout = 0



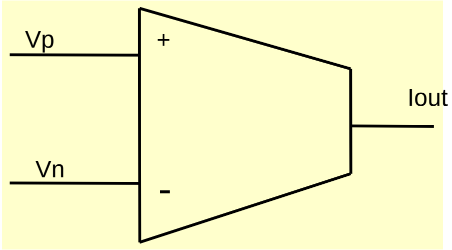
- Transimpedance operationnal amplifier (CFOA !)
  - Vout = Z(ω) iin
  - Zin- = 0   Zout = 0



- Current conveyor (CCI,CCII)
  - Iout = G(ω) Iin
  - Zin = 0   Zout = ∞

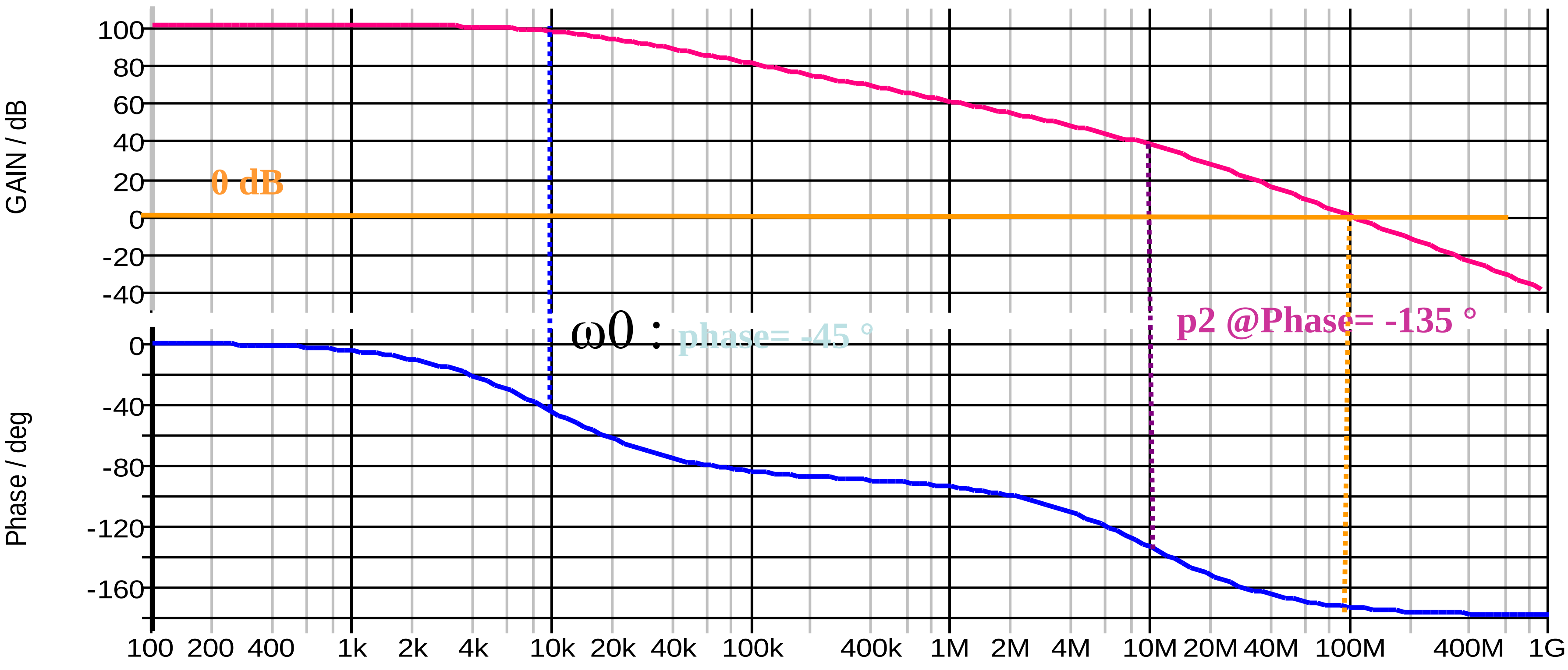


- Transconductance amplifier (OTA)
  - Iout = Gm(ω) Vin diff
  - Zin+ = Zin- = ∞   Zout = ∞

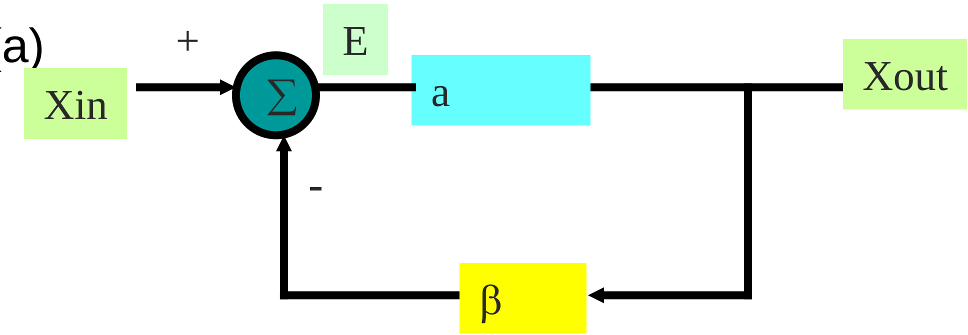


Open loop gain variation with frequency

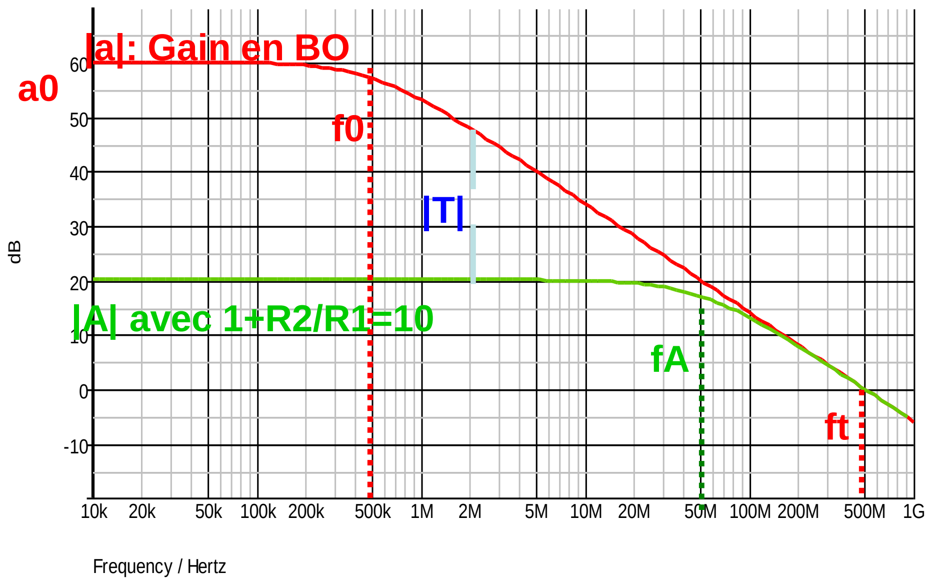
- Define exactly what is « gain » vout/vin, vout/iin…
- « Gain » varies with frequency : $G(j\omega) = G_0/(1 + j\ \omega/\omega_0)$
  - **G_0** low frequency gain
  - **ω_0** dominant pole
  - **$\omega_C = G_0\ \omega_0$** Gain-Bandwidth product (sometimes referred to as unity gain frequency)



- Improves gain performance
  - Less sensitivity to open loop gain (a)
  - Better linearity
- Essential in low power design
- Potentially unstable
- Feedback constant : β = E/Xout
- Open loop gain : a = Xout/E
- Closed loop gain : Xout/Xin -> 1/β
- Loop gain : T = 1/aβ

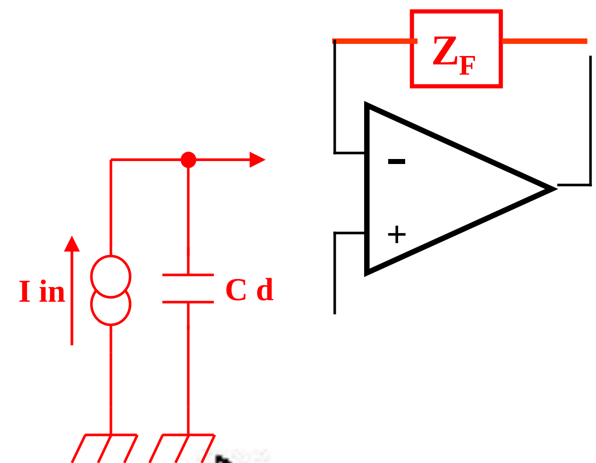


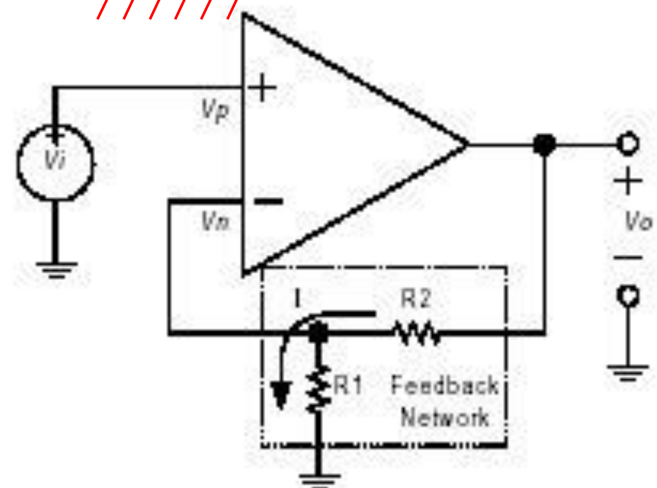
$$\frac{Xout}{Xin} = \frac{a}{1 + a\beta} = \frac{1/\beta}{1 + 1/a\beta}$$



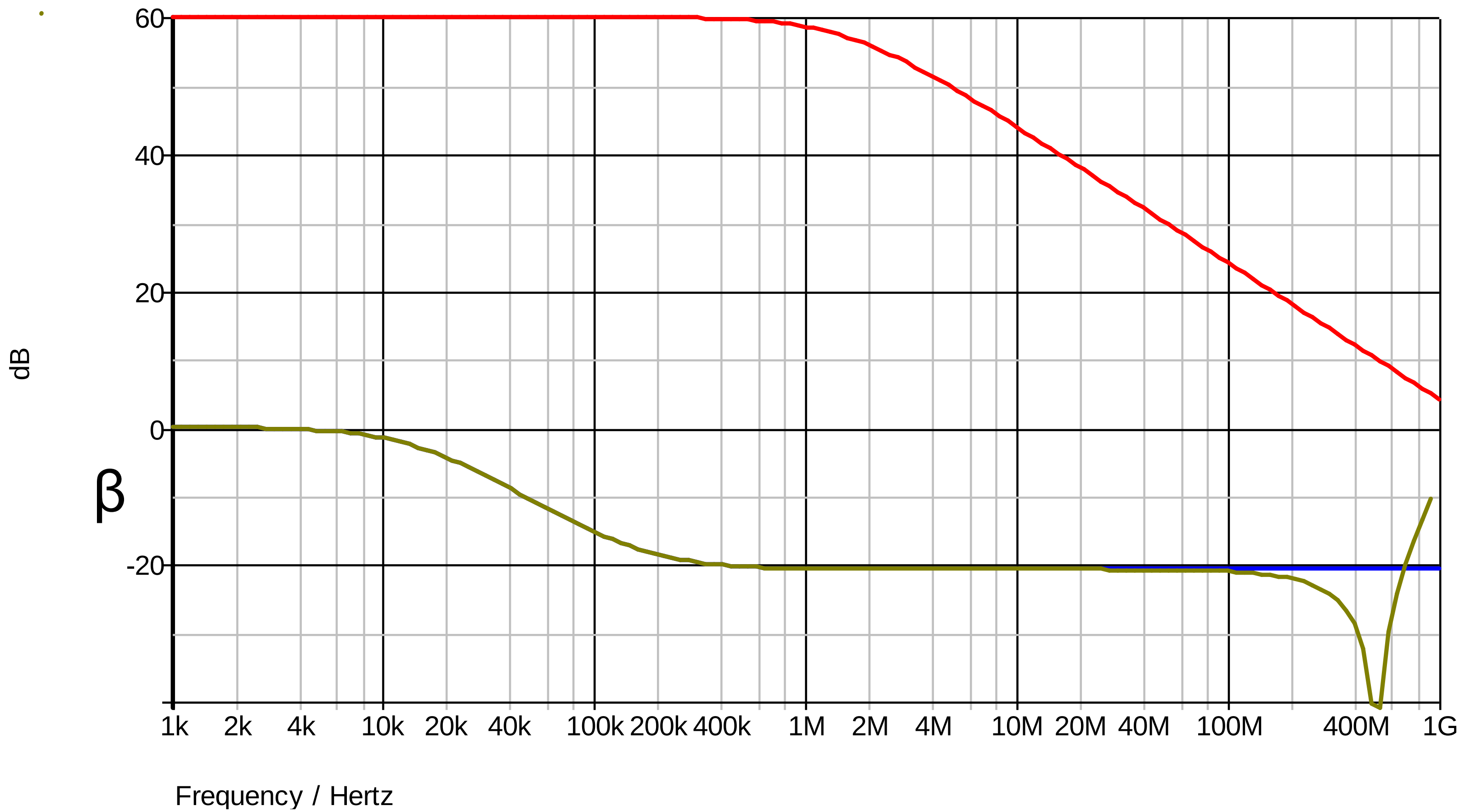
Only 4 feedback configurations

- Shunt-shunt = transimpedance
  - Small Zin (= Zin(OL)/T) -> current input
  - small Zout (= Zout(OL)/T) -> voltage output
  - De-sensitizes transimpedance = 1/β = Zf
- Series-shunt
  - Large Zin (= Zin(OL)*T) -> voltage input
  - Small Zout (= Zout(OL)/T) -> voltage output
  - Optimizes voltage gain (= 1/β)
- Shunt series
  - Small Zin (= Zin(OL)/T) -> current input
  - Large Zout (= Zout(OL)*T) -> current output
  - Current conveyor
- Series-series
  - Large Zin (= Zin(OL)*T) -> voltage input
  - Large Zout (= Zout(OL)*T) -> current output
  - Transconductance
  - Ex : common emitter with emitter degeneration





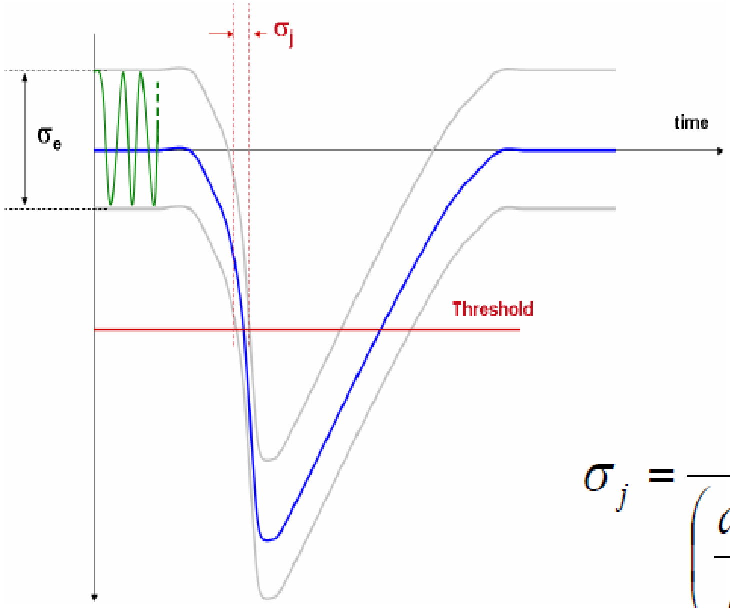
- Calculating β = E/Xout = Zd/(Zd+Zf)



Noise and jitter

- Electronics noise dominated by series noise en
  - Large detector capacitance
  - For voltage preamp and load resistor RL,
  - Output rms noise $Vn^2=(en^2+4kTRs)\ G^2\ \pi/2*BW_{-3dB}$
  - Typical values : Rs=50 Ω, en=1 nV/√Hz Vn=1 mV for G=10, BW=1GHz
  - For current sensitive preamps, possible noise peaking due to Cd

- Jitter
  - Part due to electronics noise :
  - $\sigma t = \sigma v / (dV/dt)$
  - Minimized by increasing BW

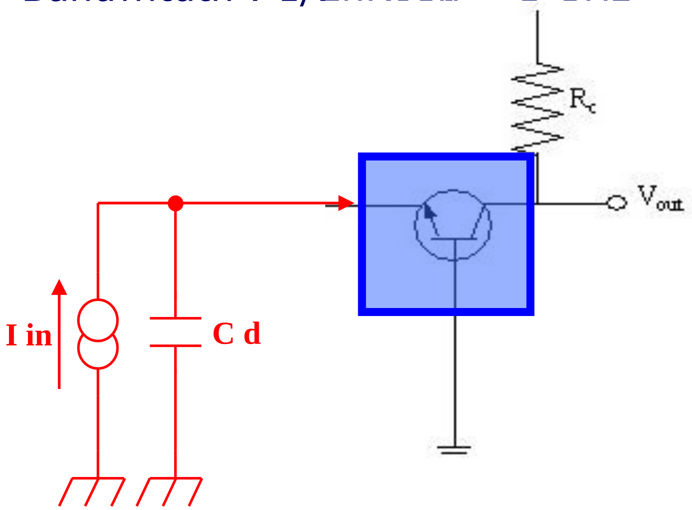


$$\sigma_j = \frac{\sigma_e}{\left(\frac{dV}{dt}\right)_{threshold}}$$

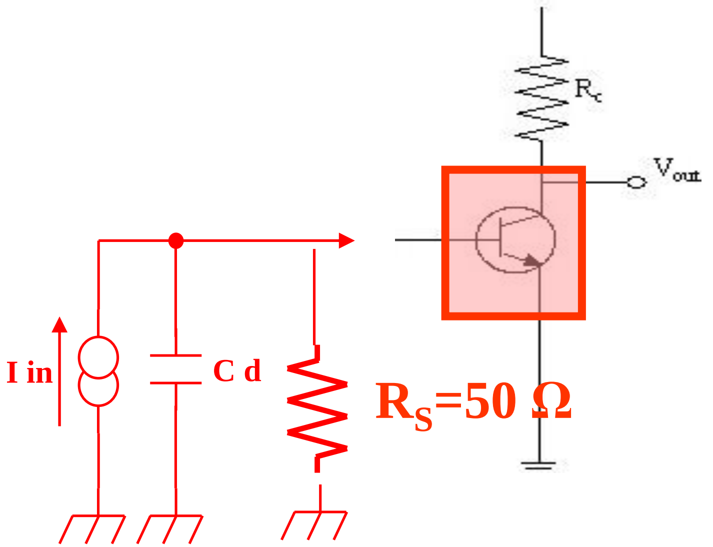
High speed configurations

- Open loop configurations : current conveyors, RF amplifiers
- Usually designed at transistor level MOS or SiGe

- **Current conveyors**
- Small Zin : current sensitive input
- Large Zout : current driven output
- Unity gain current conveyor
- E.g. : (super) common-base configuration
- Low input impedance : Rin=1/gm
- Transimpedance : Rc
- Bandwitdth : 1/2πRcCu > 1 GHz



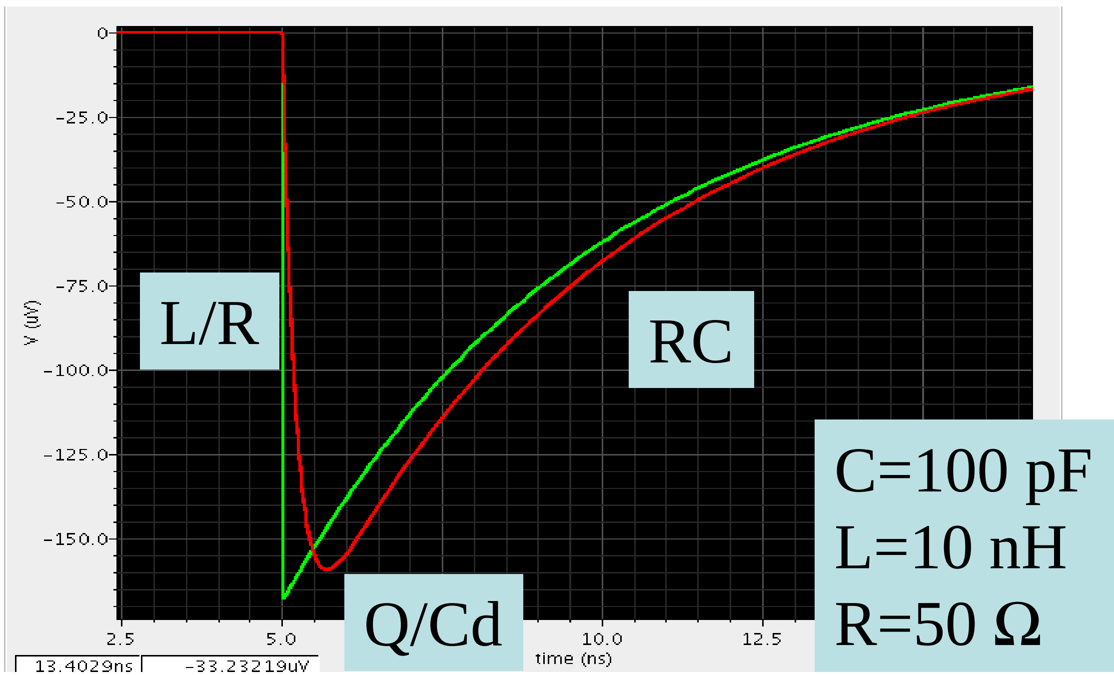
- **RF amplifiers**
- Large Zin : voltage sensitive input
- Large Zout : current driven output
- Current conversion with resistor R_S
- E.g. common-emitter configuration
- Transimpedance : -gmRcRs
- Bandwitdth : 1/2πRsCt

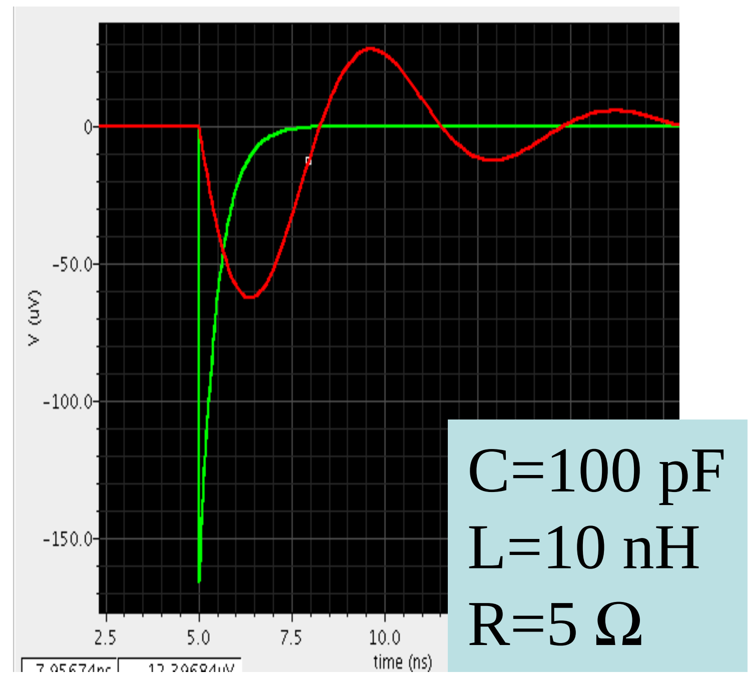


Examples of pulse shapes

Ωmega

- Short pulse : Q=16 fC, Cd=100 pF, L=0-10 nH, RL=5-50 Ω
- Smaller signals with SiPM (large Cd) ~ mV/p.e.
- Sensitivity to parasitic inductance
- Choice of RL : decay time, stability
- Convolve with current shape… (here delta impulse)





- Experimental measurements on SiGe test structures

Testboard #3	RF (Common Emitter)	Common Base	Super Common Base
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

With 1pe-=160 fC

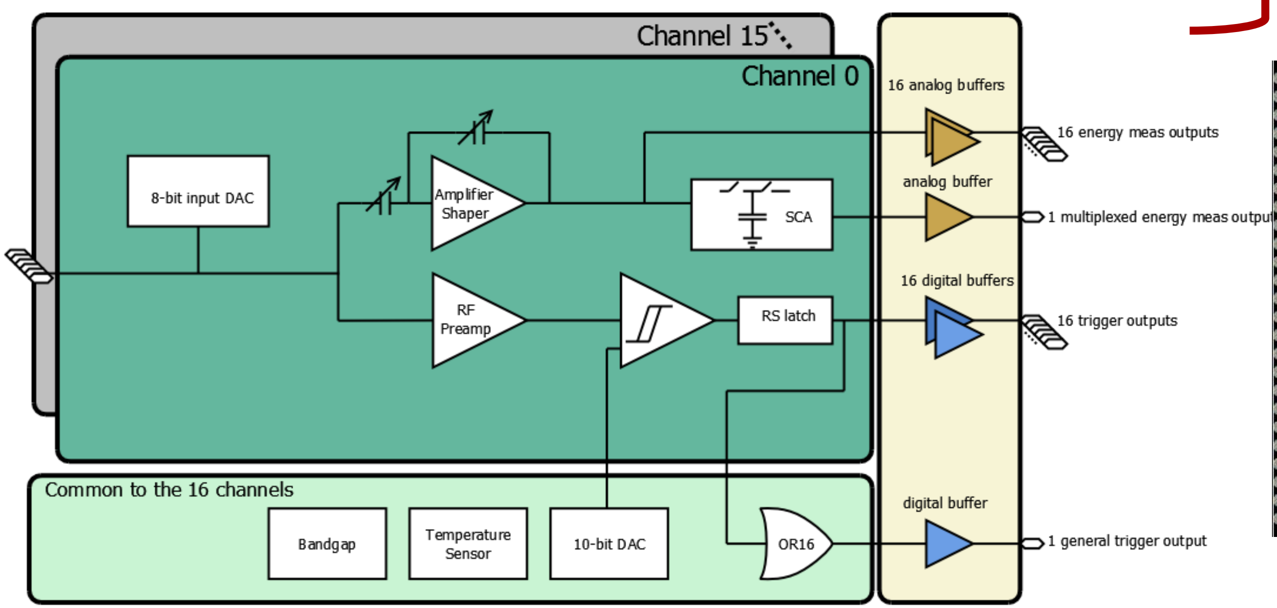
PETIROC [http://omega.in2p3.fr]

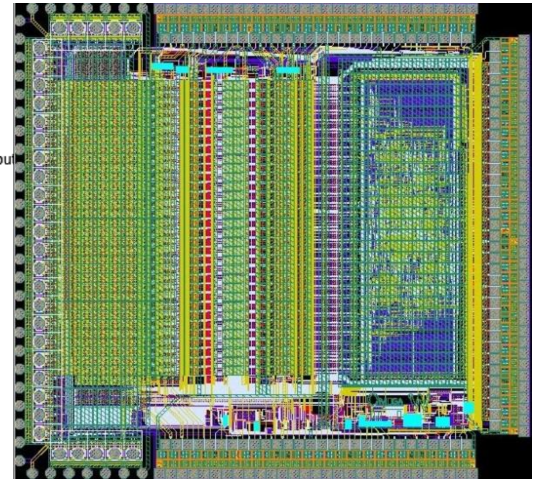
Omega

- 16 channels, prototyping ASIC
- 16 discriminator output, 16 charge output, MUX charge output, Trigger OR
- Power consumption 3.5mW/ch
- RF, common emitter SiGe fast amplifier, DC coupled to detector, GBWP 10GHz@1mW
- Fast SiGe discriminator, BW 1GHz @ 1.5mW
- Low noise amp+shaper for charge measurement
  - Adjustable peaking time (25ns, 50ns, 75ns, 100ns)
  - Low gain for high swing (up to 3000pe) : 360uV/pe

PETIROC2
- **32 channels**
- **Internal ADC/TDC**

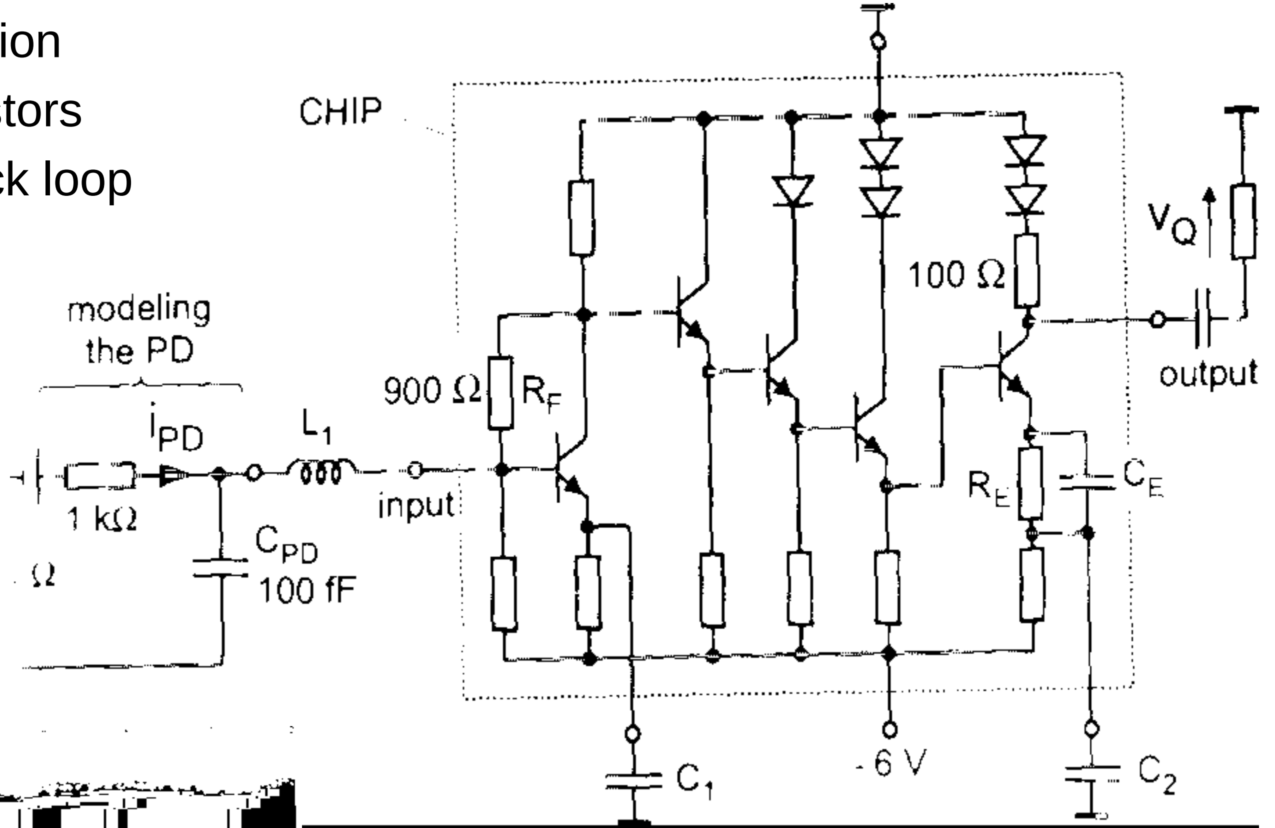
weeroc

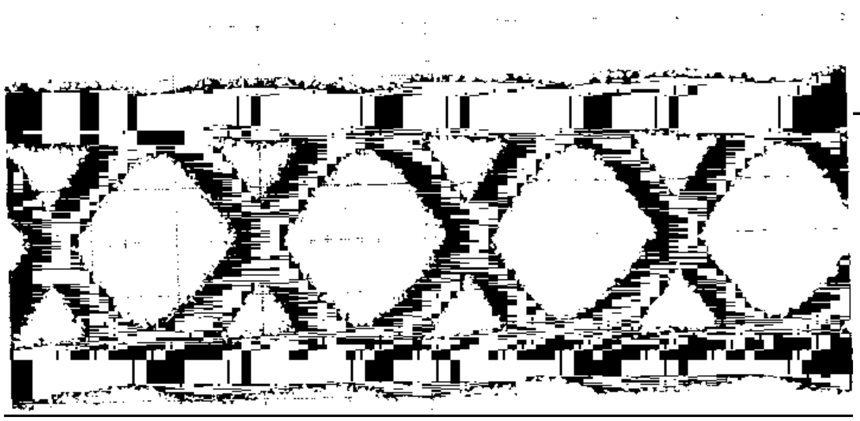




40 Gb/s transimpedance amplifier

- « Simple architecture »
  - CE + CC configuration
  - SiGe bipolar transistors
  - CC outside feedback loop
  - « pole splitting »



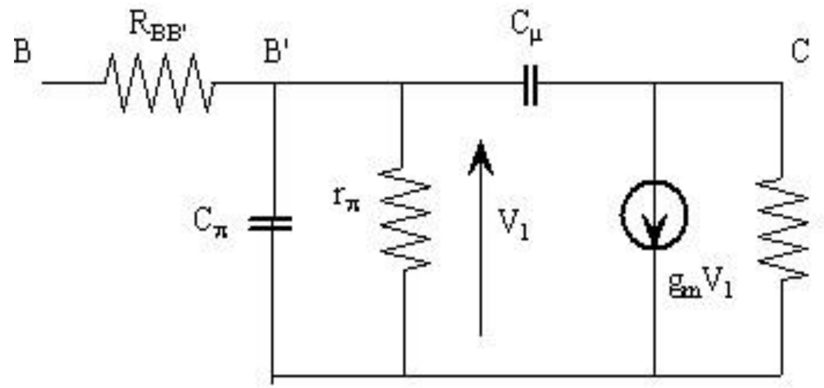


A few (personal) comments

- Strong push for high speed front-end > GHz
  - Essential for timing measurements
  - Several configurations to get GBW > 10 GHz
  - Optimum use of SiGe bipolar transiistors
- Voltage sensitive front-end
  - Easiest : 50Ω termination, many commercial amplifiers (mini circuit…)
  - Beware of power dissipation
  - Easy multi-gain (time and charge)
- Current sensitive front-end
  - Potentially lower noise, lower input impdance
  - Largest GBW product
- In all cases, importance of reducing stray inductance

Summary of transistor level design

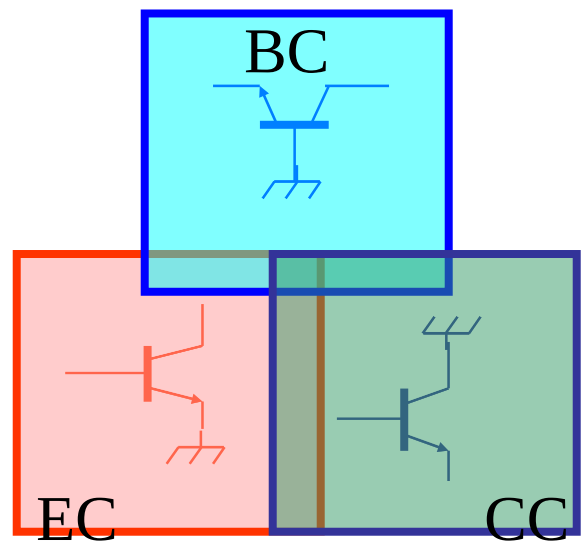
- Performant design is at transistor level



High frequency hybrid model of bipolar

- Simple models
  - hybrid π model
  - Similar for bipolar and MOS
  - Essential for design

- **Three basic configurations**
  - Common emitter (CE) = V to I (transconductance)
  - Common collector (CC) = V to V (voltage buffer)
  - Common base (BC) = I to I (current conveyor)

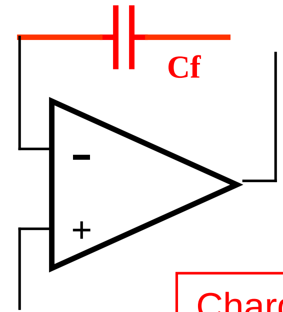


The *Art* of electronics design

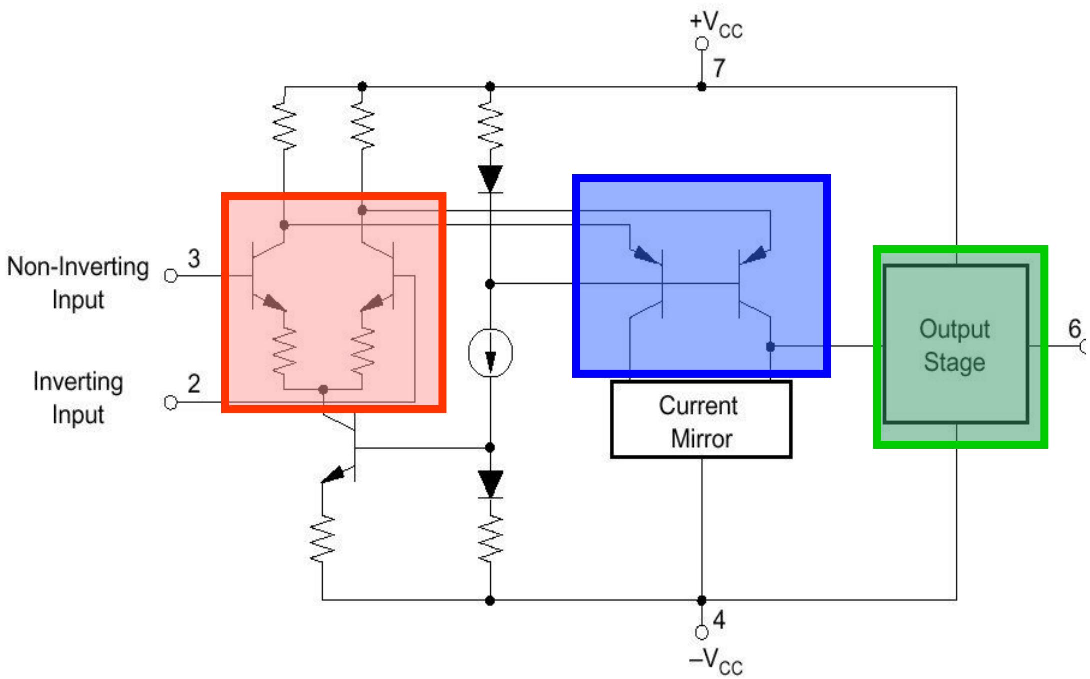
- Numerous « composites »
  - Darlington, Paraphase, Cascode, Mirrors…

Designing a charge preamp…

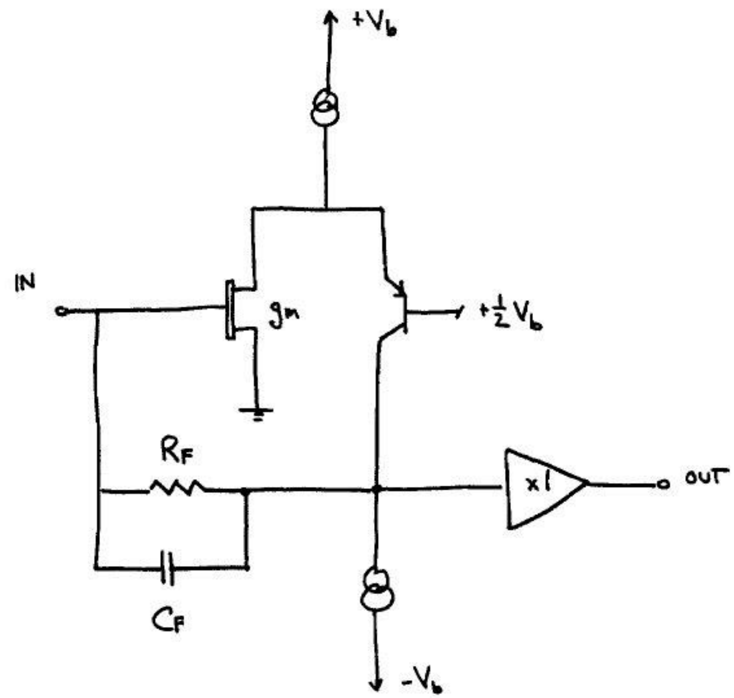
- From the schematic of principle
  - Using of a fast opamp (OP620)
  - Removing unnecessary components…
  - Similar to the traditionnal schematic «Radeka 68 »
  - Optimising transistors and currents



Charge preamp



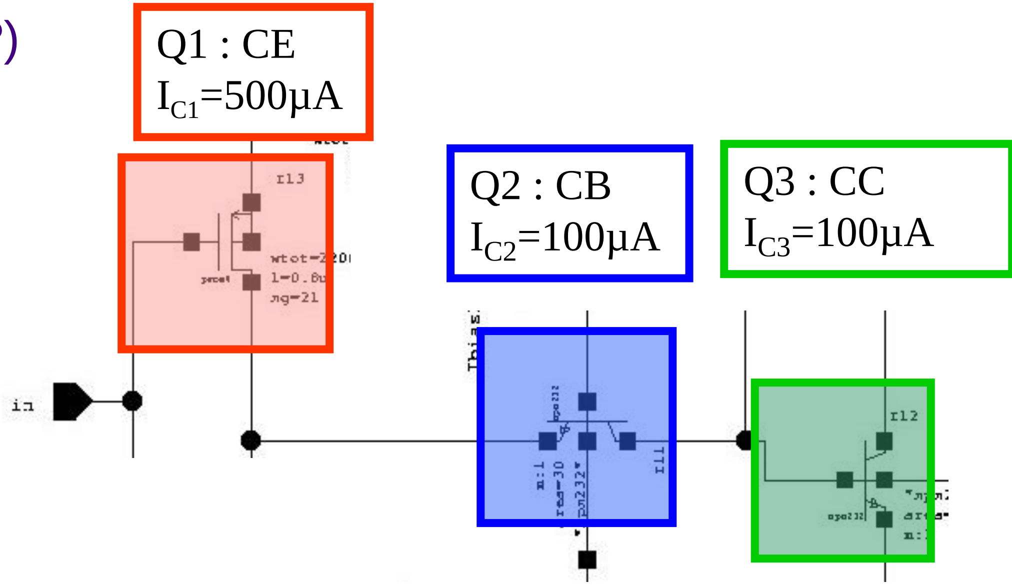
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

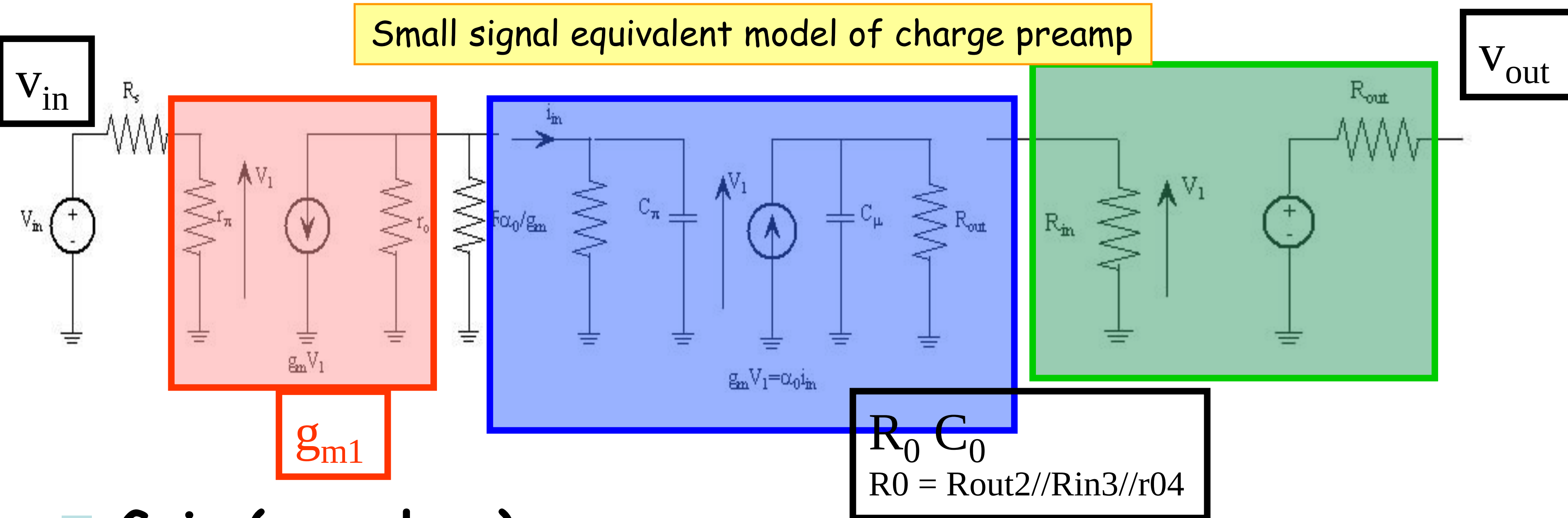
Example : designing a charge preamp (2)

- Simplified schematic
- Optimising components
  - What transistors (PMOS, NPN ?)
  - What bias current ?
  - What transistor size ?
  - What is the noise contribution of each component ?
  - how to minimize it ?
  - What parameters determine the stability ?
  - Waht is the saturation behaviour
  - How vary signal and noise with input capacitance ?
  - How to maximise the output voltage swing ?
  - What is the sensitivity to power supplies, temperature…



Simplified schematic of Charge preamp

- Small signal equivalent model
  - Transistors are replaced by hybrid π model
  - Allows to calculate open loop gain

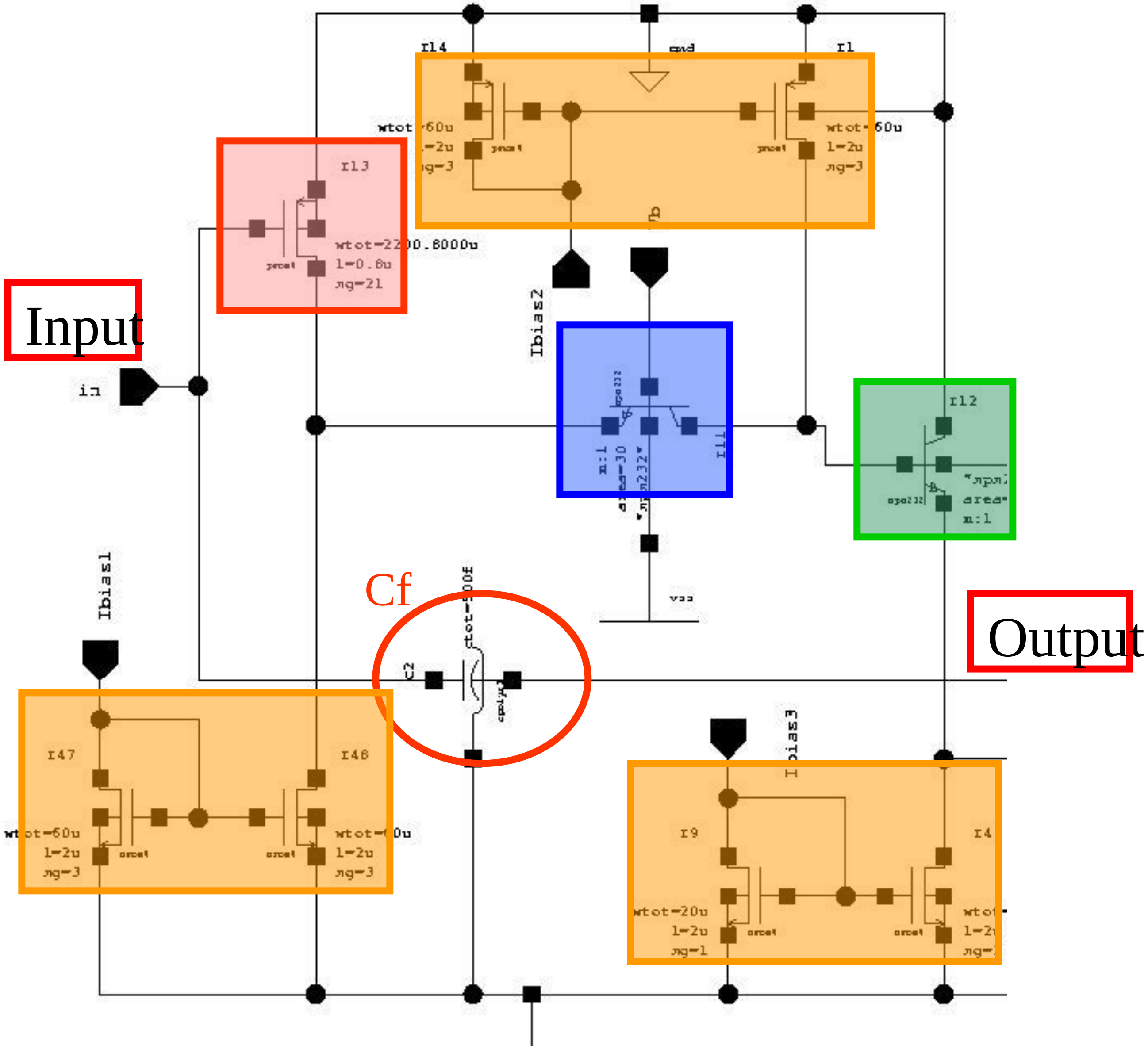


- **Gain (open loop) :**

$$v_{out}/v_{in} = - g_{m1} R_0 /(1 + j\omega \ R_0 C_0)$$

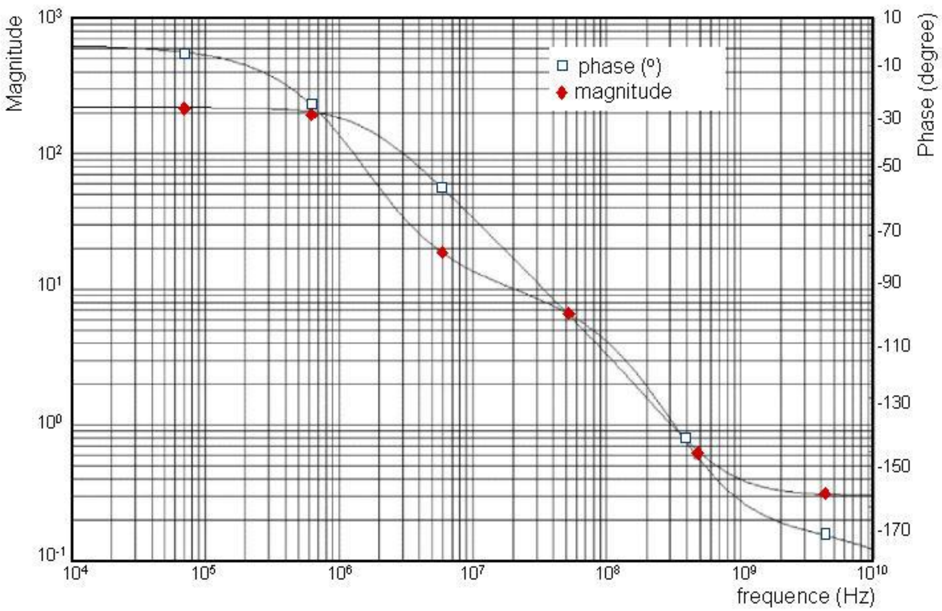
- *Ex : g_{m1}=20mA/V , R_0=500kΩ, C_0=1pF => $G_0=10^4$ $\omega_0=2 10^6$ $G_0\omega_0=2\ 10^{10}$ = 3 GHz !*

- Complete schematic
  - Adding bias elements

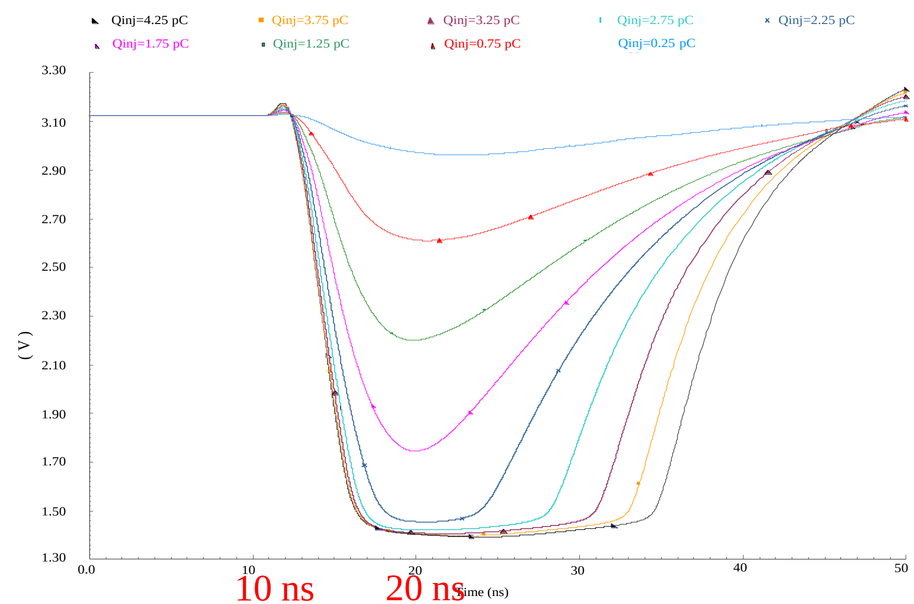


Example : designing a charge preamp (5)

- Complete simulation
  - Checking hand calculations against 2nd order effects
  - Testing extreme process parameters (« corner simulations »)
  - Testing robustness (to power supplies, temperature…)



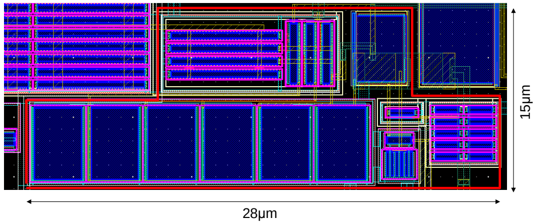
Simulated open loop gain



Saturation behaviour

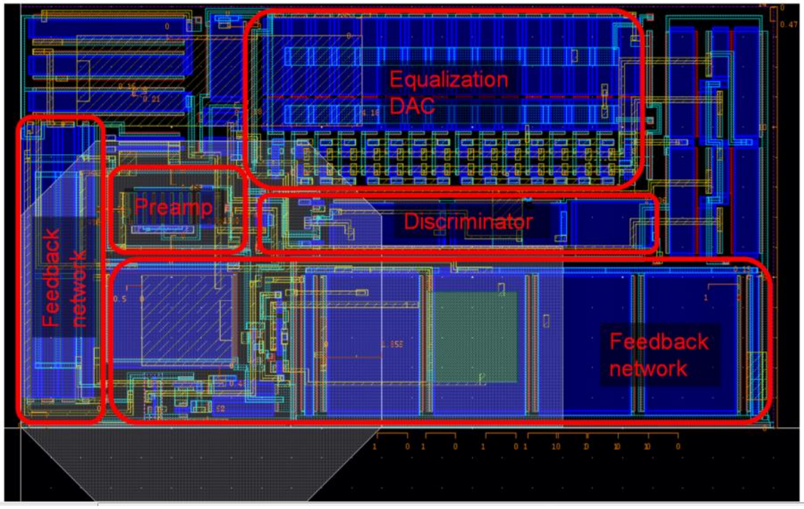
Example : designing a charge preamp (6)

- Layout
  - Each component is drawn
  - They are interconnected by metal layers



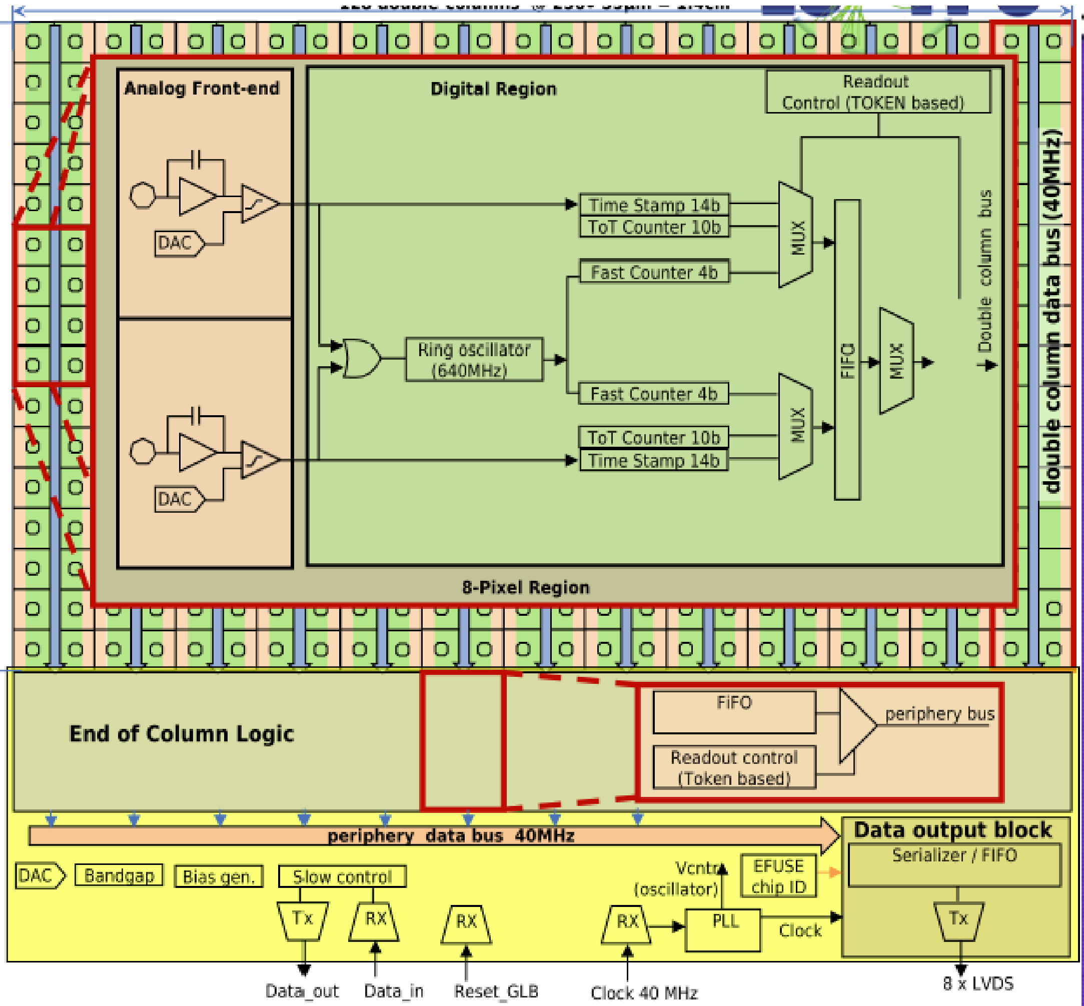
Charge preamp in 65nm
Clicpix P. Valerio (CERN 2013)

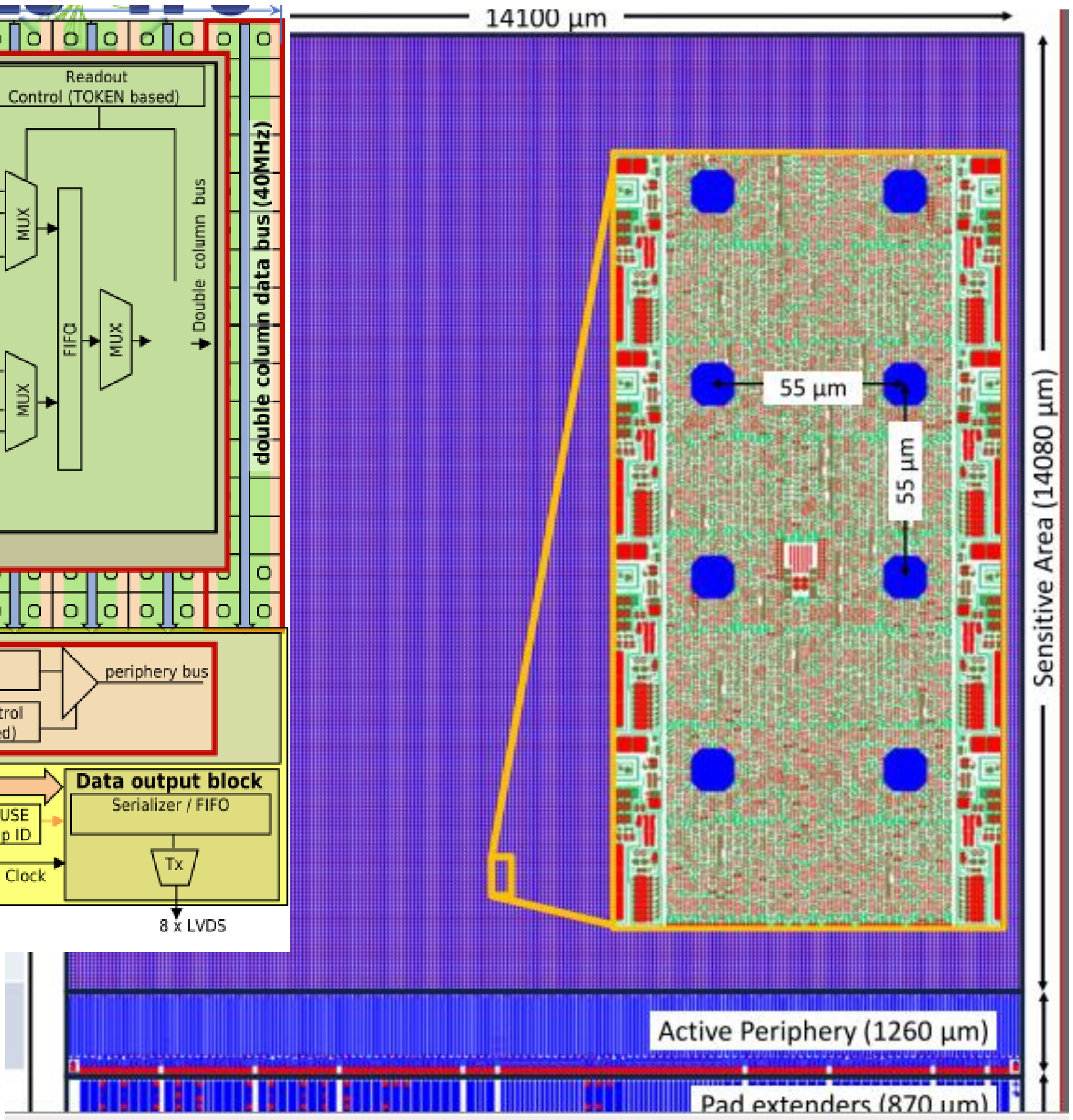
- Checks
  - DRC : checking drawing rules (isolation, minimal dimensions…)
  - ERC : extracting the corresponding electrical schematic
  - LVS (layout vs schematic) : comparing extracted schematic and original design
  - Simulating extracted schematic with parasitic elements



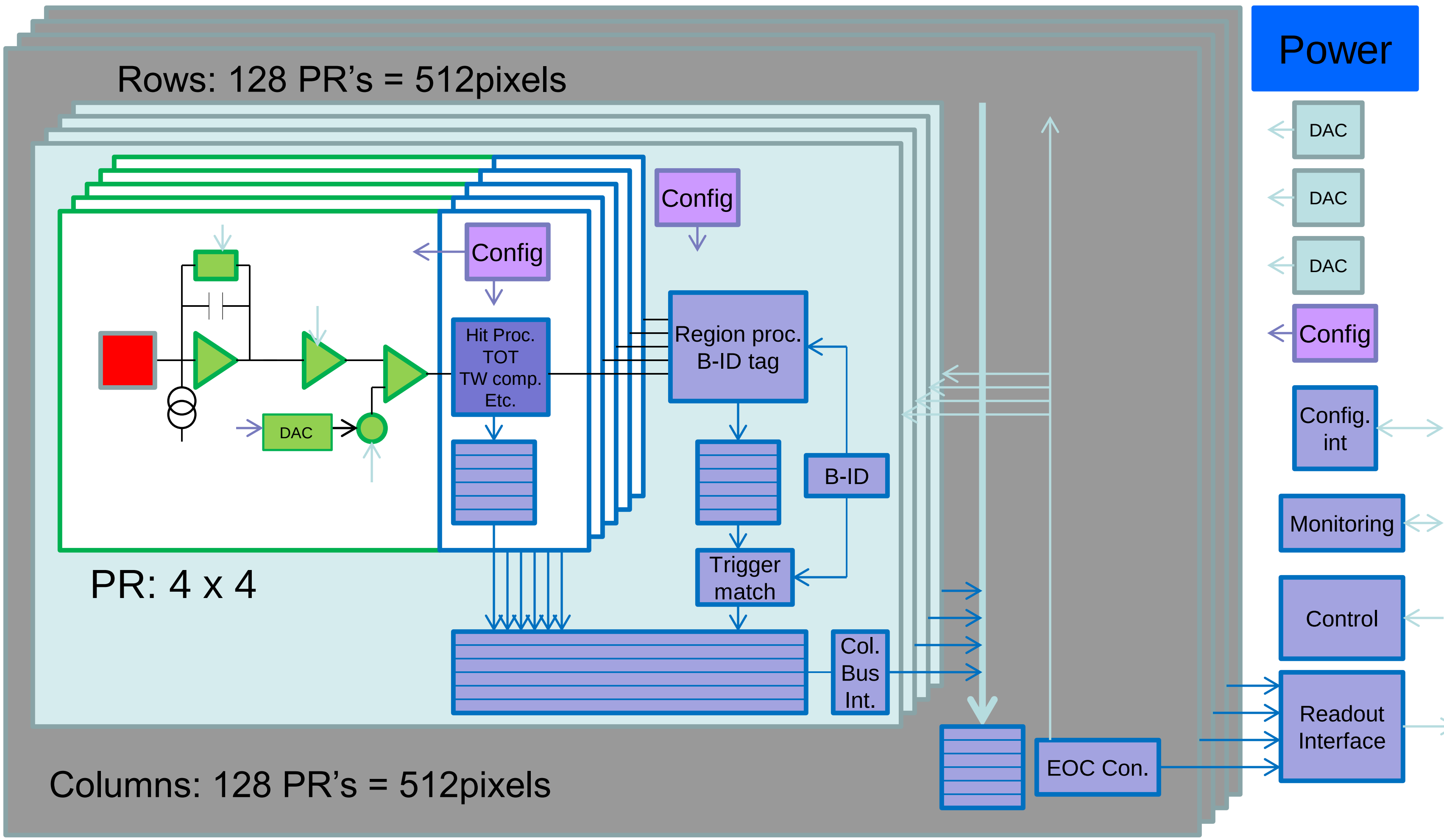
- Generating GDS2 file
  - Fabrication masks : « reticule »

From preamp to chip : Timepix 3 [CERN]…





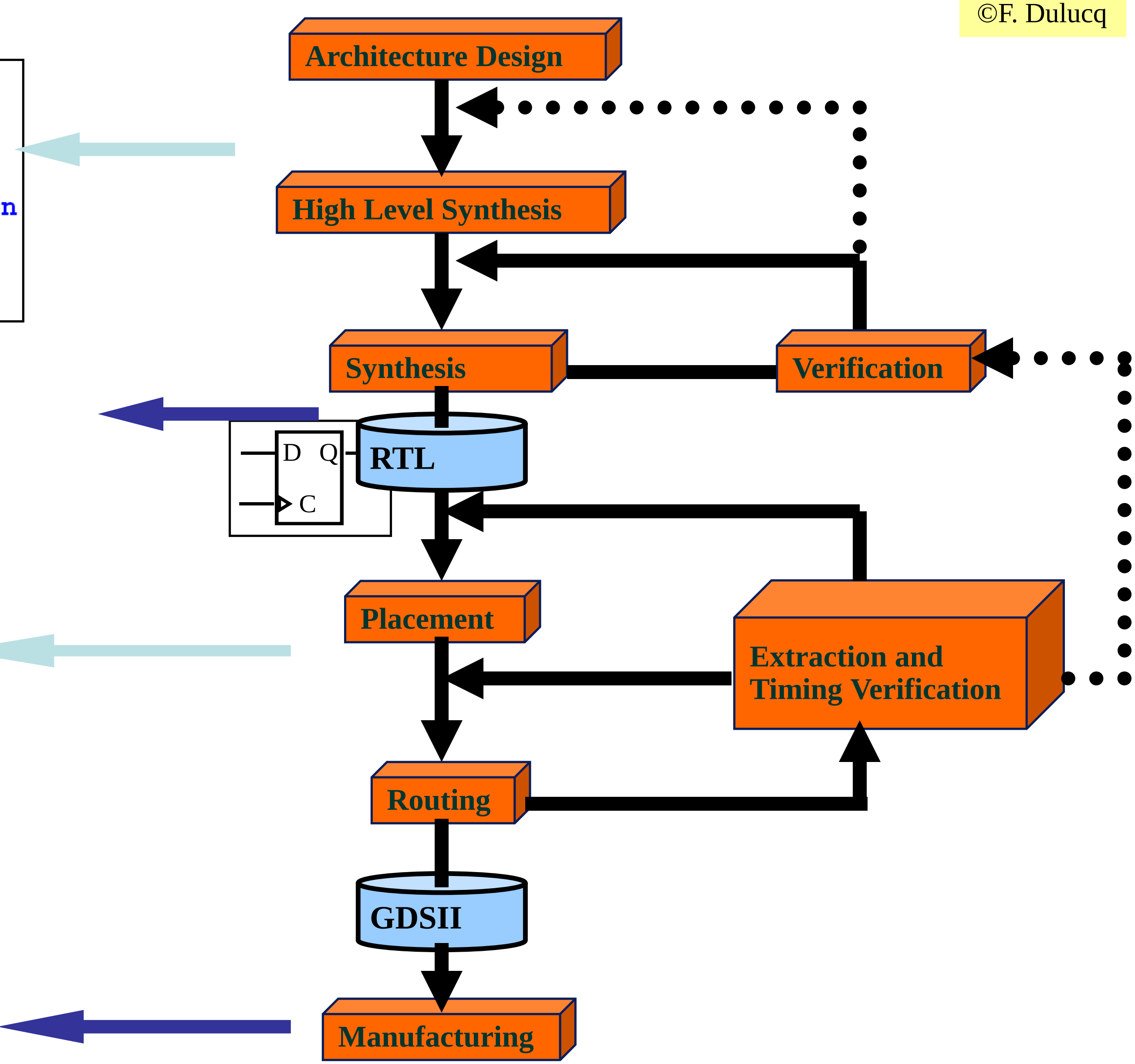
General pixel chip architecture

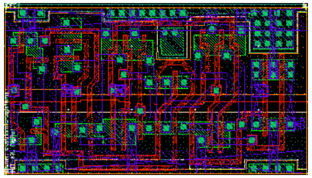


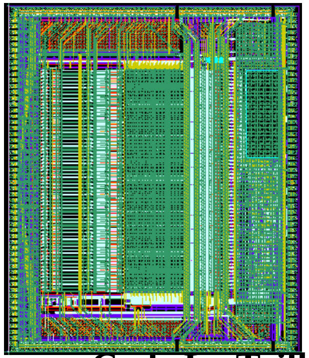
- Pixels: 4 x 4 x ~128 x ~128 = ~256k (262144)
- Chip size = ~50um x 4 x 128 = ~2.6cm x ~3cm (Yield maximization required)
- Obviously resembles LHCb/ALICE, FEI4, LHCb Velopix and other high rate pixels
  - And any other data driven (HEP) chip/system: System on a chip

Digital implementation global Flow


```
process(Rstb, Clk)
begin
   if Rstb ='0' then
     Q <= '0';
   elsif rising_edge Clk then
     Q <= D;
   end if;
end process;
```





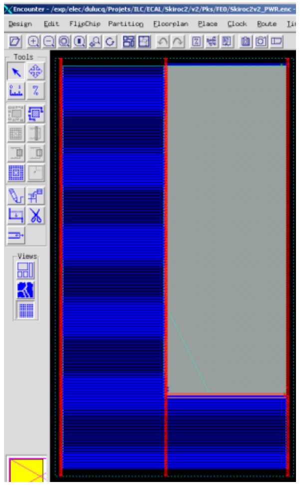


ASIC specific flow for digital routing

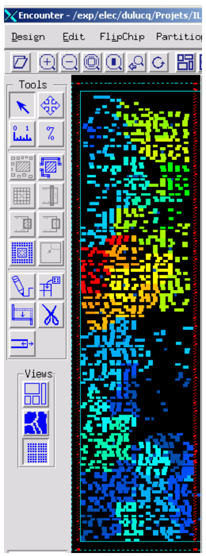
Ωmega

©F. Dulucq

Skiroc2 power planning



Skiroc2 clock tree



IO Pad Placement

Power planning (Stripes & rings)

Global Placement

DFT (scan chains)

Clock Tree Synthesis

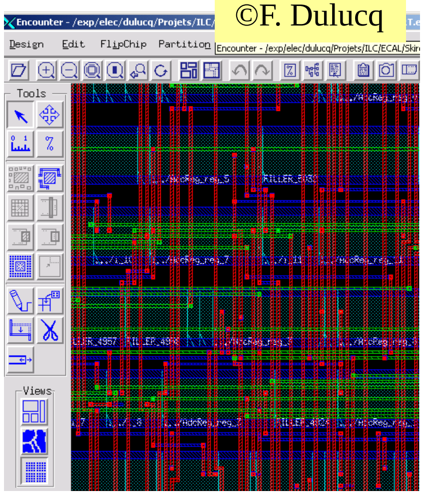
Global Routing

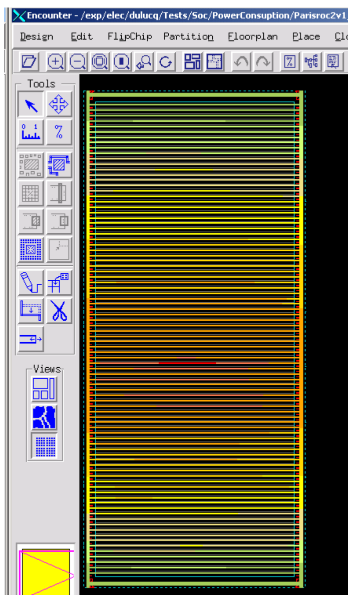
LVS / DRC
Specific Analysis (IR, Antennas)

GDS2

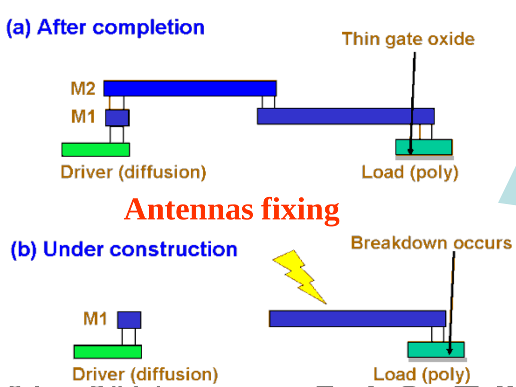
Extraction and Delay Calc. Timing Verification

(M1, M2, M3) = (blue, red, green)





Parisroc2 IR drop Analysis (red = drop > 5mV)



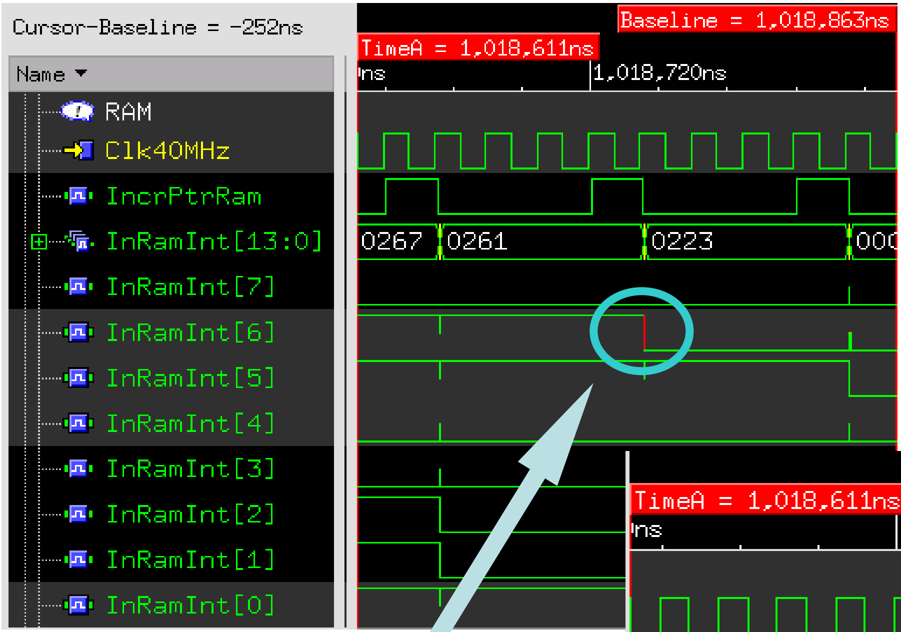
Antennas fixing

Pentium4

Post layout simulation (extracted RC)

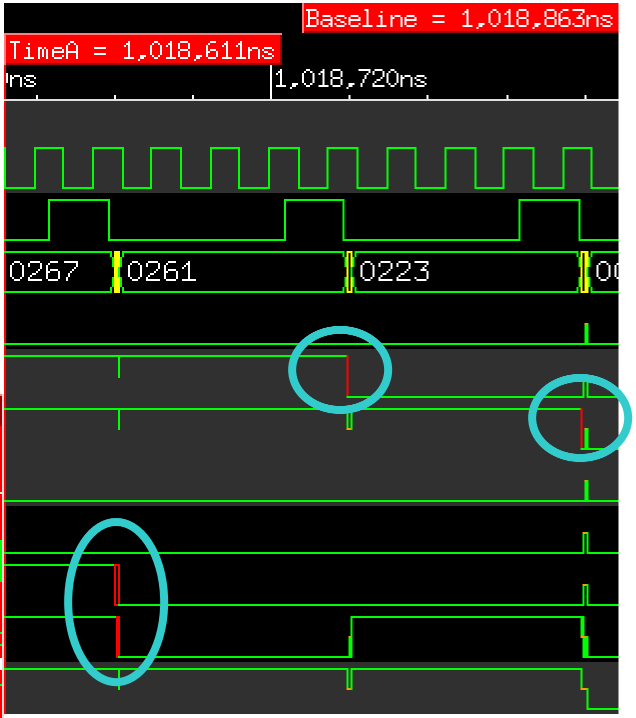
©F. Dulucq

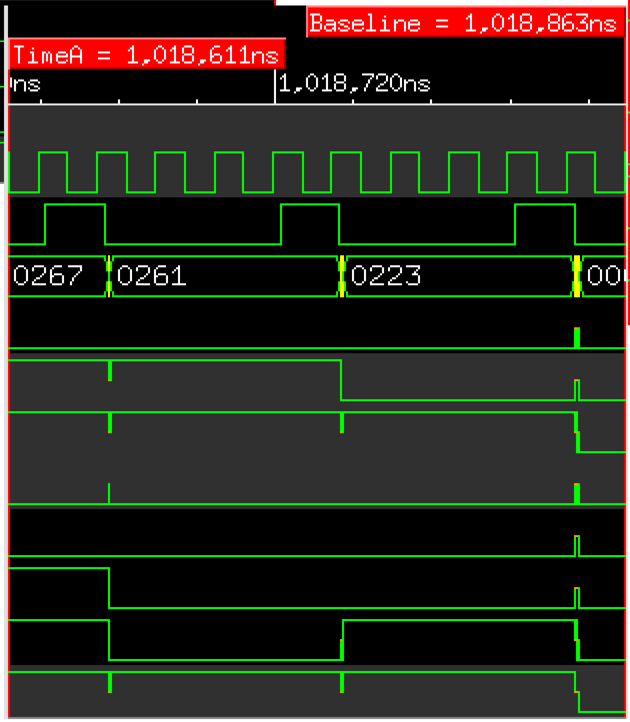
MIN PVT (1.6 ; 3.6V ; -50°C)



1 violations

MAX PVT (1.4 ; 3V ; 125°C)



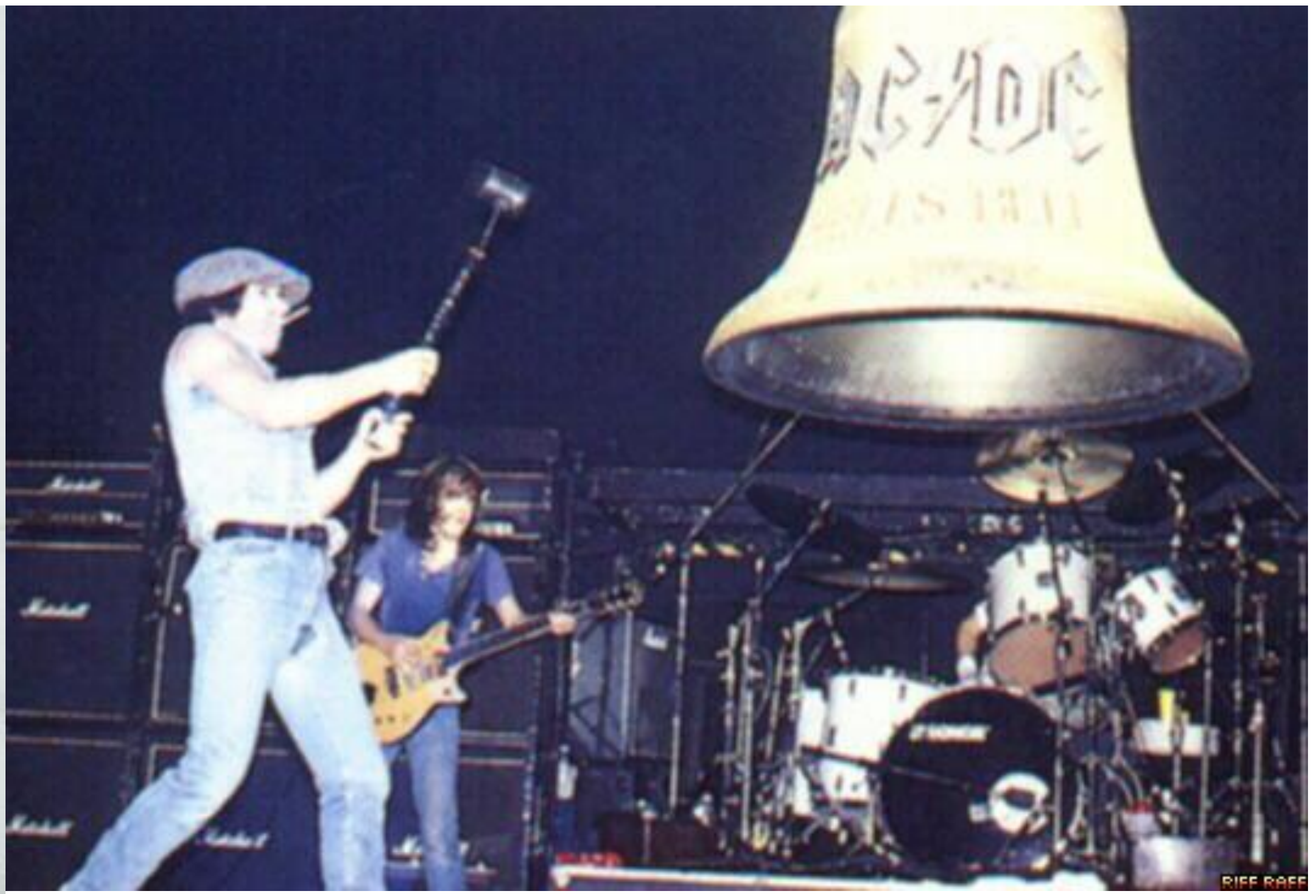


TYP PVT (1 ; 3.3V ; 25°C)

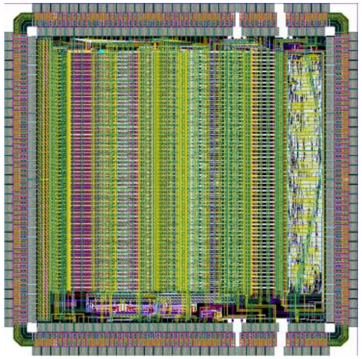
0 violations

4 violations

- Coexistence analog-digital
  - Capacitive, inductive and common-impedance couplings
  - A full lecture !
  - A good summary : there is no such thing as « ground », pay attention to current return

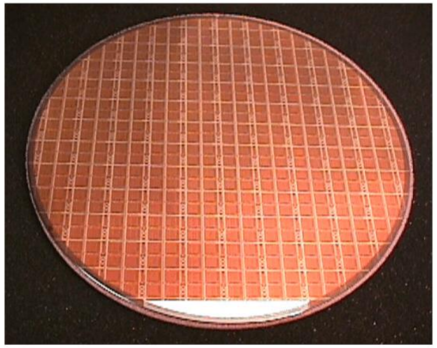


- ASICs : Application Specific Integrated Circuits
  - Access to foundries through multiproject runs (MPW)
  - Reduced development costs : 600-1000 €/mm^2 compared to dedicated runs (50-200 k€)
  - Full custom layout, at transistor level
  - mostly CMOS & BiCMOS



MAROC : 64ch MaPMT readout chip

- Very widespread in high Energy Physics
  - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
  - Better performance : reduction of parasitics
  - Better reliability (less connections)
  - But longer developpement time



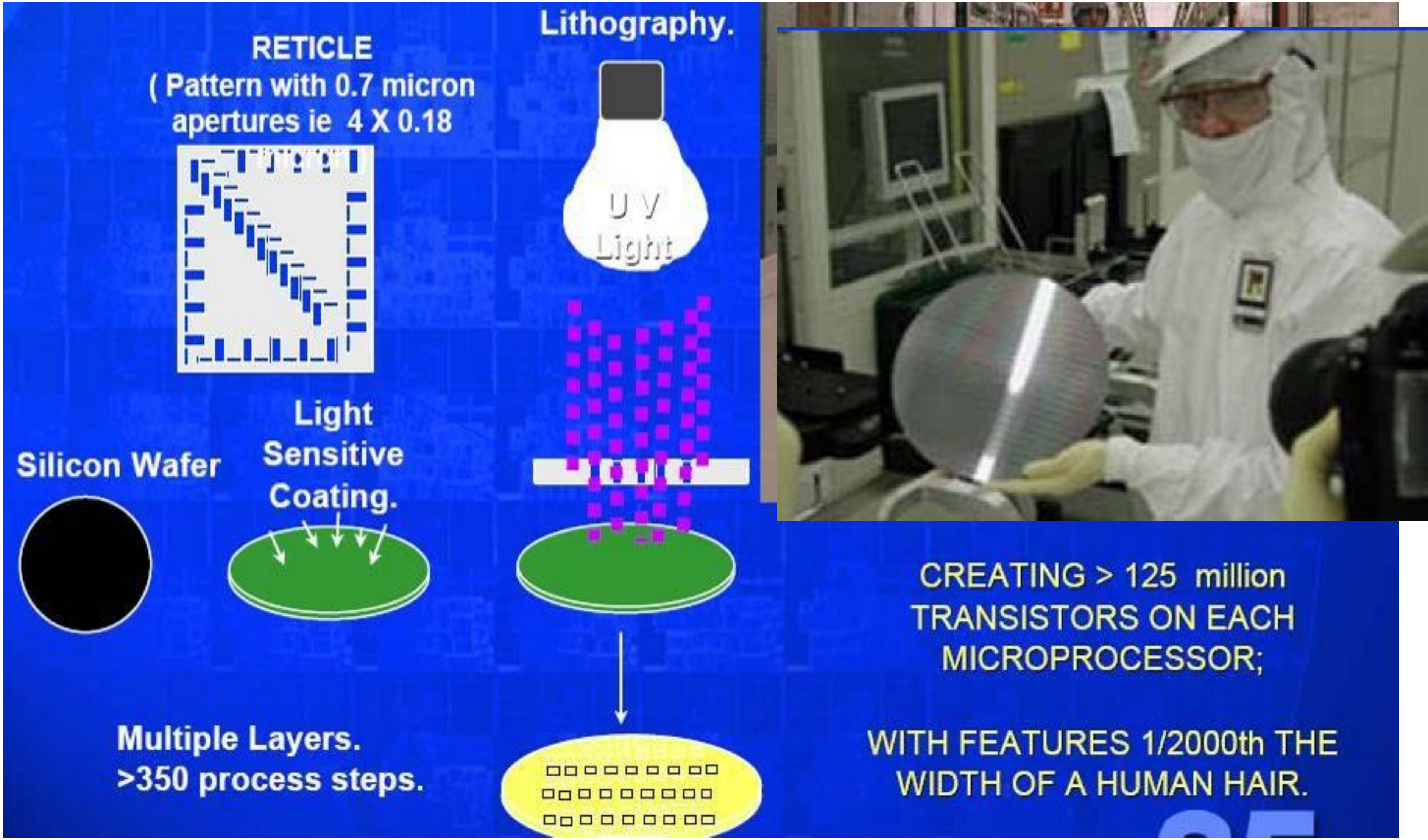
300 mm wafer

- Trends :
  - Evolution of technologies (see next slides)
  - Low power design

Processing of ASICs

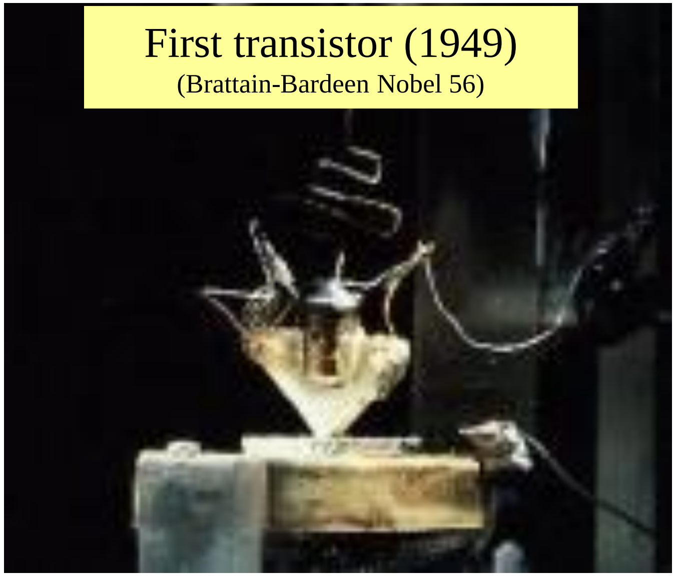
© Intel

- From Sand to ICs…

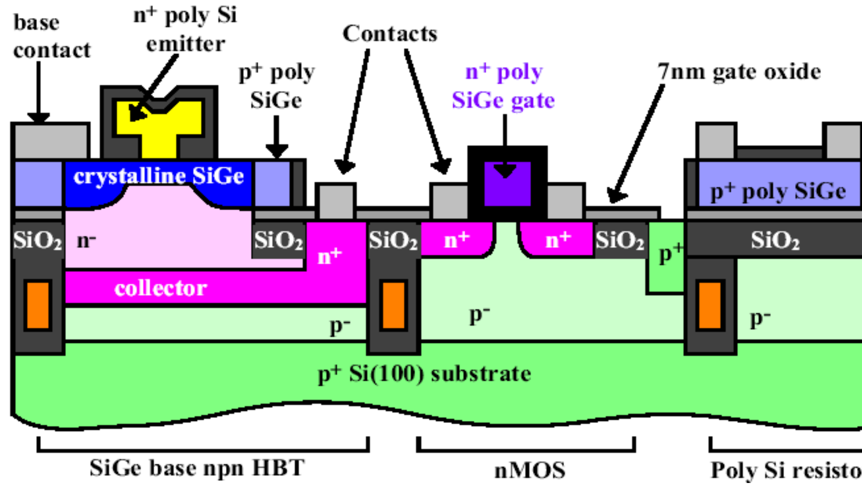


Evolution of technologies

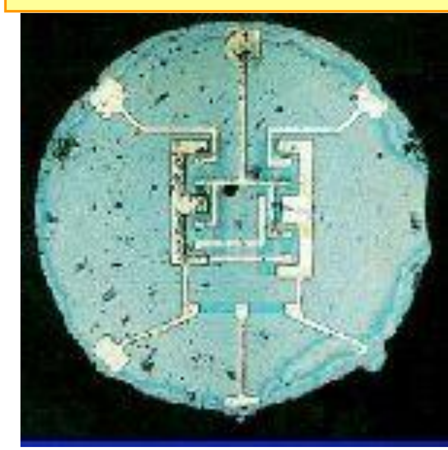
First transistor (1949)
(Brattain-Bardeen Nobel 56)



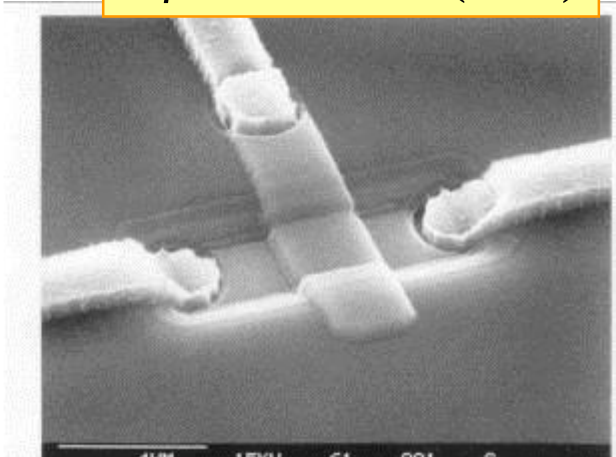
SiGe Bipolar in 0.35µm monolithic process



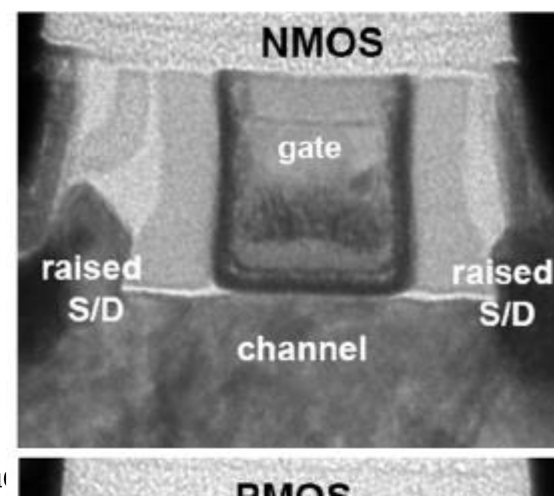
First planar IC (1961)



5 µm MOSFET (1985)



32 nm MOSFET (2010)

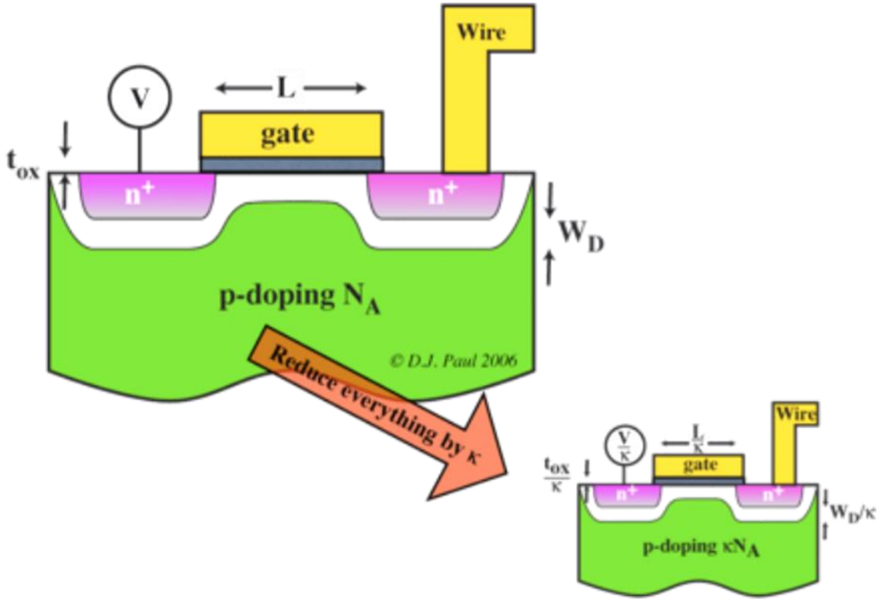


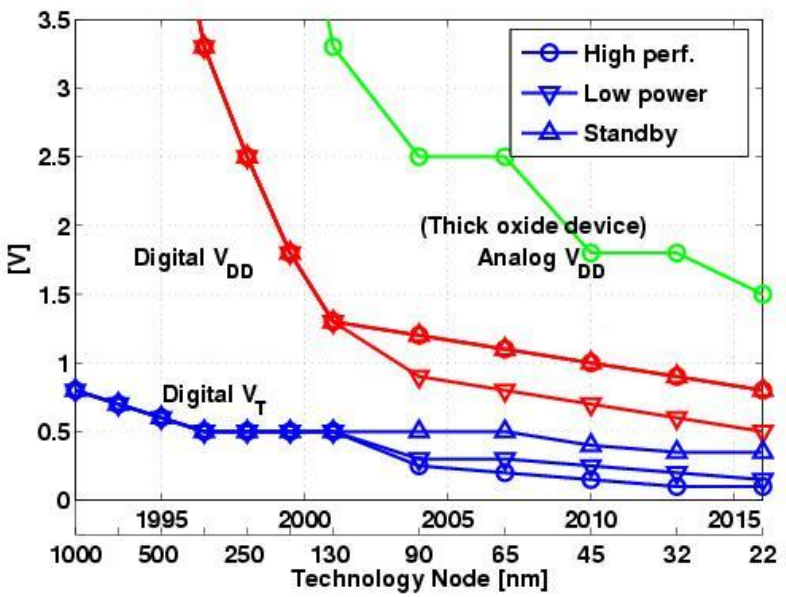
CMOS scaling

- Reduction of dimensions
  - « Quasi-constant voltage scaling »
  - Decrease of W,L,tox
  - (partial) decrease of V_{DD} et V_{Th}

- Improvement of speed as $1/L^2$
  - Improvement of transconductance as W/L and reduction of capacitance as WL

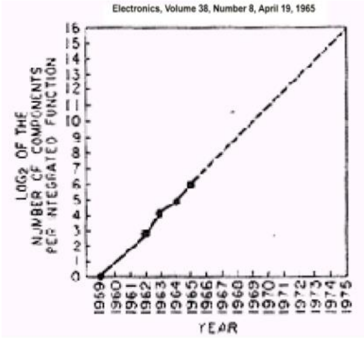
- Power increases as k and power density even worse
  - VDD does not scale as L

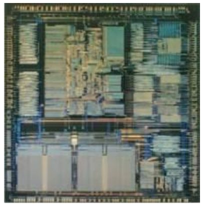


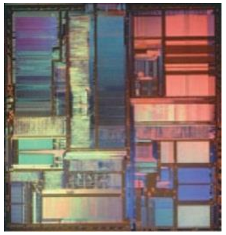


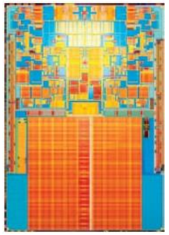
Evolution of CMOS technologies

- Moore's law : number of transistors doubling every ~2 years
- Technology nodes (gate length) *0.7 every 2 years



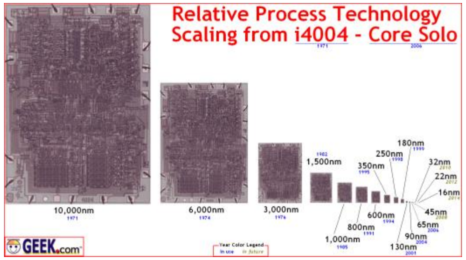




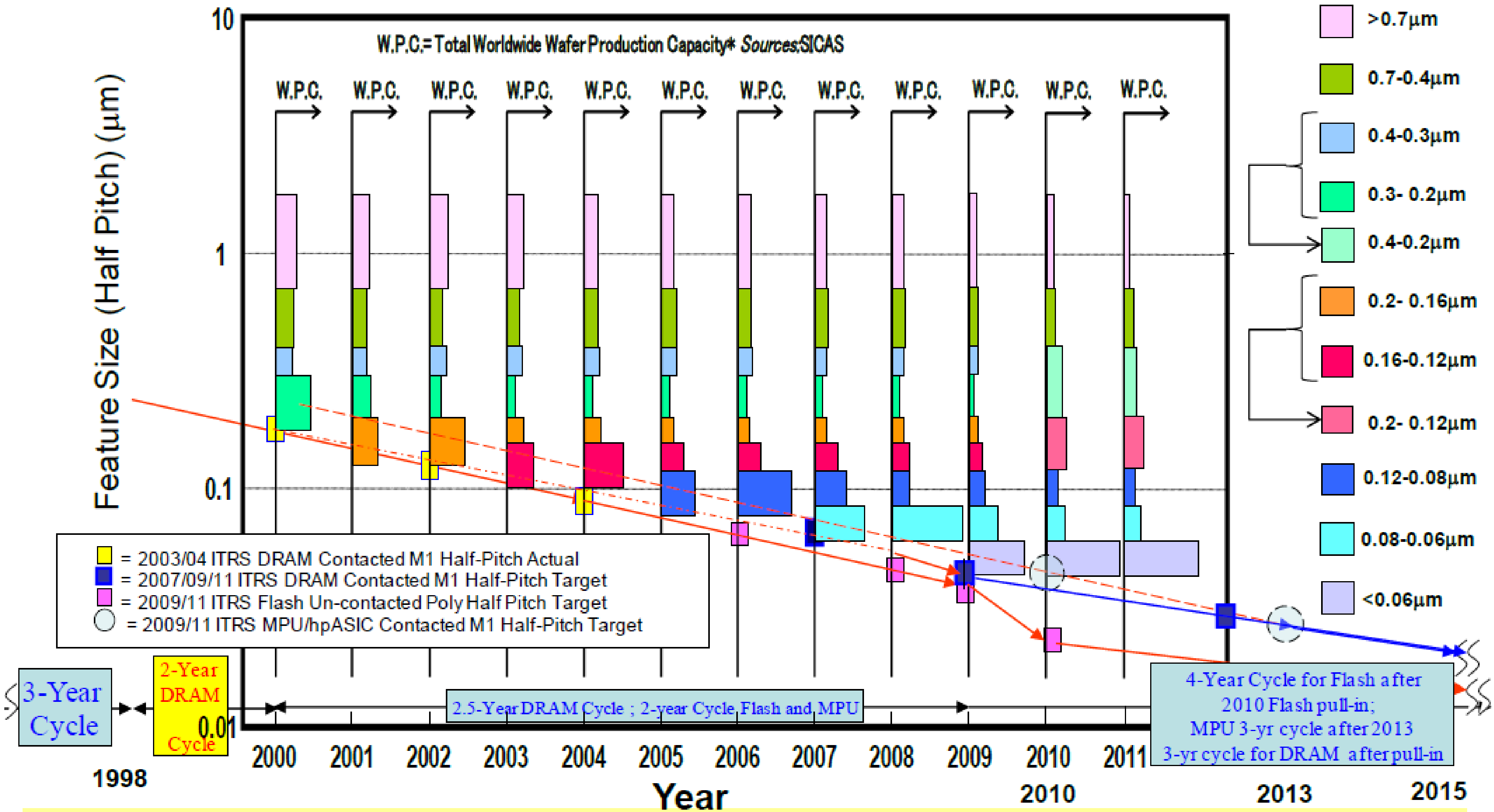


Processor	4004	8086	i386	Pentium	Pentium 4	Core2	3G Core7
Year	1971	1978	1985	1993	2000	2007	2012
Clock	108 kHz	10 MHz	16 MHz	66 MHz	1.5 GHz	2.4 GHz	2.9 GHz
Technology	10 µm	3 µm	1.5 µm	0.8 µm	0.18 µm	65 nm	22 nm
Nb transistors	2300	29000	275000	3.1M	42M	291M	1.4G

http://www.intel.com/content/www/us/en/history



ITRS 2011 roadmap



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 1Q data for 2011. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf

Ωmega

CMP
CNRS – INPG – UJF

Example of prices, prototyping

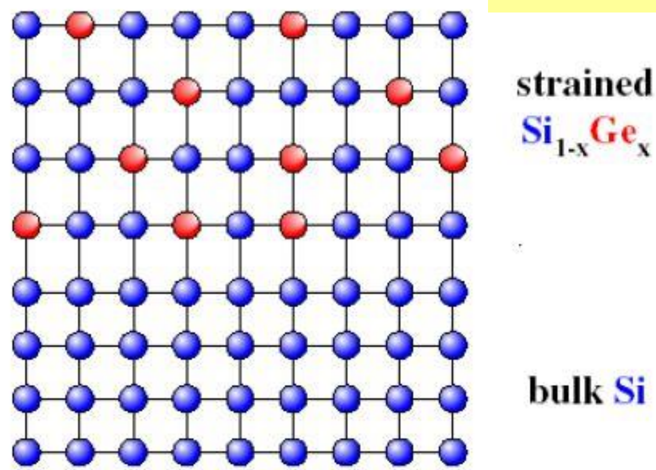
SSCS Chapitre Français
Section France

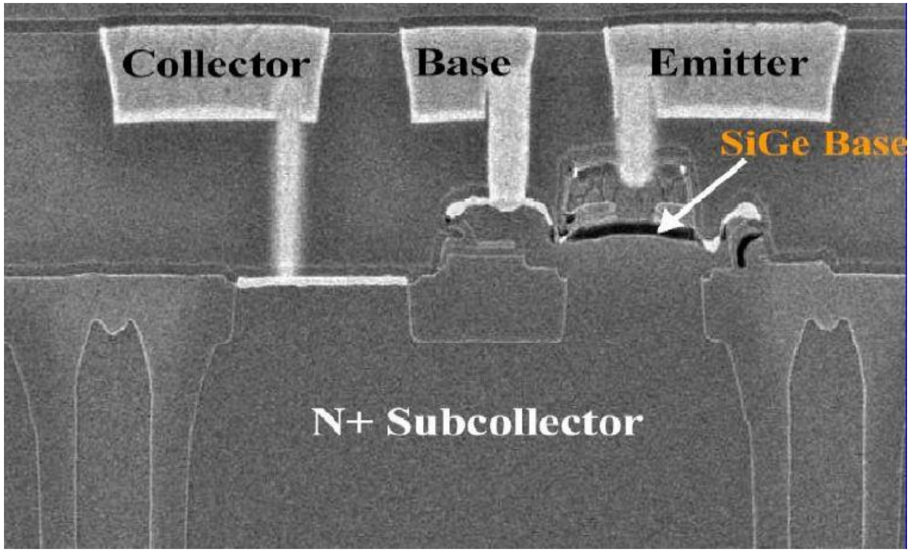
CMOS	.35 µ	AMS	650 €/mm²
CMOS opto	.35 µ	AMS	810 €/mm²
CMOS HV	.35 µ	AMS	1000 €/mm²
CMOS	130nm	ST	2200 €/mm²
CMOS	65 nm	ST	7500 €/mm²
CMOS	40 nm	ST	15000 €/mm²
SiGe BiCMOS	.35 µ	AMS	890 €/mm²
SiGe:C BiCMOS	130nm	ST	3500 €/mm²
SOI	130nm	ST	4000 €/mm²
SOI	65nm	ST	9500 €/mm²
Poly-SOI-Metal	MUMPS	MEMSCAP	3700 €/cm²

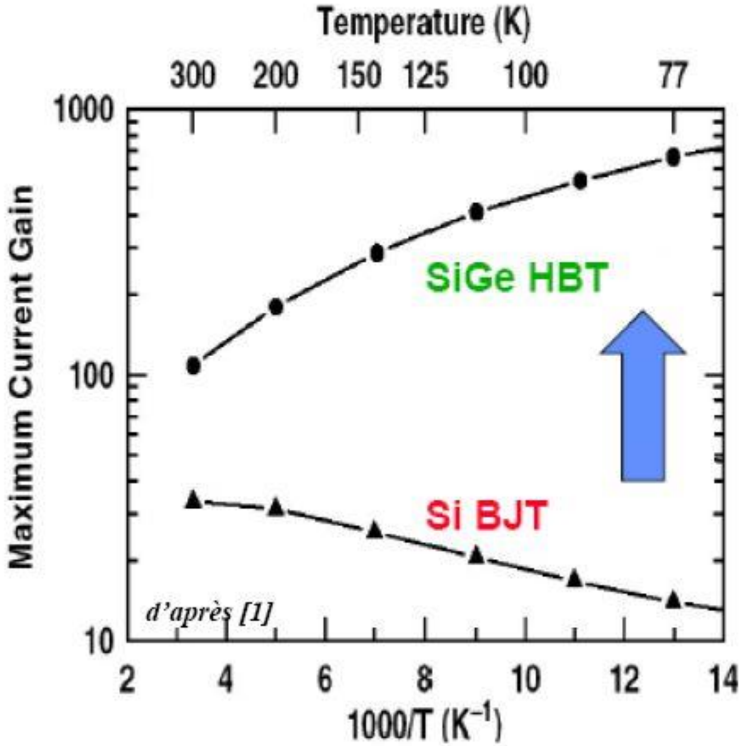
CMP annual users meeting, January 20th 2011, PARIS

http://cmp.imag.fr/aboutus/slides/Slides2011/02_Runs_2011.pdf

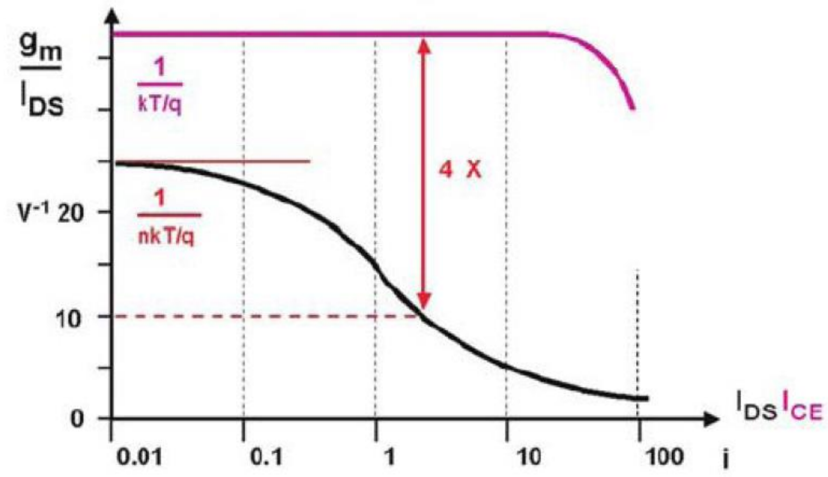
- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-s

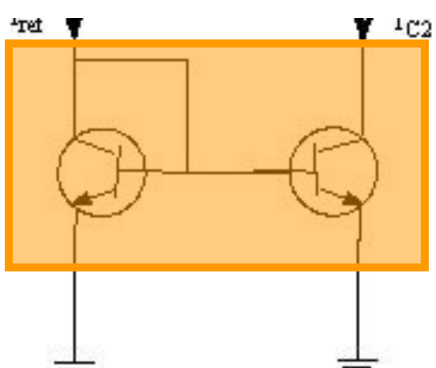


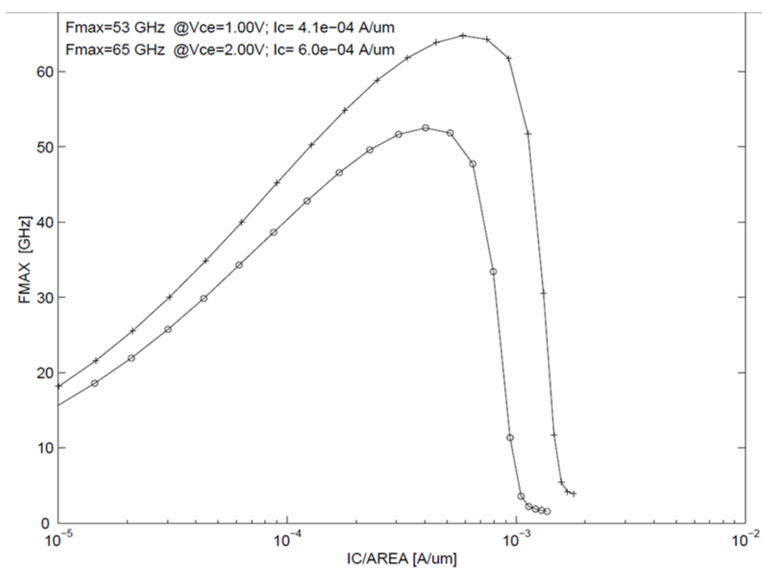


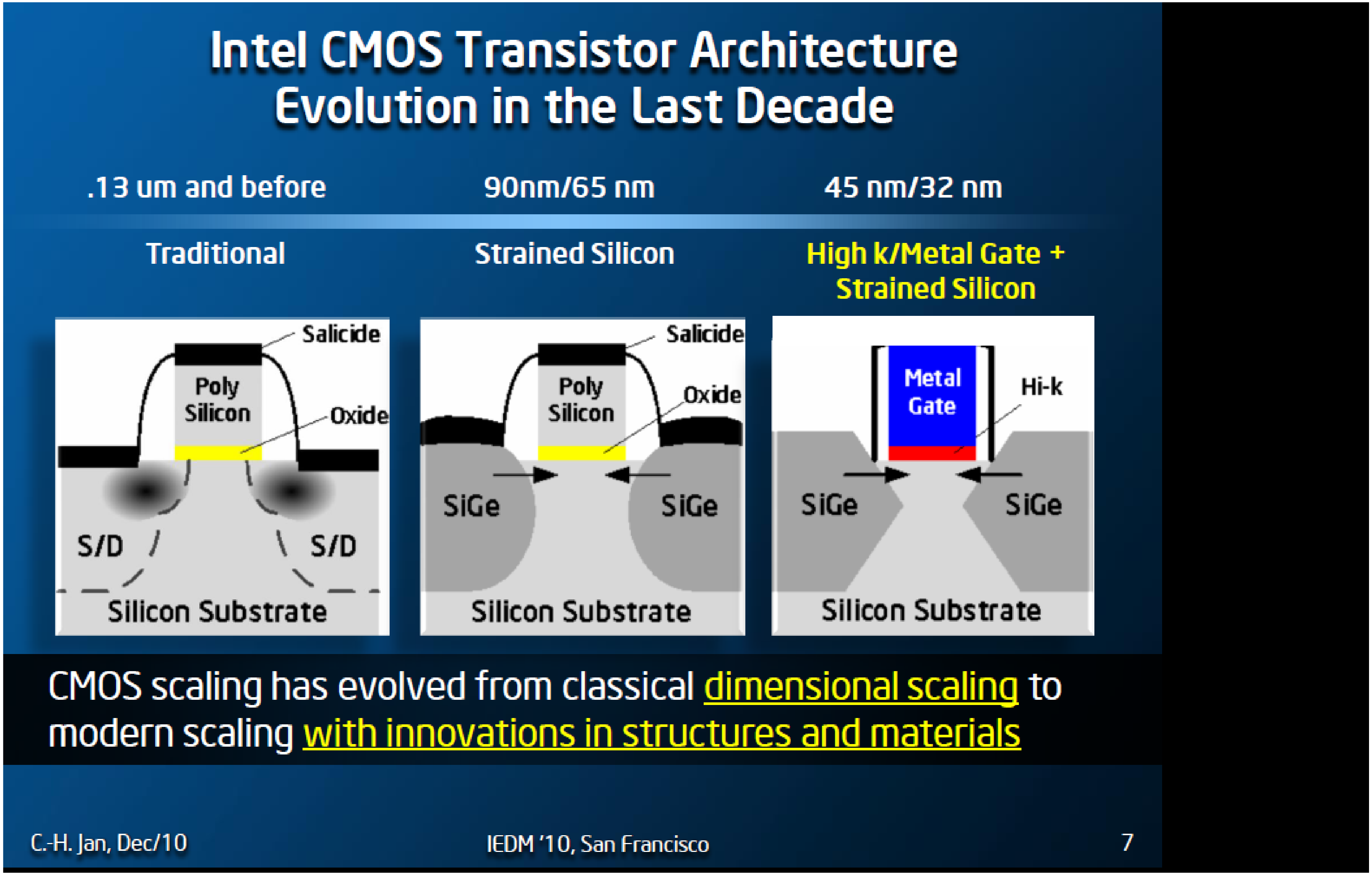


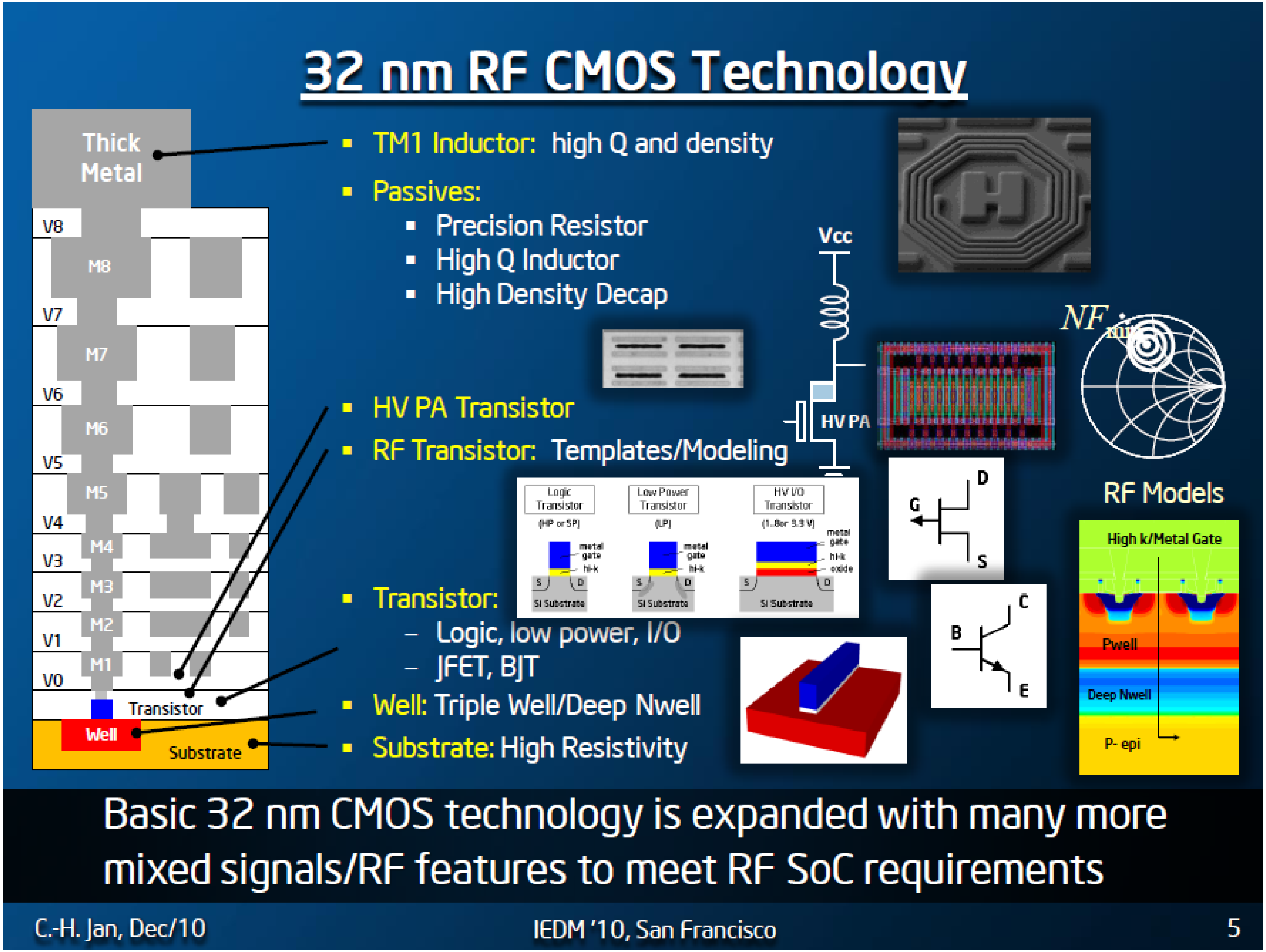
- BJT : best g_m /I ratio (1/U_T)
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance (A~mV*µm)
- $V_{BE}=V_T Ln(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T





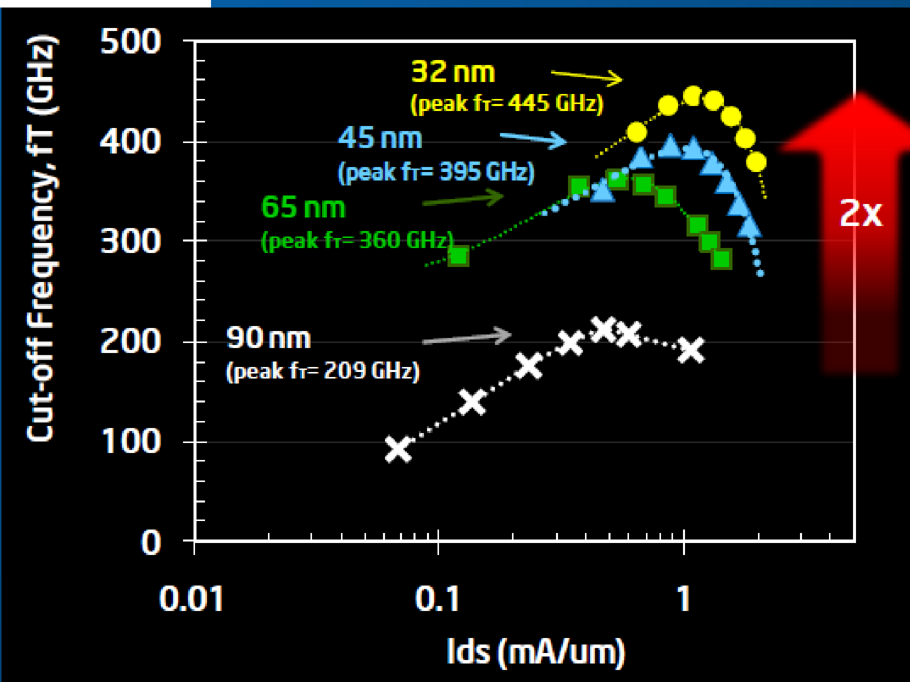



Intel CMOS Transistor Architecture
Evolution in the Last Decade
.13 um and before
90nm/65 nm
45 nm/32 nm
Traditional
Strained Silicon
High k/Metal Gate +
Strained Silicon
Salicide
Poly
Silicon
Oxide
S/D
S/D
Silicon Substrate
Salicide
Poly
Silicon
Oxide
SiGe
SiGe
Silicon Substrate
Metal
Gate
Hi-k
SiGe
SiGe
Silicon Substrate
CMOS scaling has evolved from classical dimensional scaling to modern scaling with innovations in structures and materials
C.-H. Jan, Dec/10
IEDM '10, San Francisco
7


32 nm RF CMOS Technology
Thick Metal
V8
M8
V7
M7
V6
M6
V5
M5
V4
M4
V3
M3
V2
M2
V1
M1
V0
Transistor
Well
Substrate
TM1 Inductor: high Q and density
Passives:
Precision Resistor
High Q Inductor
High Density Decap
HV PA Transistor
RF Transistor: Templates/Modeling
Transistor:
– Logic, low power, I/O
– JFET, BJT
Well: Triple Well/Deep Nwell
Substrate: High Resistivity
Vcc
HV PA
Logic Transistor
Low Power Transistor
HV I/O Transistor
metal gate
hi-k
oxide
Si Substrate
G
D
S
B
C
E
RF Models
High k/Metal Gate
Pwell
Deep Nwell
P- epi
Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements
C.-H. Jan, Dec/10
IEDM '10, San Francisco
5

RF 32 nm CMOS

RF CMOS Technology Performance Metrics

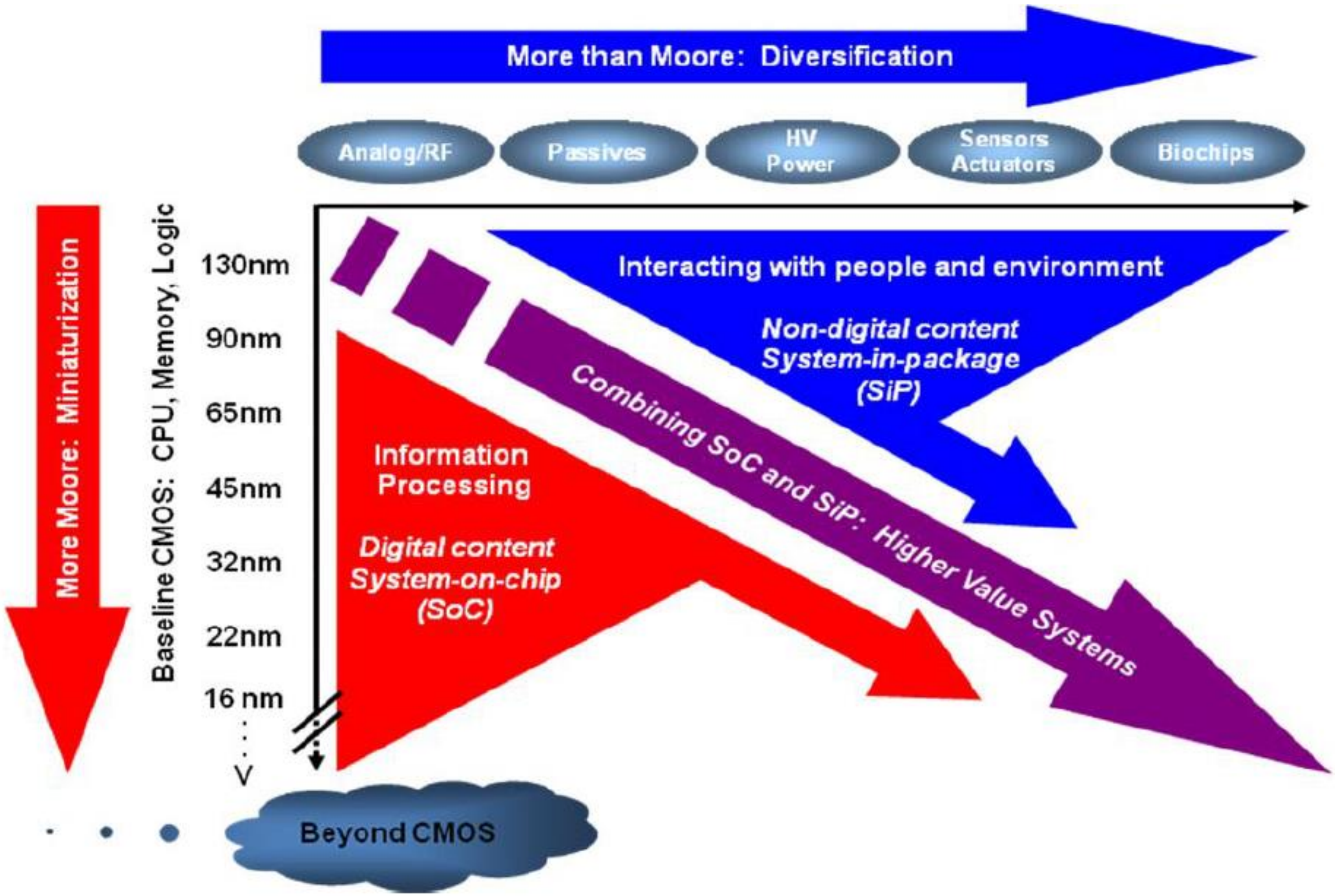


RF Devices	RF Circuits	Key Device Characteristics
Logic Transistor	MAC/BB, ADC, DAC	Idsat, Idlin, Vt, Ioff
Analog Transistor	ADC, DAC, MAC/BB	Gm, Rout, Matching, Linearity, Noise, NF_{min}
RF Transistor	PA, Mixer, T/R Switch	f_T, f_{max}, 1/f Noise, NF_{min}
PA Transistors	PA	Ron, Linearity, f_T, f_{MAX}, Efficiency, Breakdwn V,
Precision Resistors	ADC, DAC, BB Filter, others	R, σR/R, Matching
Linear Capacitors	PLL, VCO	C, Q, Matching
Varactors	PLL, VCO	Tuning Ratio, Q, Kv_{CO},
Inductor/ Transformer/Balun	PA, LNA, Mixer	L, Q

What are the impacts of CMOS scaling on these metrics ?

C.-H. Jan, Dec/10 IEDM '10, San Francisco 11

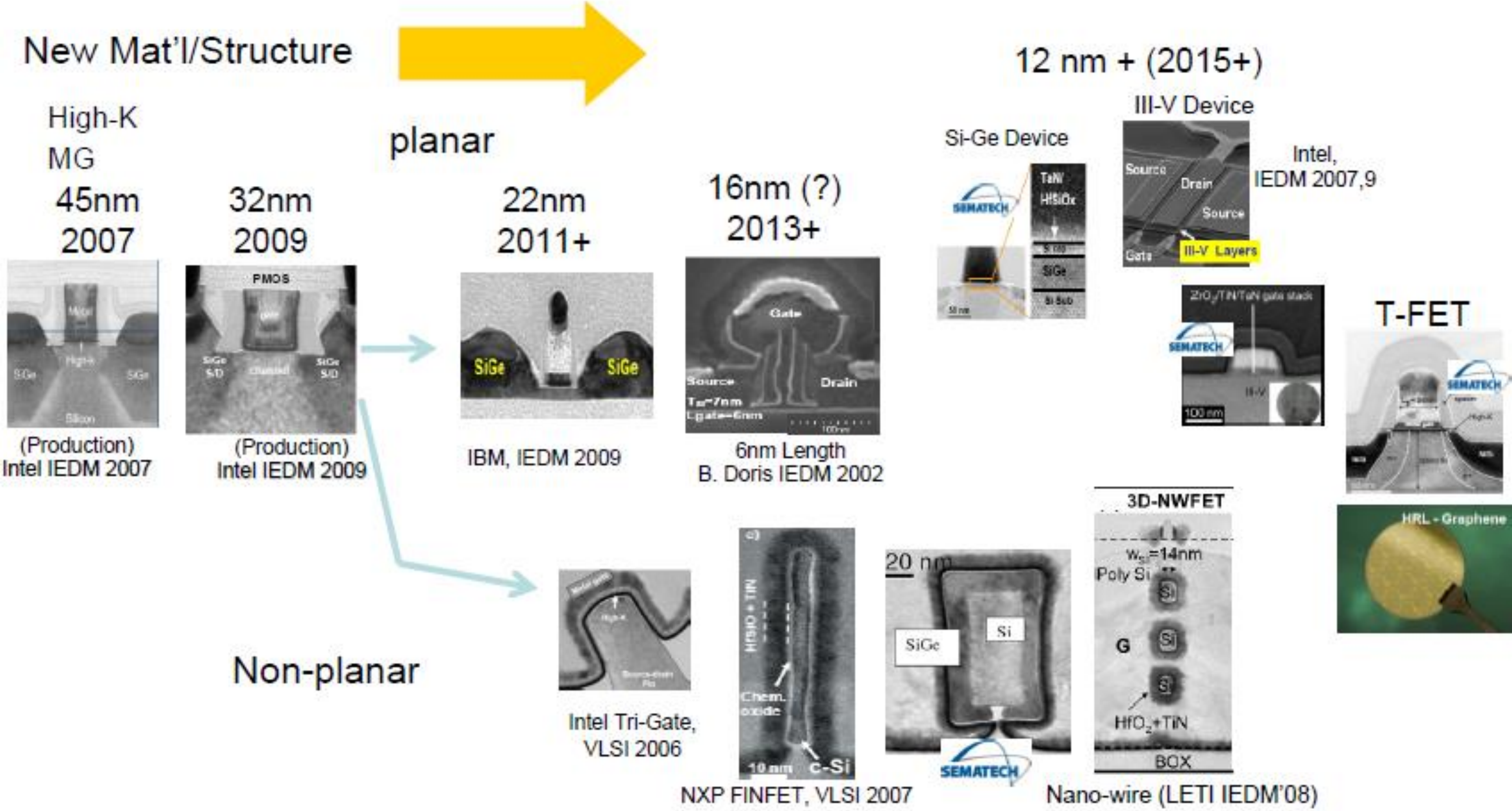
« Moore » and « More than Moore »



Generic MOSFET scaling trends

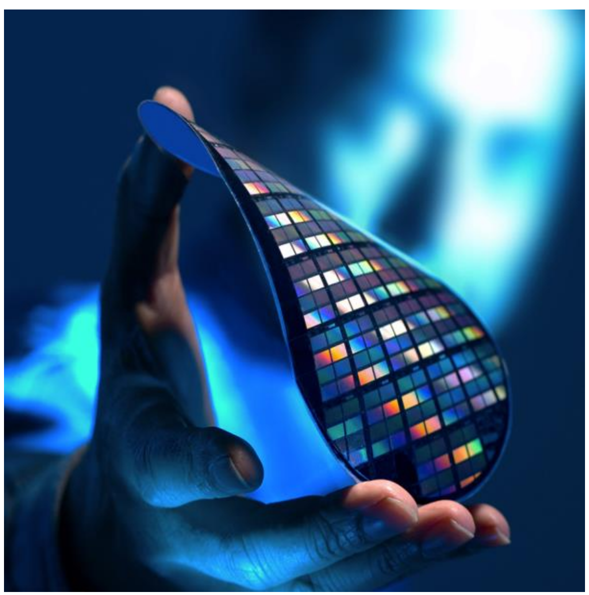
Novel materials and architectures

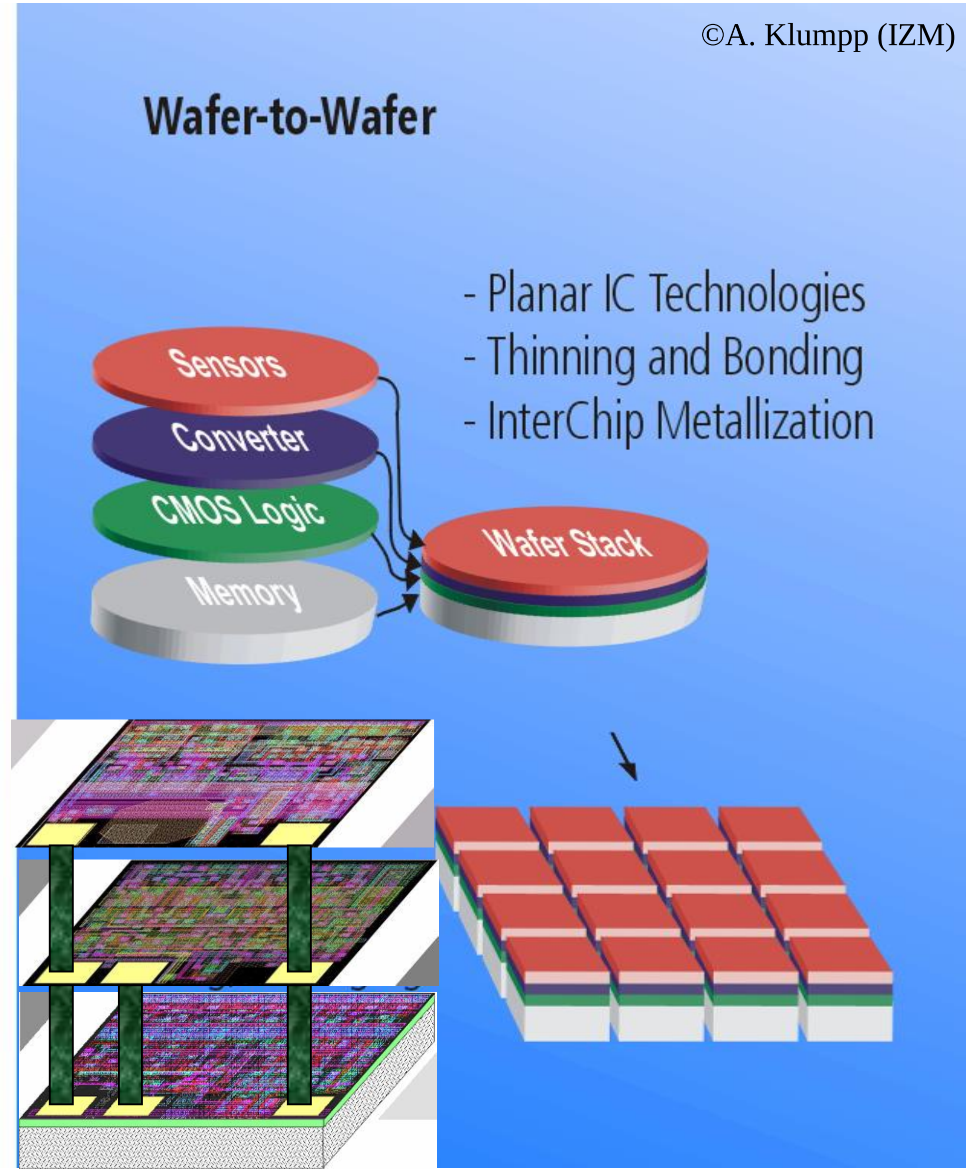
http://www.sematech.org/meetings/archives/symposia/9027/pres/Session%202/Jammy_Raj.pdf



3D technology

- Increasing integration density, mixing technologies
- Wafer thinning to <50 µm
- Minimization of interconnects
- Large industrial market
  - Processors, image sensors…

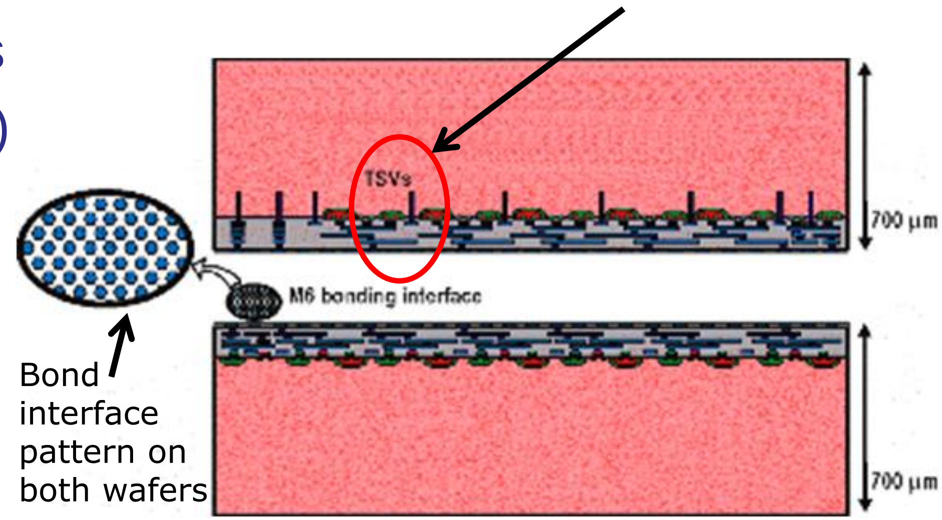




3D technology in HEP

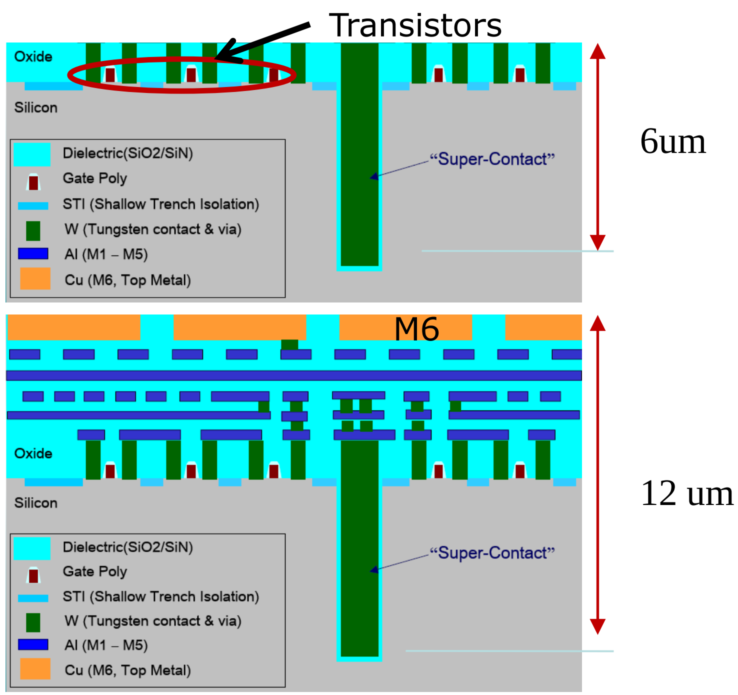
© R. Yarema (FNAL)

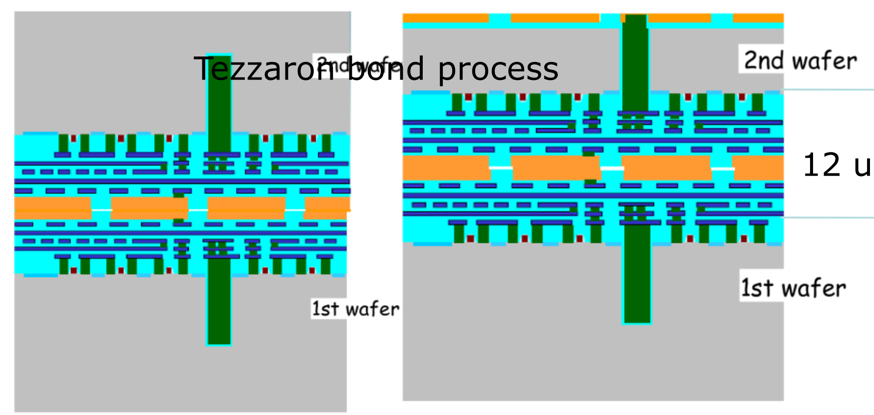
- Access to 3D via Tezzaron
  - 130 nm Global foundry wafers
  - 1µm vias (Via middle process)
  - Cu-Cu bonding face to face



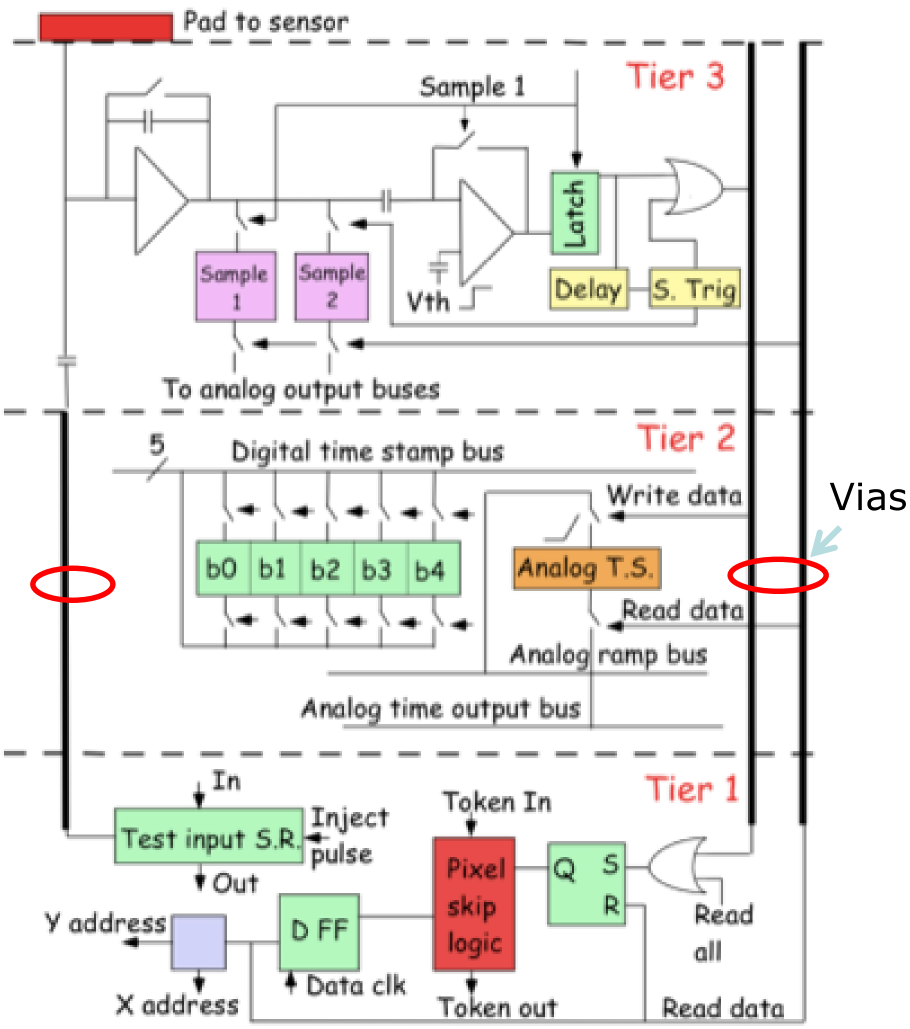
After FEOL fabricate 6 um super contact (via)

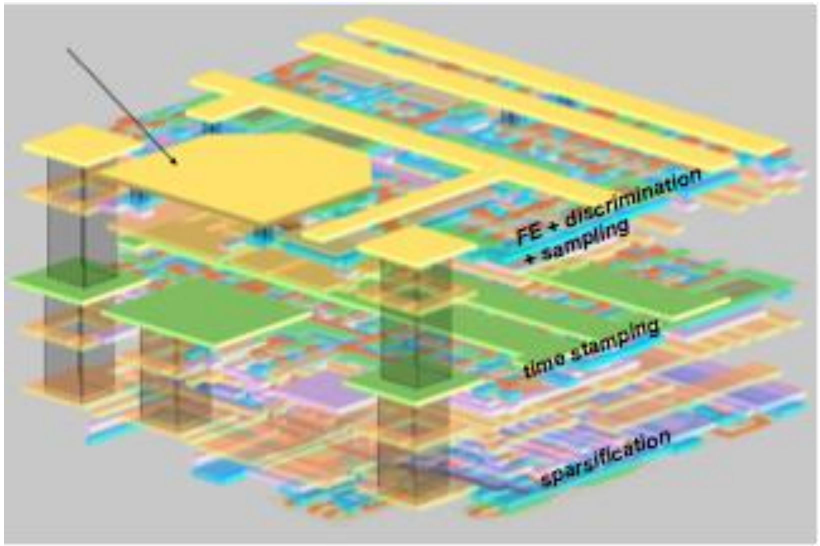
Complete BEOL processing



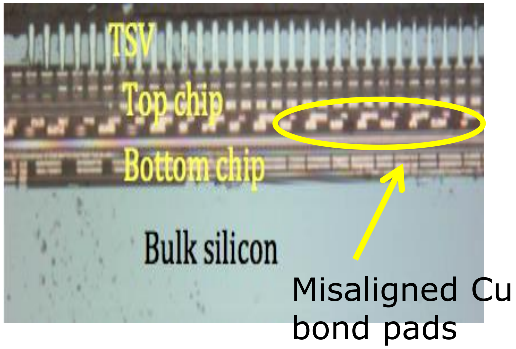


Exampe of realization at FNAL





V1P1 3D chip by FNAL



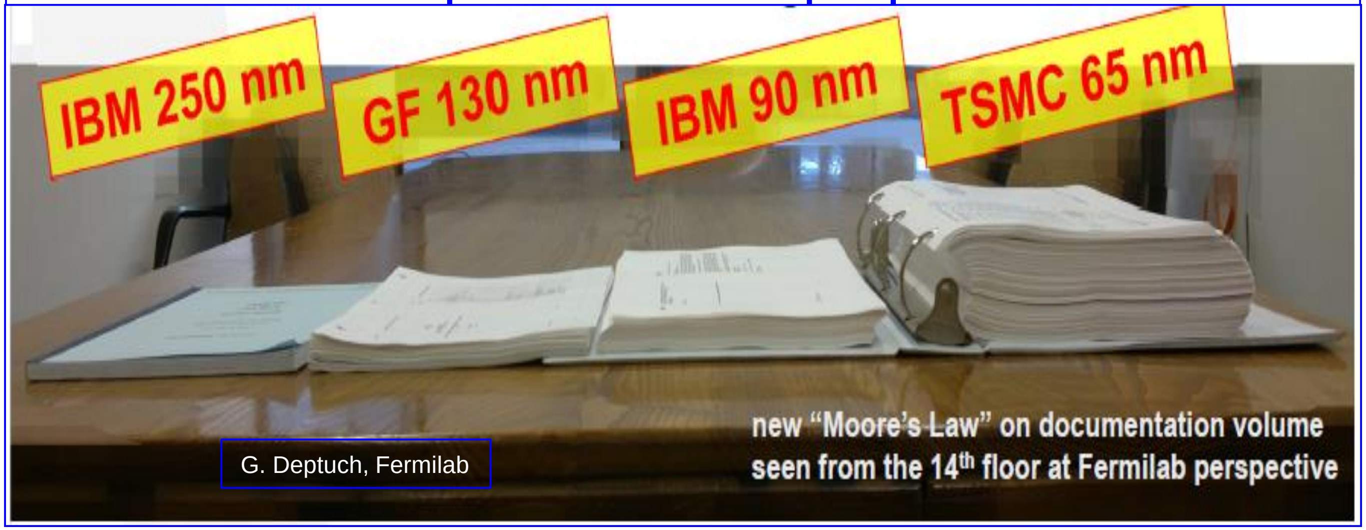
Medipix related hybrid pixel readout chips

Medipix1 (1998)	*1μm SACMOS, 64x64 pixels, 170x170μm^2* *PC / Frame based readout*
Medipix2 (2001)	*0.25μm CMOS, 256x256 pixels, 55x55μm^2* *PC / Frame based readout*
Timepix (2006)	*0.25μm CMOS, 256x256 pixels, 55x55μm^2* *PC, ToT, ToA / Frame based readout*
Medipix3 (2009)	*0.13μm CMOS, 256x256 pixels, 55x55μm^2* *PC / Frame based readout* *Event by event charge reconstruction and allocation*
Dosepix (2011)	*0.13μm CMOS, 16x16 pixels, 220x220μm^2* *ToT, PC / Rolling shutter (programmable column readout)* *Event by event binning of energy spectra (16 digital thrs)*
Timepix3 (2013)	*0.13μm CMOS, 256x256 pixels, 55x55μm^2* *PC; ToT, ToA (simultaneous)/ Data driven readout*
Velopix	*0.13μm CMOS, 256x256 pixels, 55x55μm^2,* *ToA, Binary/ToT (TBD), Data driven readout*
Smallpix	*0.13μm CMOS, 512x512 pixels, 40x40μm^2 (TBD), TSV compatible* *PC, iToT; ToA, ToT1 (simultaneous)/ Frame based (ZC)*
Clicpix prototype (2013)	*65nm CMOS, 64x64 pixels, 25x25μm^2* *ToA, ToT1 (simultaneous)/ Frame based (ZC)*

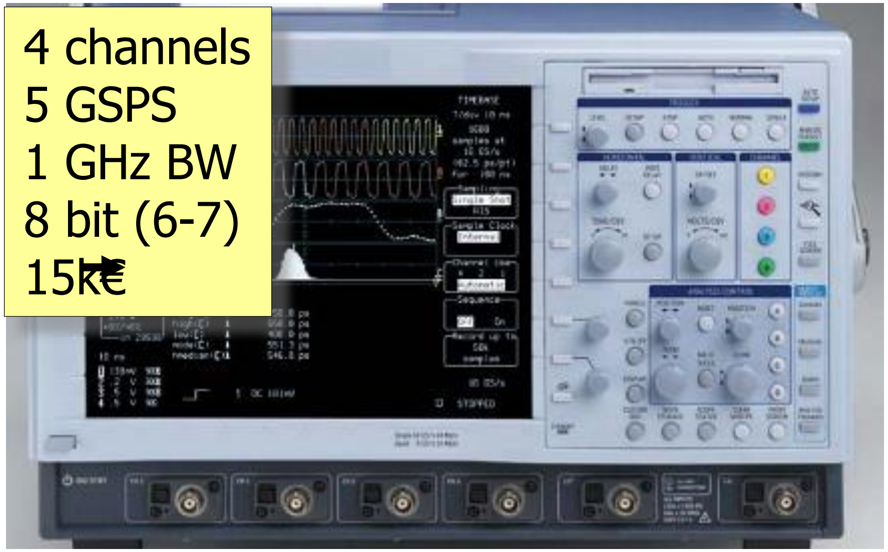
- More and more functions are integrated inside chips (ASICs)

- Evolution of technologies make them more and more performant but more and more complex

10 ans d'évolution des spécifications techniques pour la réalisation d' ASIC



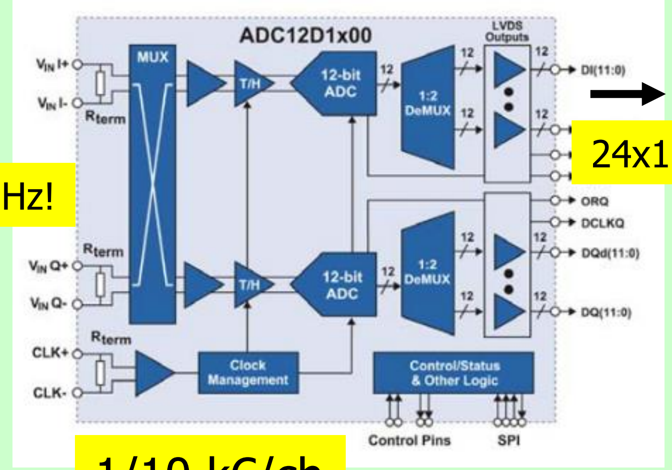
4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15k€



FADCs

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s

1.8 GHz!



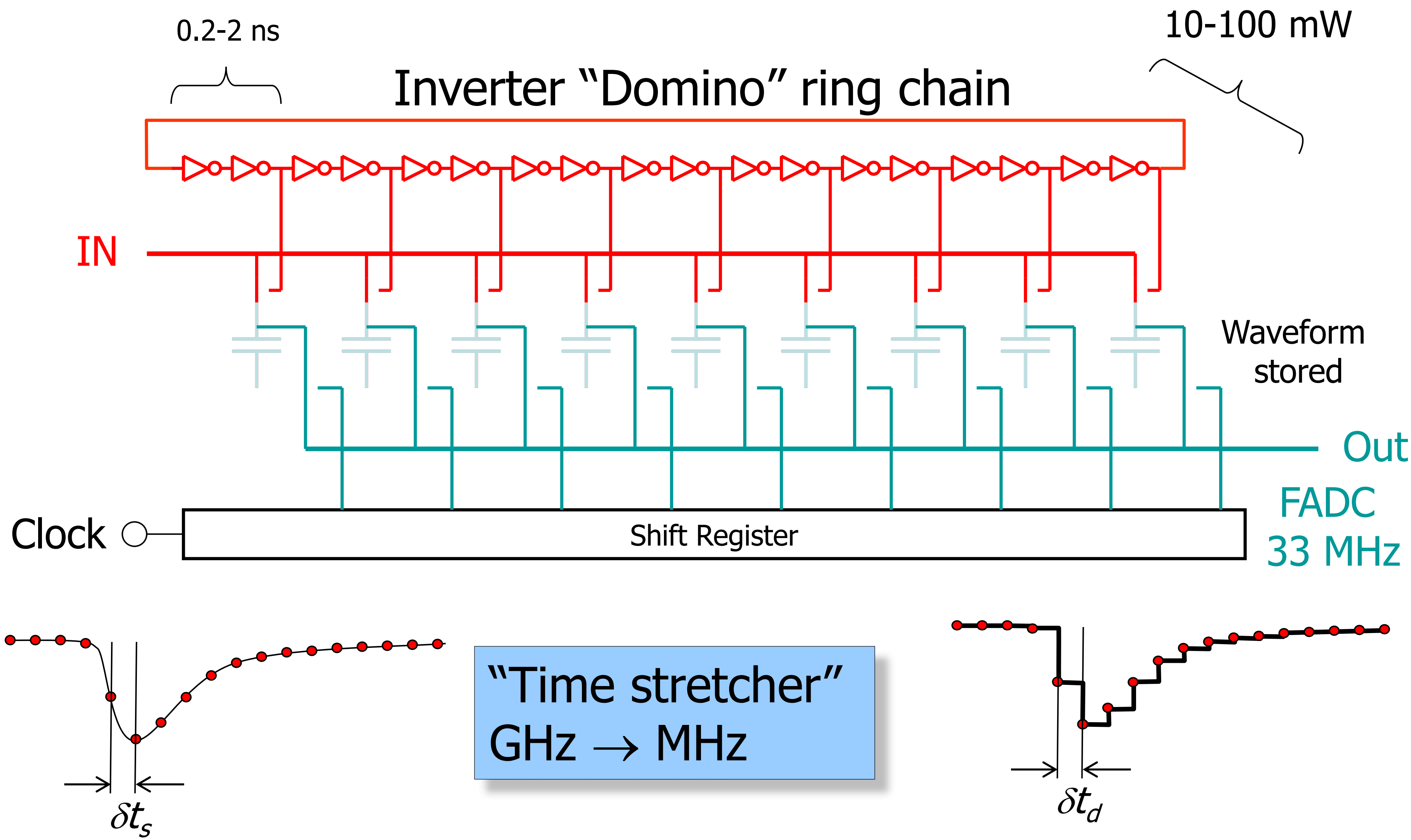
24x1.8 Gbits/s

1/10 k€/ch

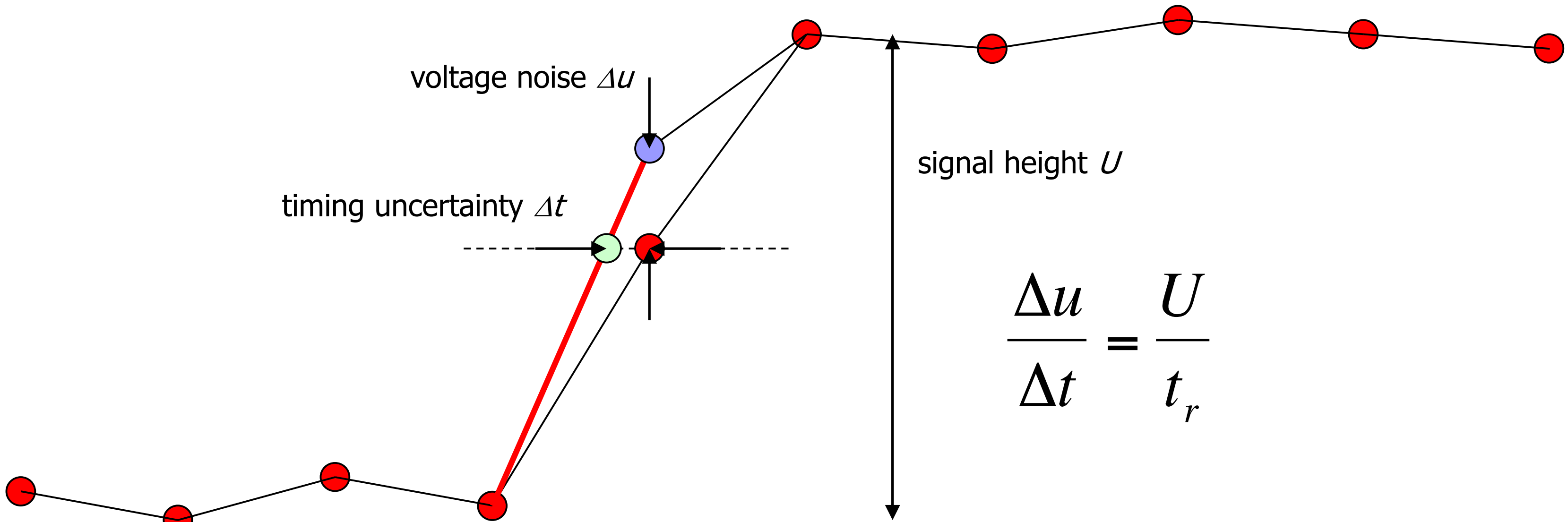
PX1500-4:
2 Channel
3 GS/s
8 bits

4 channels
5 GSPS
1 GHz BW
11.5 bits
900€
USB Power

Switched Capacitor Array (Analog Memory)



How is timing resolution affected?



$$\frac{\Delta u}{\Delta t} = \frac{U}{t_r}$$

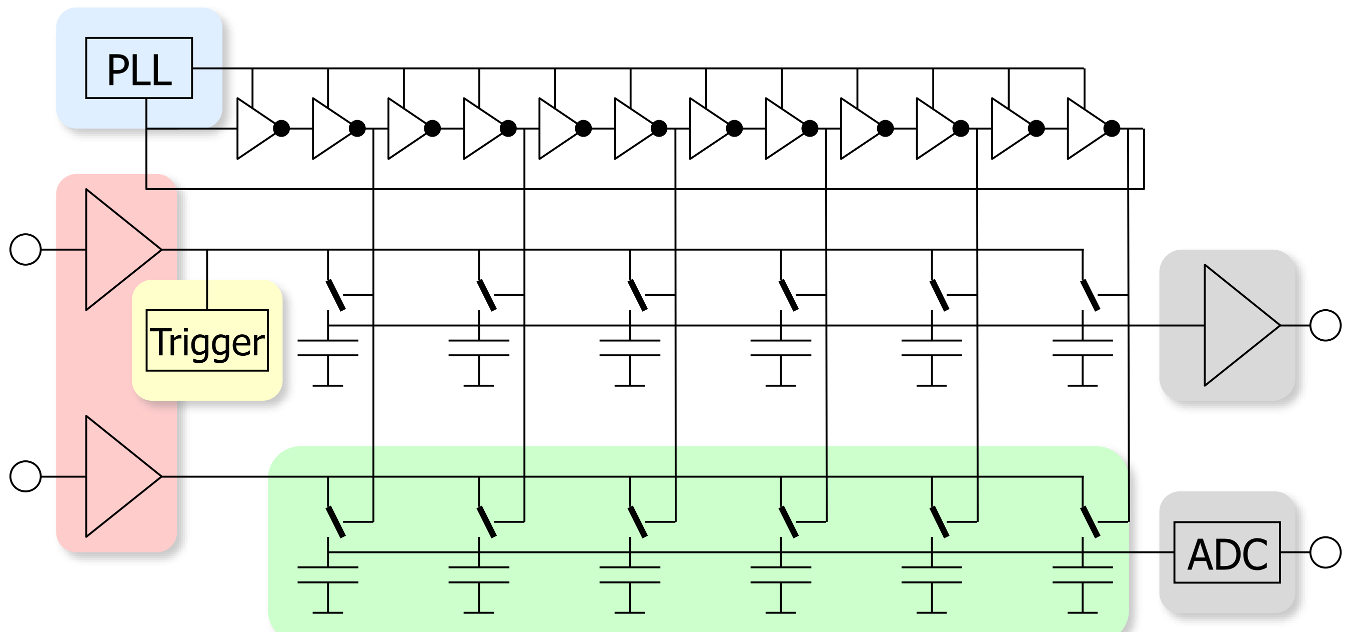
$$\Delta t = \frac{\Delta u}{U} \cdot \frac{1}{\sqrt{3 f_s \cdot f_{3dB}}}$$

Assumes zero aperture jitter

	U	Δu	f_s	f_{3db}	Δt
today:	100 mV	1 mV	2 GSPS	300 MHz	~10 ps
optimized SNR:	1 V	1 mV	2 GSPS	300 MHz	1 ps
next generation:	1V	1 mV	10 GSPS	3 GHz	0.1 ps

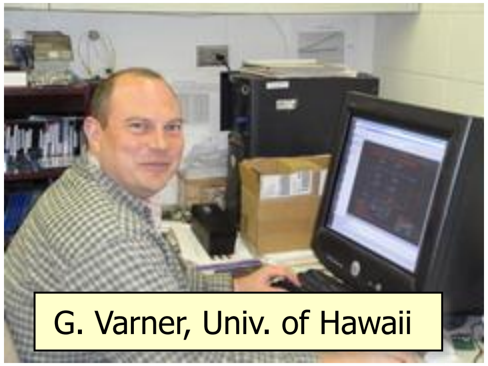
Design Options

- CMOS process (typically 0.35 … 0.13 μm) → sampling speed
- Number of channels, sampling depth, differential input
- PLL for frequency stabilization
- Input buffer or passive input
- Analog output or (Wilkinson) ADC
- Internal trigger
- Exact design of sampling cell



Switched Capacitor Arrays for Particle Physics

Omega

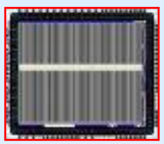


G. Varner, Univ. of Hawaii

E. Delagnes
D. Breton
CEA Saclay

H. Frisch et al., Univ. Chicago

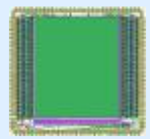
STRAW3 | LABRADOR3 | TARGET

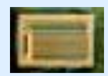


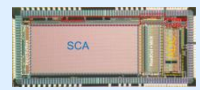
- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube …)

www.phys.hawaii.edu/~idlab/

AFTER | SAM | NECTAR0







- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

matacq.free.fr

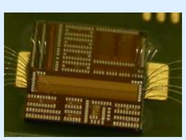
PSEC1 - PSEC4

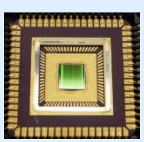
Poster 232

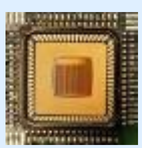
- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

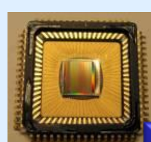
psec.uchicago.edu

DRS1 | DRS2 | DRS3 | DRS4









2002 | 2004 | 2007 | 2008

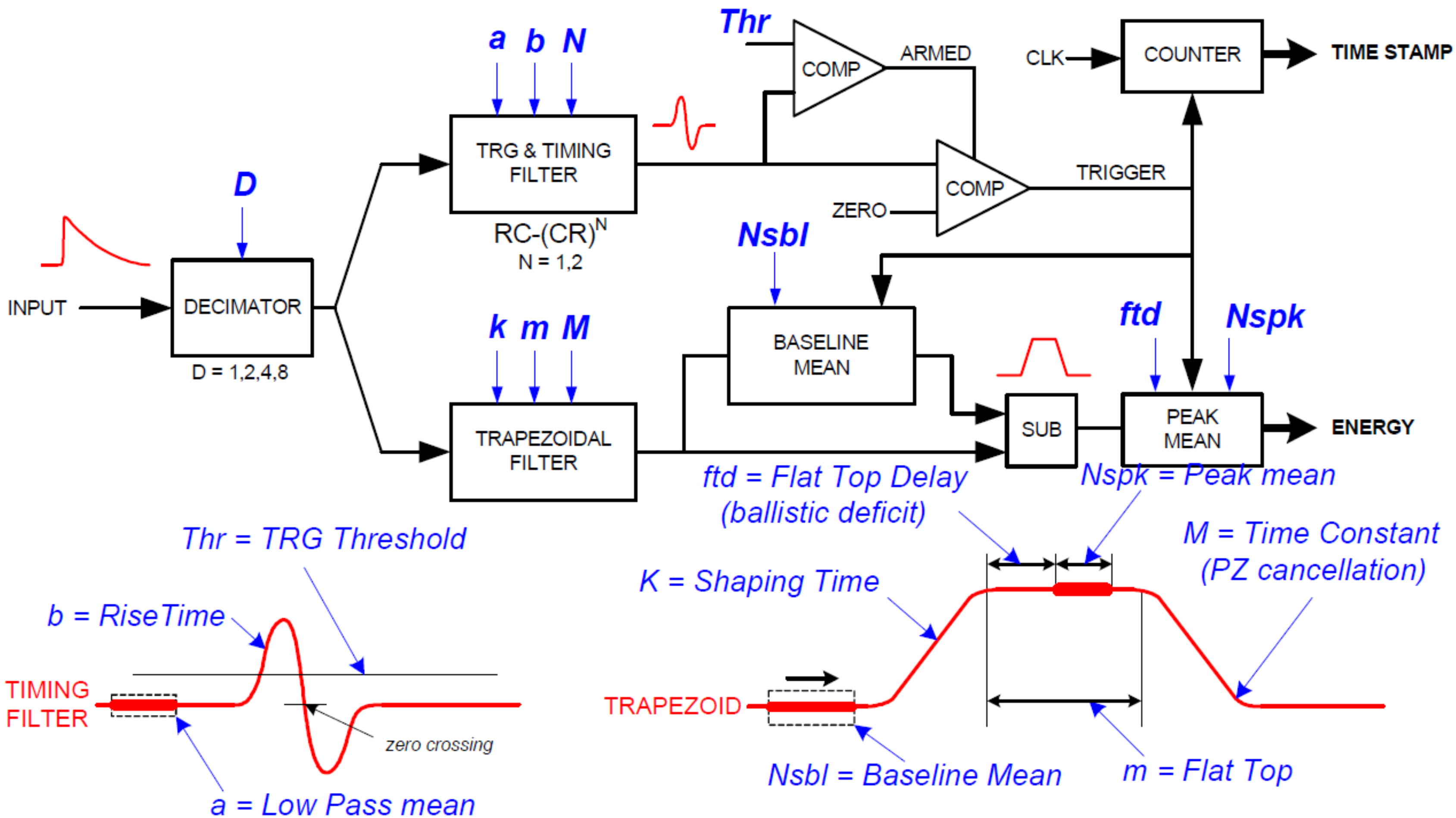
- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET

Poster 15, 106

Stefan Ritt
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

Digital Pulse Processing (DPP)



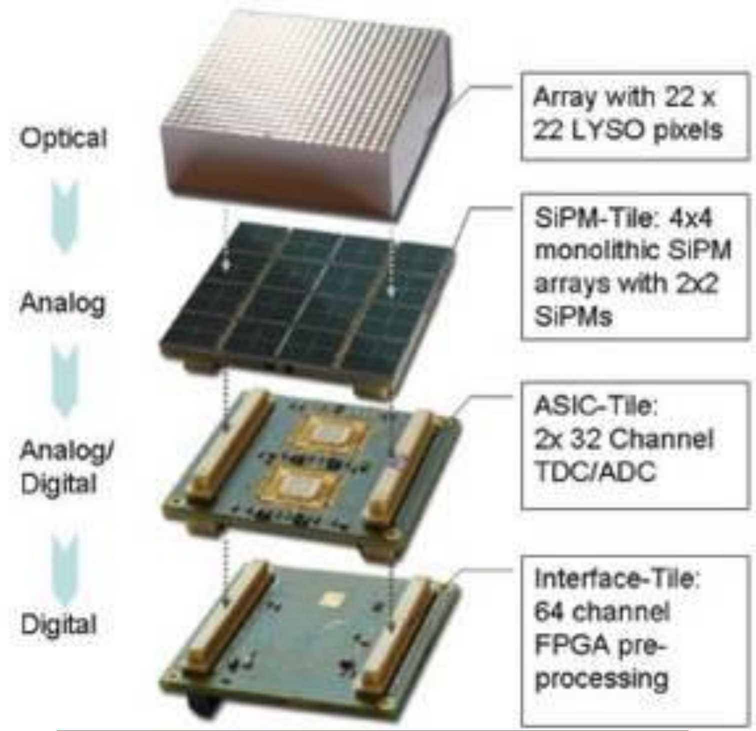
C. Tintori (CAEN)
V. Jordanov *et al.*, NIM **A353**, 261 (1994)

Comments

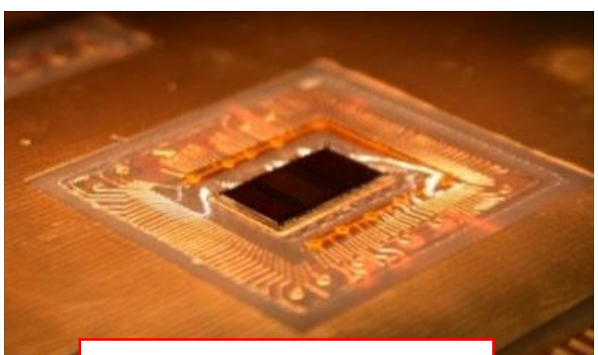
- Trends
  - Reduce dead time
  - increase analog bandwidth
  - Increase depth, give more latency
  - Include high speed low noise preamps (NECTAR…)

- Comments
  - Unbeatable for pulse shape analysis or discrimination
  - Ultra low timing measurements (ps)
  - More power hungry than dedicated front-end (many CdV/dt…), needs careful study for large systems (>> kch)

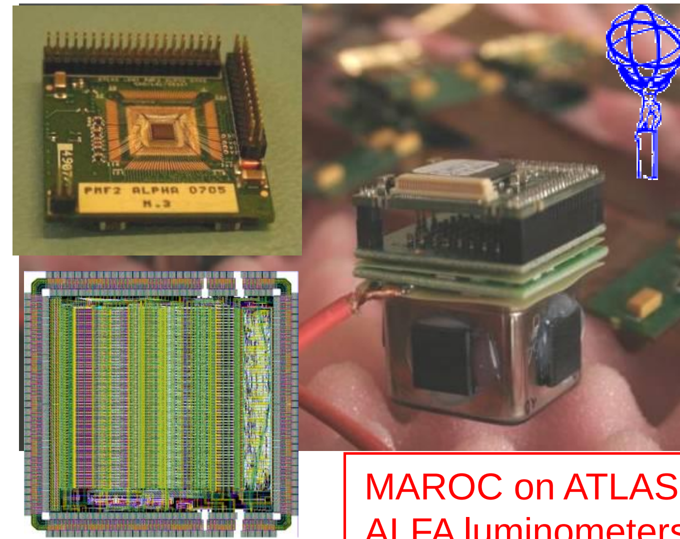
Electronics moves onto detectors



PET hyperimage project [P. Fisher]



SKIROC on ILC ECAL



MAROC on ATLAS ALFA luminometers

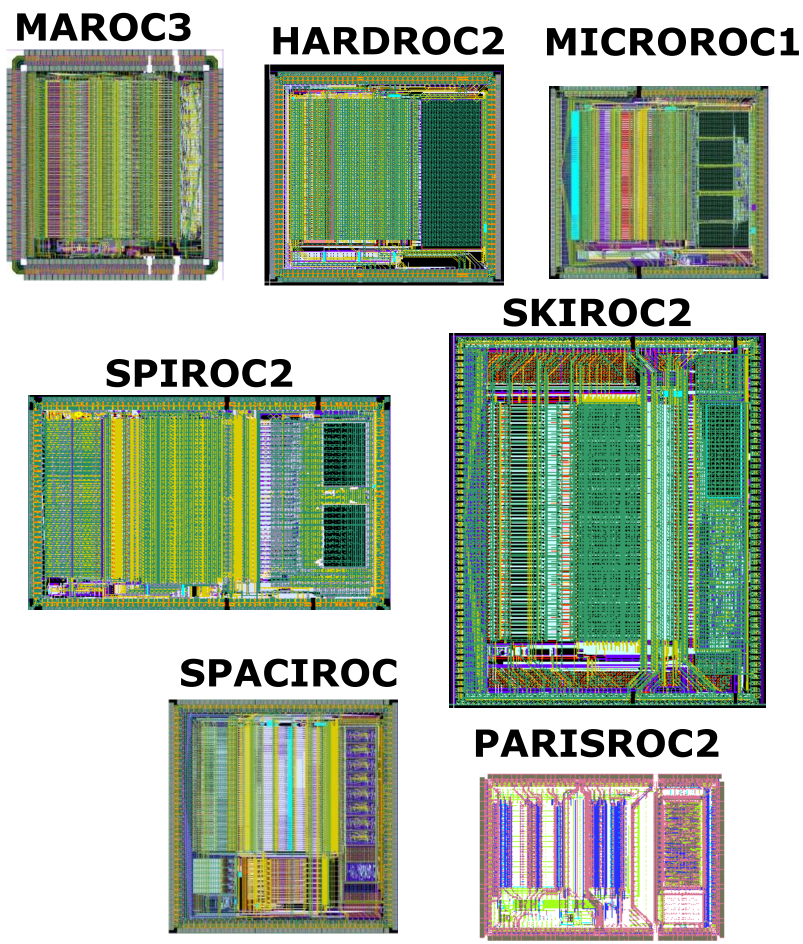
1m² RPC detector for ILC DHCAL [I. Laktineh]

Example of SoC : OMEGA « ROC chips »

- Move to Silicon Germanium 0.35 µm BiCMOS technology in 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

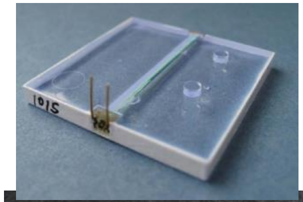
http://omega.in2p3.fr

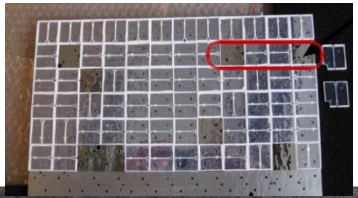
Chip	detector	ch	DR (C)
MAROC	PMT	64	2f-50p
SPIROC	SiPM	36	10f-200p
SKIROC	Si	64	0.3f-10p
HARDROC	RPC	64	2f-10p
PARISROC	PM	16	5f-50p
SPACIROC	PMT	64	5f-15p
MICROROC	µMegas	64	0.2f-0.5p
PETIROC	SiPM	32	10f-200p

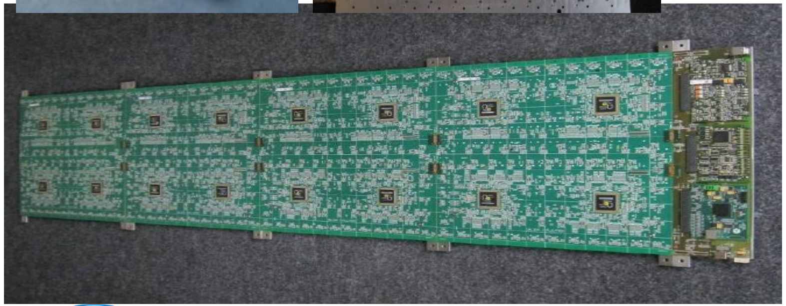


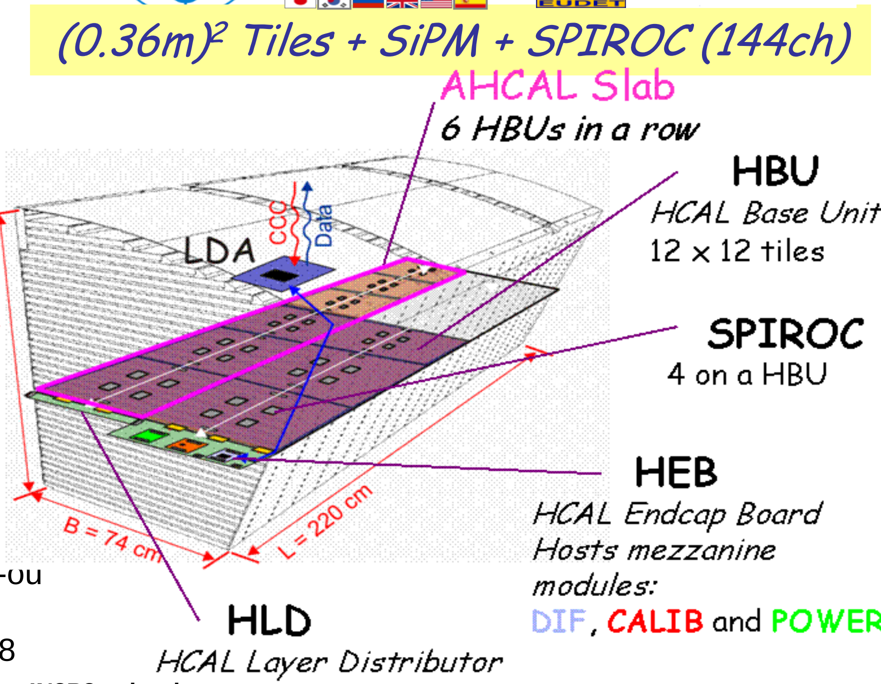
Example : SPIROC for SiPM

- SPIROC : Silicon Photomultiplier Integrated Readout Chip to read out the analog hadronic calorimeter for CALICE (ILC)
- **Ultra low-power 36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits, 1 pe to 2000 pe**
  - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
  - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step~1 ns TDC->TAC (fine time)
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - 4kbytes internal memory and daisy chain readout



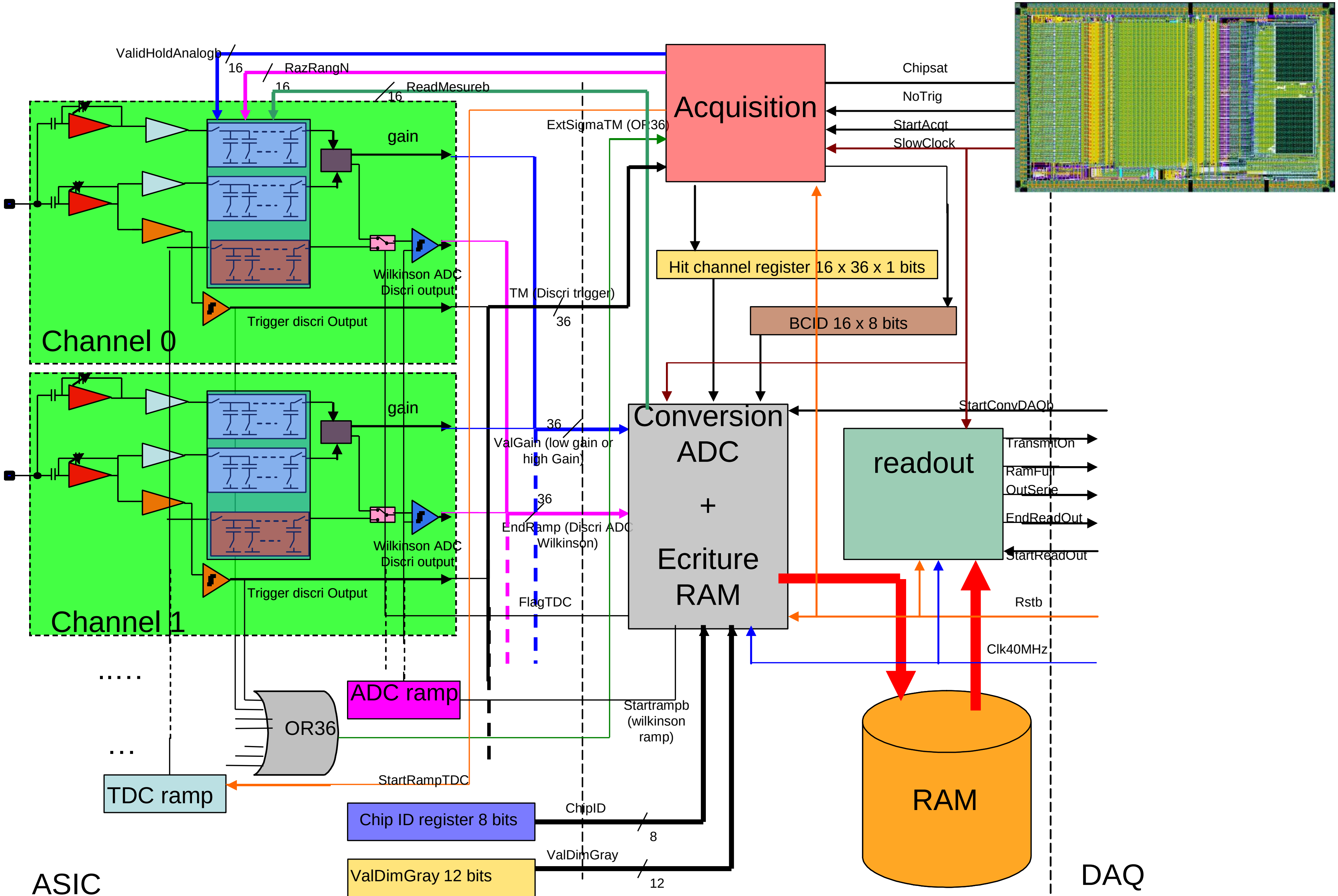






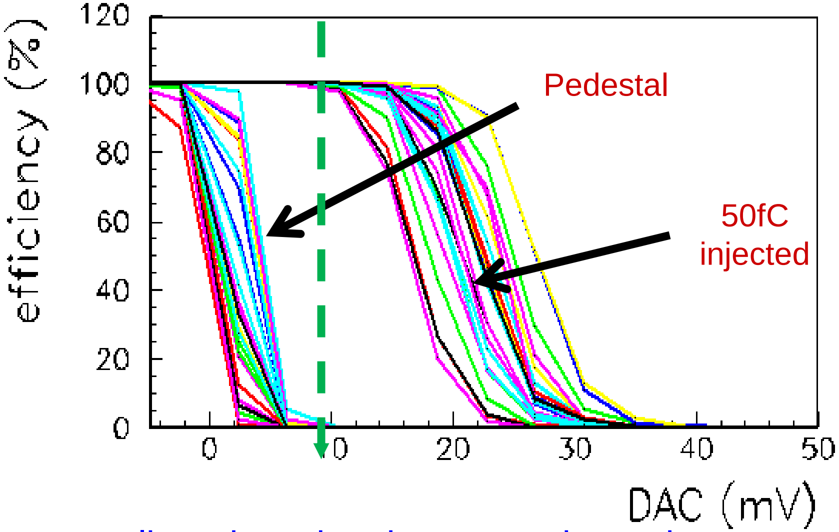
M. Bouchel, S. Callier, F. Dulucq, J. Fleury, J.-J. Jaeger, C. de La Ta G. Martin-Chassard, and L. Raux, “SPIROC (SiPM integrated read-ou chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out,” J. Instrum. 6(01), C01098 (2011).

SPIROC architecture

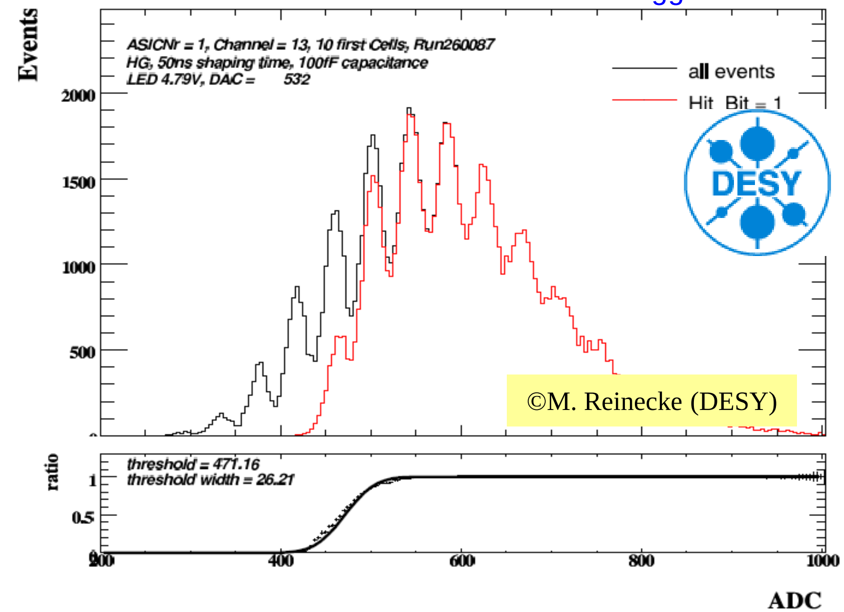


SPIROC: trigger efficiency measurements

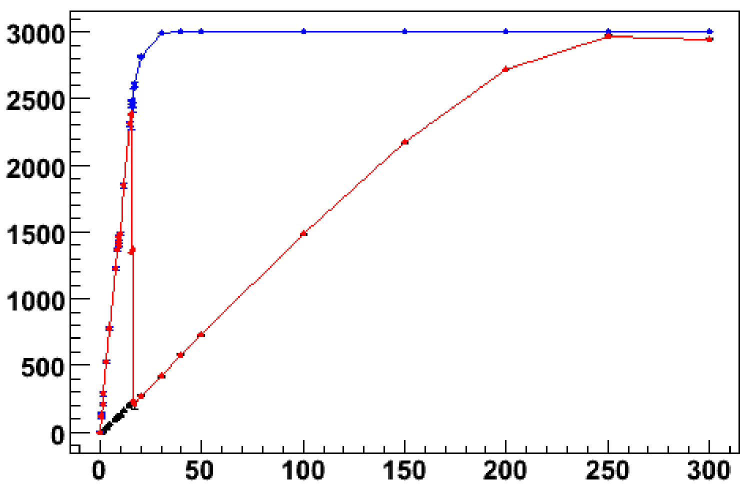
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



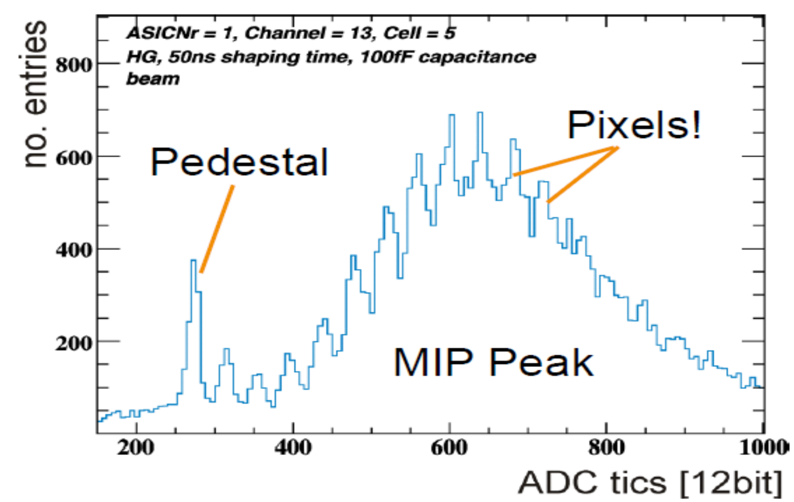
SiPM SPECTRUM with Autotrigger



linearity using the auto gain mode and internal ADC



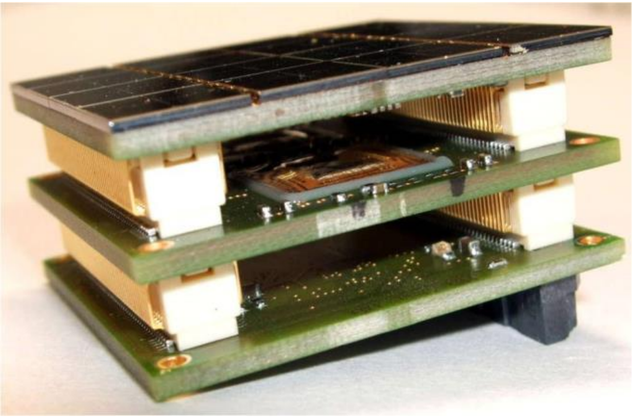
MIP response in DESY
6 GeV electron testbeam

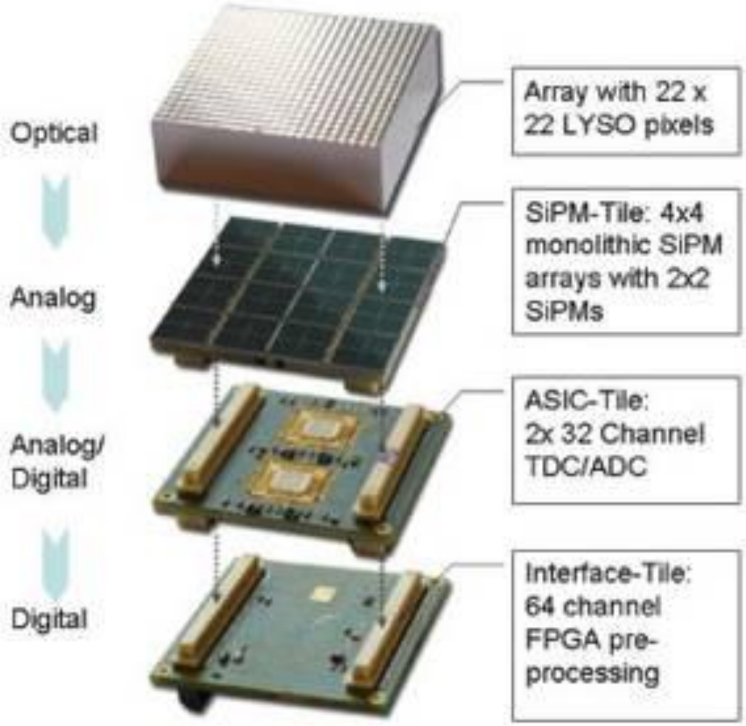


PET Hyperimage

- PET/MRI projekt
  - P. Fischer et al. Heidelberg, Philips, Aachen, FBK Trento
- 40-channel system on chip for readout of the detectors that generate low voltage (several mV) signals
- Combined high precision time (~14 ps) and energy measurements (signal integral = energy)
- Time of flight measurements with energy discrimination
- Particle recognition, by mass measurement
- Medical imaging (SiPM based PET)

- [M. Ritzert…: "*Compact SiPM based Detector Module for Time-of-Flight PET/MR*" on IEE NPS Real Time Conference





- Have fun designing electronics for future detectors !

Large collaborations… [V. Radeka]