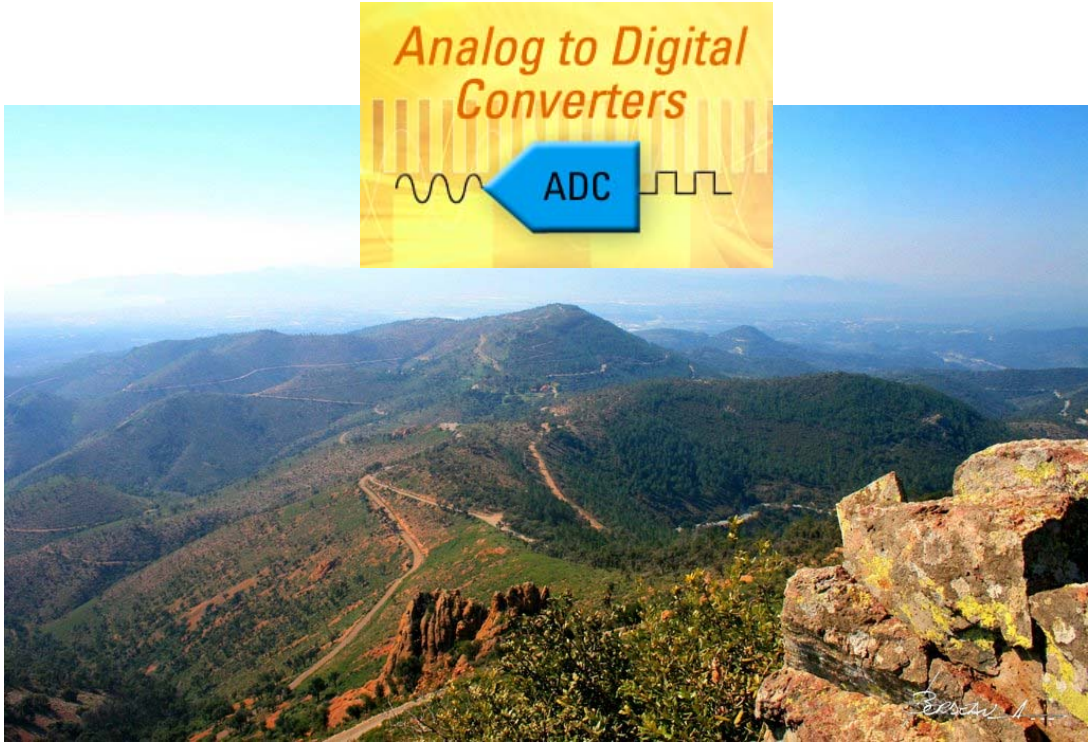
Conversion: mesures sur les ADC

Laurent Royer



Ecoles d'électronique analogique de l'IN2P3
Fréjus, juin 2014

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2ème partie: utilisation des ADC

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1. Choisir un ADC

Les principaux fabricants d'ADC (1)

AKM Semiconductor {Audio ADCs/DAC IC Manufacturer}

Analog Devices {Analog-to-Digital Converters/Digital-to-Analog Converter ICs}

Cirrus Logic {Audio A/D and D/A converters, CODEC Manufacturer}

Fairchild Semiconductor {ADCs/DAC IC Manufacturer}

Holtek Semiconductor Inc. {DAC/ADC ICs}

Intersil {ADCs/DAC IC Manufacturer}

Linear Technology {ADCs/DAC IC Manufacturer}

Maxim Integrated Products {ADCs/DAC IC Manufacturer}

Microchip {Delta-Sigma/Dual Slope/Binary/BCD ADC ICs}

National Semiconductor {ADCs/DAC IC Manufacturer}

NEC {D/A Converter for Audio System}

NJR Corporation {ADC-DAC-V/F-F/V Converter ICs}

Renesas Technology America, Inc {D/A R2R, Multiplying, A/D Converter}

Sony {A/D Converter 1:2 De-Multiplex, TTL Output, Sample & Hold, D/A Converter}

Thaler Corp. {A/D Converter Manufacturer. ADC 18-26 bits}

Texas Instruments 'TI' {ADC-DAC-Voltage/Freq Converter IC Manufacturers}

Wavefront Semiconductor {48kHz 24-bit stereo audio ADC, low-cost 24-bit DAC IC Manufacturer}

Wolfson Microelectronics
{Mono, Multi-channel and Stereo ADCs}

http://www.interfacebus.com/Analog_DAC.html

Les principaux fabricants d'ADC (2)

- ✓ Analog Devices: 604 références
  - ✓ Precision and General purpose ADCs (<=10MSPS) (310)
  - ✓ High speed ADCs (> 10MSPS) (294)

PRECISION AND GENERAL PURPOSE ADC FINDER

Resolution (Bits)	ADC Throughput Rate (SPS)					
	<1k	1 - 100k	100 - 250k	250 - 450k	450k - 1M	1M - 10M
18 - 24	✓	✓	✓	✓	✓	✓
14 - 17	✓	✓	✓	✓	✓	✓
8 - 13	✓	✓	✓	✓	✓	✓

HIGH-SPEED ADC FINDER

Resolution (Bits)	ADC Throughput Rate (MSPS)			
	10 - 50	50 - 100	100 - 250	250+
>/=16	✓	✓	✓	✓
14 - 15	✓	✓	✓	✓
12 - 13	✓	✓	✓	✓
10 - 11	✓	✓	✓	✓
</=9	✓	✓	✓	✓

SELECTION TABLE FOR 18 TO 24 BIT, 1 MSPS TO 10 MSPS

Sort by newest | Choose parameters | Quick Filter | Reset Table | Download to Excel | Help | Maximize Filters

Part #	Hardware	Resolution (Bits) (bit)	Throughput Rate (SPS)	# Channels	Full Power BW (Hz)	Vsupply Pos (min) (V)	Max Pos Supply (V) (V)	Power Dissipation (W)	US Price 1000-4999 ($ US)
	0 Values ...	4 Values Selected	1M - 10M	0 Values Selec...	23.4 - 2G	1.22 - 12	1.7 - 16.5	142u - 4.05	0.95 - 833.21
AD7960	✓	18	5 MSPS	1	28 MHz	4.75 V	5.25 V	21 mW	$31.00
AD7986		18	2 MSPS	1	19 MHz	4.75 V	5.25 V	29 mW	$29.95
AD7984	✓	18	1.33 MSPS	1	-	2.375 V	2.625 V	14 mW	$28.29
AD7982	✓	18	1 MSPS	1	10 MHz	2.375 V	2.625 V	8.6 mW	$23.28
AD7643		18	1.25 MSPS	1	50 MHz	2.3 V	3.6 V	80 mW	$19.50
AD7641		18	2 MSPS	1	50 MHz	2.5 V	2.5 V	92 mW	$29.33
AD7760		24	2.5 MSPS	1	1.35 MHz	4.75 V	5.25 V	958 mW	$24.90

Aide au choix: *ressources*

ADDITIONAL RESOURCES

Application Notes

- Frequency Domain Response of Switched-Capacitor ADCs (pdf)
- How ADIsimADC Models an ADC (pdf)
- Understanding High Speed ADC Testing and Evaluation (pdf)
- VisualAnalog™ Converter Evaluation Tool Version 1.0 User Manual (pdf)

Circuit Notes

- Using the AD8376 VGA to Drive Wide Bandwidth ADCs for High IF AC-Coupled Applications (CN0002)
- Interfacing the ADL5534 Dual IF Gain Block To The AD9640 High Speed ADC (CN0049)
- Driving the AD9233/9246/9254 ADCs in AC-Coupled Baseband Applications (CN0051)
- Interfacing the ADL5382 Quadrature I/Q Demodulator to the AD9262 16-Bit Continuous Time Sigma-Delta ADC as an RF-to-Bits Solution (CN0062)
- Low Noise, Low Distortion Single-Ended Input Drive Circuit for Differential Input IF Sampling ADCs (CN0171)
- High Performance, 16-Bit, 250 MSPS Wideband Receiver with Antialiasing Filter (CN0227)

Mini Tutorials

- MT-003: Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor (pdf)
- MT-004: The Good, the Bad, and the Ugly Aspects of ADC Input Noise– Is No Noise Good Noise? (pdf)
- MT-006: ADC Noise Figure – An Often Misunderstood and Misinterpreted Specification (pdf)
- MT-007: Aperture Time, Aperture Jitter, Aperture Delay Time – Removing the Confusion (pdf)
- MT-012: Intermodulation Distortion Considerations for ADCs (pdf)

Seminars

- Data Conversion Handbook

Technical Articles

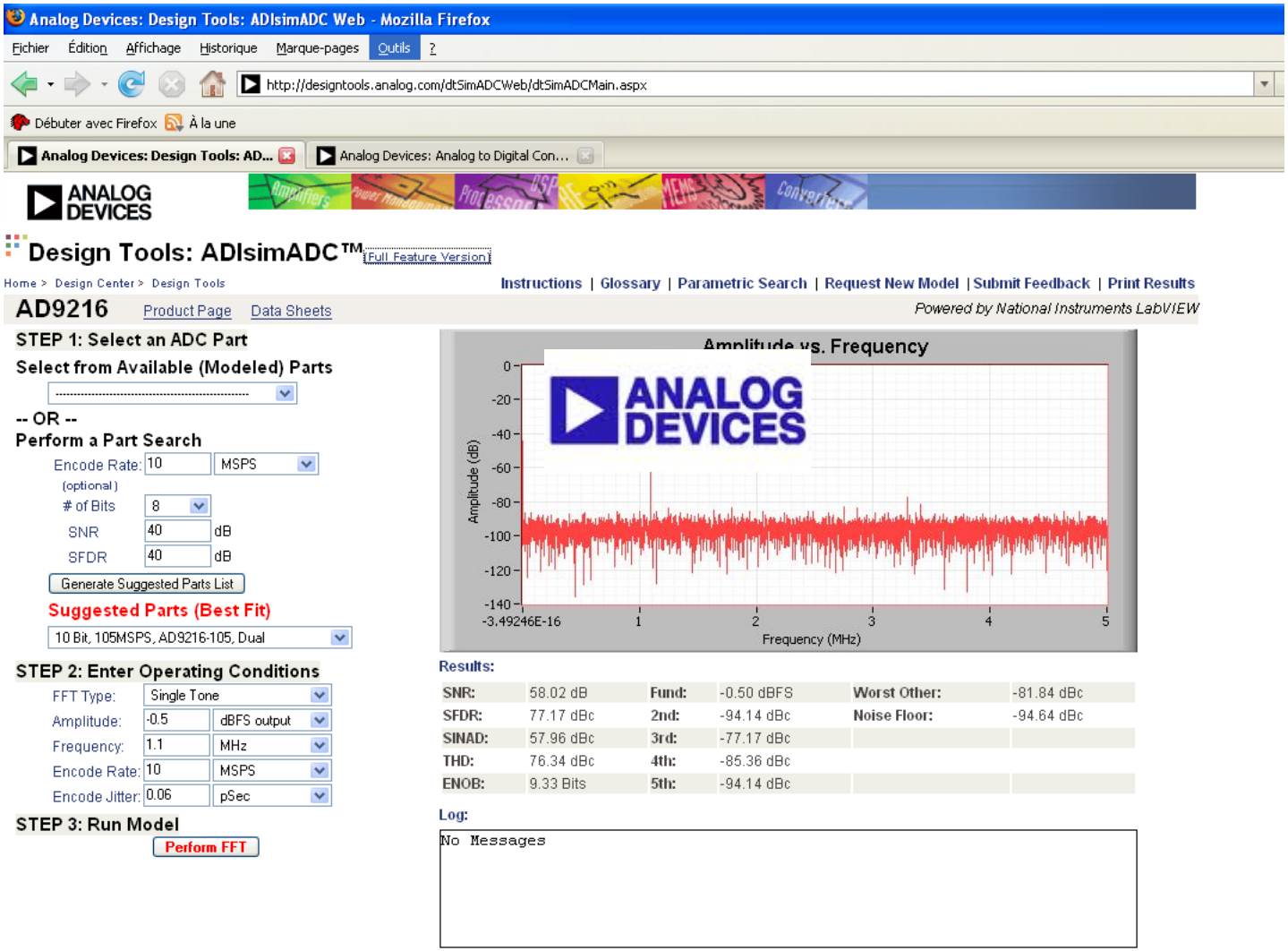
- Analog-to-Digital Converter Clock Optimization: A Test Engineering Perspective
- Redefining the Role of ADCs in Wireless (pdf)
- Understanding AC Behaviors of High Speed ADCs (pdf)

Webcasts

- Converter Simulation – Beyond the Eval Board

Aide au choix: *Design tools*

http://designtools.analog.com/dtSimADCWeb/dtSimADCMain.aspx



Exemples

ADC 24 bits, 10Hz :AD7780

ADC 8 bits, 500MS/s AD9484

Les principaux fabricants d'ADC (4)

- ✓ National Semiconductor → Ti depuis 2011

Products for Analog to Digital Converter

TI delivers a broad portfolio of high-speed and precision analog-to-digital converters (ADC). Products range from 12-bit to 18-bit SAR ADC, 16-bit to 24-bit delta-sigma ADC, and 10-bit to 16-bit pipeline ADC. TI's A/D converter portfolio targets a wide variety of applications for communications, industrial, consumer and many more.

View New Products

ADC16DX370 : Dual 16-bit 370 MSPS ADC, 7.4 Gbps JESD204B Outputs

DDC1128 : 128-Channel, Current-Input Analog-to-Digital Converter

AFE1256 : 256-Channel Analog Front-End fc Flat-Panel Digital X-ray Detector

Technical Documents

- **Understanding Low-Amplitude Behavior of 11-bit ADCs** (sboa133.HTM, 8 KB)
  22 Oct 2011 Abstract
- **A Glossary of Analog-to-Digital Specifications and Performance Characteristics (Rev. B)**
  (sbaa147b.HTM, 8 KB)
  09 Oct 2011 Abstract

Browse Other Products | Send Email | Download | Save Settings

Add/Hide Parameters

Total Parts: 774
Matching Parts: 7

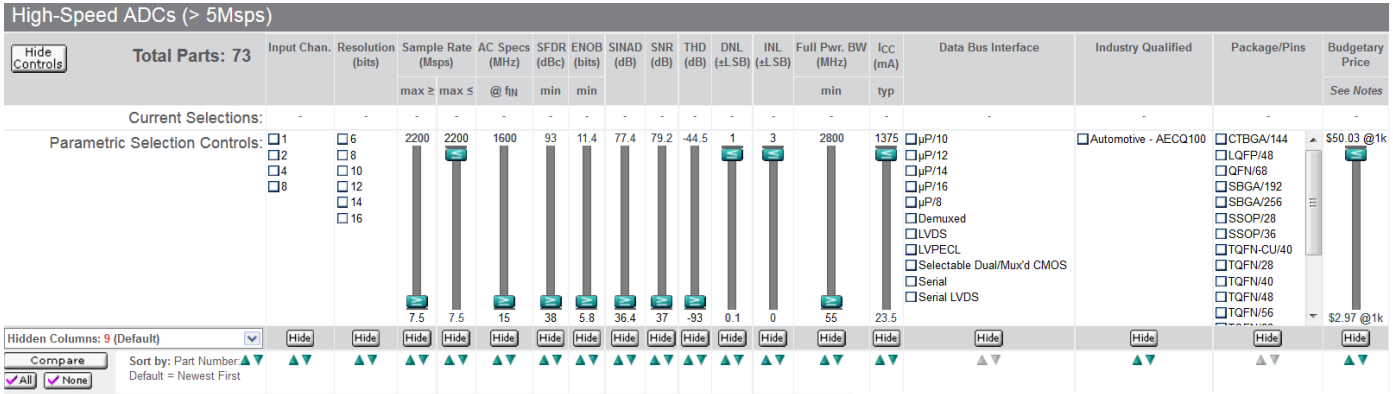
Reset

Status	SubFamily	Resolution (Bits)	Sample Rate (max) (SPS)	# Input Channels	INL (Max) (+/-LSB)	SNR (dB)	SFDR (dB)	Power Consumption (Typ) (mW)	Interface	Architecture	Analo Voltag AV/DI (Min)
ACTIVE, PREVIEW	Current Input ADC, High Speed ADC (>10MSPS), High Speed ADC (>=1GSPS), Isolated ADC, Precision ADC (<=10MSPS)	≤24 / ≥24	≤999 / ≥100	≤256 / ≥1	≤10 / ≥0.09	≤111 / ≥42.7	≤98 / ≥42	≤4,400 / ≥0.21	Byte-Wide, CMOS, DDR LVDS, JESD204A, JESD204B, Microwire (Serial I/O), Parallel CMOS, Parallel LVDS, QSPI, Serdes, Serial	Continuous-Time Delta Sigma, Delta-Sigma, Digital Filter, Dual-Slope, Flash, Folding Interpolating, Hybrid Pipeline-SAR, Modulator, Pipeline, SAR, String, Two-Step	≤5.5
ACTIVE	Precision ADC (<=10MSPS)	24	780SPS	8	-	-	-	0.6	Serial SPI	Delta-Sigma	2.7
ACTIVE	Precision ADC (<=10MSPS)	24	780SPS	8	-	-	-	0.8	Serial SPI	Delta-Sigma	2.7
ACTIVE	Precision ADC (<=10MSPS)	24	780SPS	8	-	-	-	0.8	Serial SPI	Delta-Sigma	2.7

ADS1216 - 24-Bit Analog-to-Digital Converter
ADS1217 - 8-Channel, 24-Bit Analog-To-Digital Converter
ADS1218 - 24-Bit, 780 SPS ADC w/FLASH Memory, 8 CH, Vref, Buffer, 2 IDACs, Serial Out,

Les principaux fabricants d'ADC (5)

- ✓ Maxim Integrated Products: 563 références (433 en 2009)
  - ✓ Display-Oriented ADCs (33)
  - ✓ High-Speed ADCs (> 5Msps) (73)
  - ✓ Precision ADCs (≤ 5Msps) (457): 8 à 24 bits (16 bits max en 2009)



High-Speed ADCs (> 5Msps)

Hide Controls — Total Parts: 73

	Input Chan.	Resolution (bits)	Sample Rate (Msps) max ≥	Sample Rate (Msps) max ≤	AC Specs (MHz) @ f_{IN}	SFDR (dBc) min	ENOB (bits) min	SINAD (dB)	SNR (dB)	THD (dB)	DNL (±LSB)	INL (±LSB)	Full Pwr. BW (MHz) min	I_{CC} (mA) typ	Data Bus Interface	Industry Qualified	Package/Pins	Budgetary Price See Notes
Current Selections:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Parametric Selection Controls:	☐1 ☐2 ☐4 ☐8	☐6 ☐8 ☐10 ☐12 ☐14 ☐16	2200	2200	1600	93	11.4	77.4	79.2	-44.5	1	3	2800	1375	☐µP/10 ☐µP/12 ☐µP/14 ☐µP/16 ☐µP/8 ☐Demuxed ☐LVDS ☐LVPECL ☐Selectable Dual/Mux'd CMOS ☐Serial ☐Serial LVDS	☐Automotive - AECQ100	☐CTBGA/144 ☐LQFP/48 ☐QFN/68 ☐SBGA/192 ☐SBGA/256 ☐SSOP/28 ☐SSOP/36 ☐TQFN-CU/40 ☐TQFN/28 ☐TQFN/40 ☐TQFN/48 ☐TQFN/56	$50.03 @1k
			7.5	7.5	15	38	5.8	36.4	37	-93	0.1	0	55	23.5				$2.97 @1k
Hidden Columns: 9 (Default)	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide	Hide
Compare ☑All ☑None — Sort by: Part Number: Default = Newest First	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼	▲▼
☑ MAX19527 Octal, 12-Bit, 50Msps, 1.8V ADC With Serial LVDS Outputs	8	12	50	50	19.3	84	11	68.2	68.5	-81	0.3	0.5	500					
☑ MAX19515 Dual-Channel, 10-Bit, 65Msps ADC	2	10	65	65	70	77	-	59.6	60.1	-79	0.2	0.25	850					
☑ MAX19516 Dual-Channel, 10-Bit, 100Msps ADC	2	10	100	100	70	83	-	59.5	60	-79	0.2	0.25	850					
☑ MAX19517 Dual-Channel, 10-Bit, 130Msps ADC	2	10	130	130	70	82	-	59.4	59.8	-78	0.2	0.25	850					
☑ MAX1437B Octal, 12-Bit, 50Msps, 1.8V ADC With Serial LVDS Outputs	8	12	50	50	20	93	11.4	69.7	70.1	-93	0.25	0.3	100					
☑ MAX19507 Dual-Channel, 8-Bit, 130Msps ADC	2	8	130	130	70	77	-	49.3	49.8	-72	0.1	0.1	850					
☑ MAX19506 Dual-Channel, 8-Bit, 100Msps ADC	2	8	100	100	70	77	-	49.3	49.8	-72	0.1	0.1	850					
☑ MAX19505 Dual-Channel, 8-Bit, 65Msps ADC	2	8	65	65	70	77	-	49.3	49.8	-72	0.1	0	850					
☑ MAX109 8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs	1	8	2200	2200	1600	50.3	-	42.1	44	-46.6	0.25	0.25	2800					
☑ MAX1213N 1.8V, 12-Bit, 170Msps ADC for Broadband Applications	1	12	170	170	100	87	-	67.1	67.2	-	0.3	0.55	700					

Precision ADC Selection Table

Maxim's precision ADCs feature successive-approximation-register (SAR) and sigma-delta architectures. These precision ADCs deliver resolutions from 8 to 24 bits and a wide range of sampling rates, with single and multiple channels. Click a cell below to find a product that matches your design requirements.

Resolution Bits	< 10ksps	10ksps to < 100ksps	100ksps to < 200ksps	200ksps to < 500ksps	500ksps to < 1Msps	1Msps to 2Msps	2Msps and above
≤ 10	●	●	●	●	●	●	●
12	●	●	●	●	●	●	●
14-16	●	●	●	●	●		
18-24	●	●		●	●	●	

Les principaux fabricants d'ADC (6)

- **Audio** (≤ 200kS/s, ≥ 16bits):
  - ✓ AKM Semiconductor
  - ✓ Cirrus Logic
  - ✓ Holtek Semiconductor Inc. {16 voies avec µ-processeur et interface SPI ou USB}
  - ✓ NEC
  - ✓ Wavefront Semiconductor {48kHz 24-bit stéréo audio ADC}
  - ✓ Wolfson Microelectronics {ADCs/DAC IC Manufacturer}

- **Vidéo** (≥ 30MS/s, 8bits):
  - ✓ Intronics Inc.

- **Affichage**
  - ✓ Intronics Inc. (LCD/LED Display)
  - ✓ NJR. (LCD Display)
  - ✓ Sony {ADC 1:2 De-Multiplex, TTL Output, SampleHold, D/A Converter} → obsolète
- **Rad Hard**
  - ✓ e2v{10 bits – 2.2 GHz}
  - ✓ ST micro. (12/14 bits – 50/20 MS/s)
- **Autre**
  - ✓ Thaler Corp. {ADC à rampe 18-26 bits très lent }
  - ✓ Intronics Inc. (Flash, Pipeline, ΔΣ, SAR)
  - ✓ Intersil {ADCs/DAC IC Manufacturer}
  - ✓ Linear Technology
    - ✓ Pipeline 16bits-160MS/s-1,45W
    - ✓ 16bits ΔΣ avec interface I2C
  - ✓ Microchip {ΔΣ, SAR, Dual Slope/Binary/BCD ADC} pas grand choix

2. Evaluer un ADC:

⇨ les principes de mesure

Document de référence

IEEE Std 1241-2000

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

Contents

Source: Norme IEEE [IEEE]

Critical ADC parameters

Table 1—Critical ADC parameters

Typical applications	Critical ADC parameters	Performance issues
Audio	SINAD, THD	Power consumption. Crosstalk and gain matching.
Automatic control	Monotonicity Short-term settling, long-term stability	Transfer function. Crosstalk and gain matching. Temperature stability.
Digital oscilloscope/waveform recorder	SINAD, ENOB Bandwidth Out-of-range recovery Word error rate	SINAD for wide bandwidth amplitude resolution. Low thermal noise for repeatability. Bit error rate.
Geophysical	THD, SINAD, long-term stability	Millihertz response.
Image processing	DNL, INL, SINAD, ENOB Out-of-range recovery Full-scale step response	DNL for sharp-edge detection. High-resolution at switching rate. Recovery for blooming.
Radar and sonar	SINAD, IMD, ENOB SFDR Out-of-range recovery	SINAD and IMD for clutter cancellation and Doppler processing.
Spectrum analysis	SINAD, ENOB SFDR	SINAD and SFDR for high linear dynamic range measurements.
Spread spectrum communication	SINAD, IMD, ENOB SFDR, NPR Noise-to-distortion ratio	IMD for quantization of small signals in a strong interference environment. SFDR for spatial filtering. NPR for interchannel crosstalk.
Telecommunication personal communications	SINAD, NPR, SFDR, IMD Bit error rate Word error rate	Wide input bandwidth channel bank. Interchannel crosstalk. Compression. Power consumption.
Video	DNL, SINAD, SFDR, DG, DP	Differential gain and phase errors. Frequency response.
Wideband digital receivers SIGINT, ELINT, COMINT	SFDR, IMD SINAD	Linear dynamic range for detection of low-level signals in a strong interference environment. Sampling frequency.

COMINT = communications intelligence
DNL = differential nonlinearity
ENOB = effective number of bits
ELINT = electronic intelligence
NPR = noise power ratio
INL = integral nonlinearity
DG = differential gain error

SIGINT = signal intelligence
SINAD = signal-to-noise and distortion ratio
THD = total harmonic distortion
IMD = intermodulation distortion
SFDR = spurious free dynamic range
DP = differential phase error

Source: Norme IEEE [IEEE]

Bancs de test dynamique

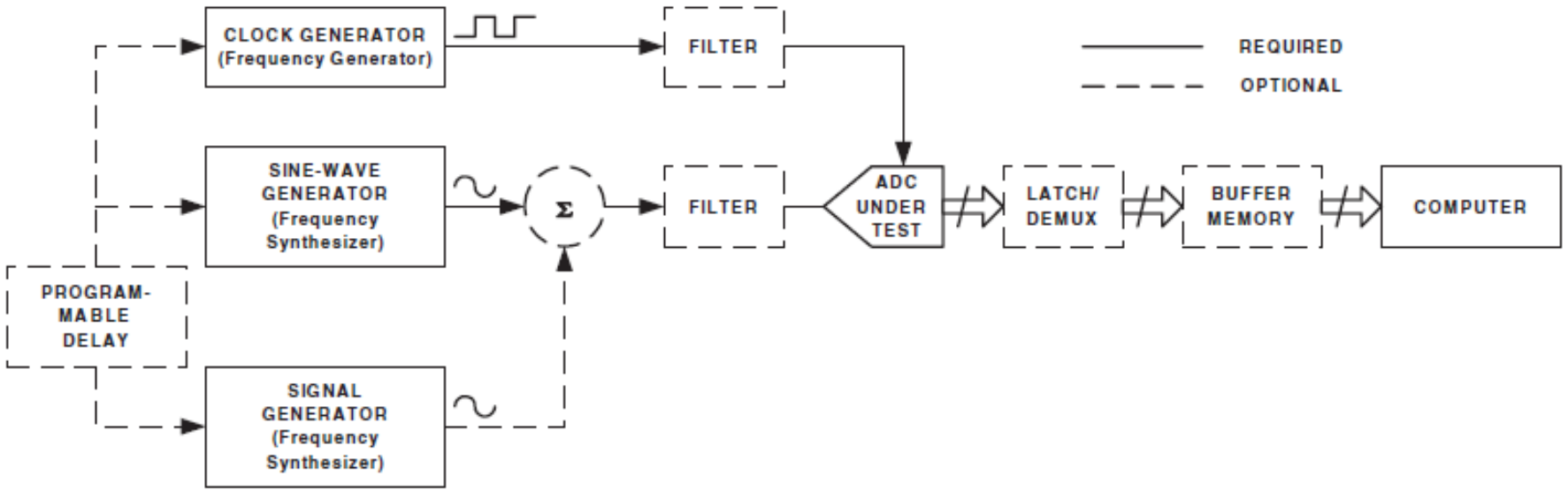


Figure 3—Setup for sine wave testing

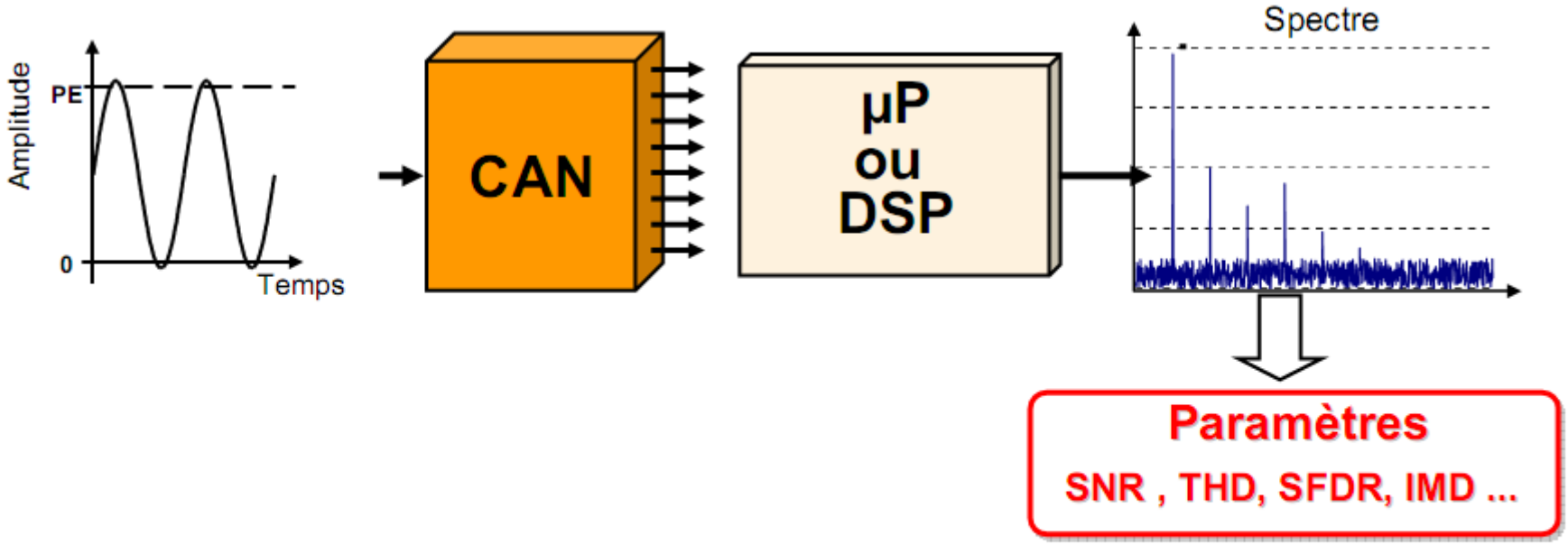
De la « pureté » fréquentielle du signal sinusoïdal d'entrée dépend la précision de la mesure.

Un filtrage sélectif sur la fréquence de test est généralement nécessaire → plusieurs filtres requis pour balayer une plage en fréquence.

Filtrage de l'horloge pour réduire le jitter.

Source: Norme IEEE [IEEE]

Test par FFT



☹ Sensible à la Synchro.

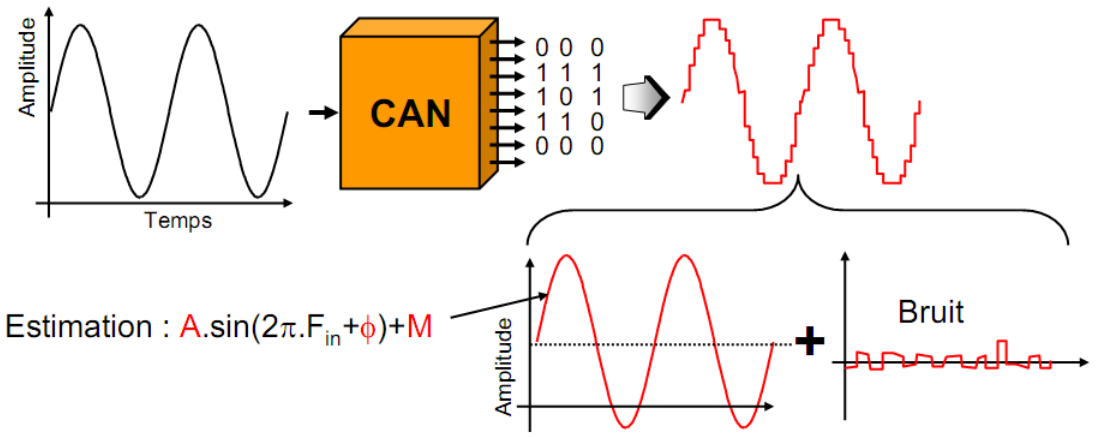
☹ Pas de paramètres Stat.

☺ Rapide

☺ Application Indus.

Source: S.Bernard, LIRMM [BER]

Régression sinusoïdale (1)



- **Principe :**
  - ✓ Signal d'entrée sinusoïdal (1.sin(2π.Fin+ϕ)) → Signal « parfait »
  - ✓ Estimer le signal sinusoïdal de la forme (A.sin(2π.Fin+ϕ)+M) vu à travers le convertisseur
  - ✓ Les paramètres M, A donnent respectivement la valeur du gain et de l'offset du CAN sous test

☹ ~~Complexité~~
☹ ~~Temps de calcul~~
☹ ~~Peu utilisé~~

Fonction sous ***sfit4*** MATLAB:
→ estime l'erreur rms par rapport à sinusoïde idéale
→ estime l'ENOB =log2(2^n_bits/(X.erms*sqrt(12)))

☺ Précision

Source: S.Bernard, LIRMM [BER]

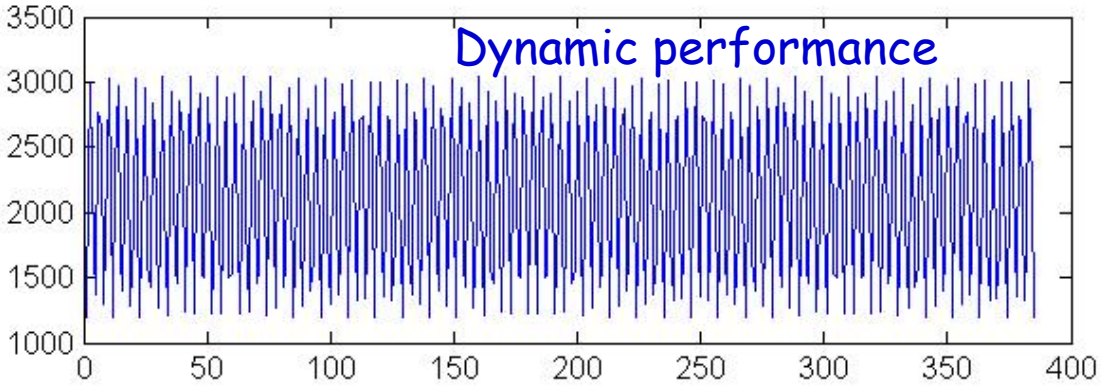
Régression sinusoïdale (2)

Fonction sous ***sfit4*** MATLAB:

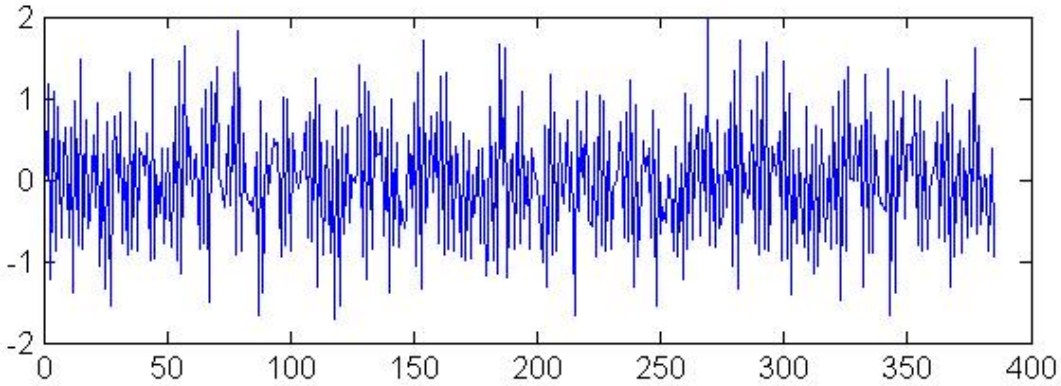
→ estime l'erreur rms par rapport à sinusoïde idéale

→ estime l'ENOB =log2(2^n_bits/(X.erms*sqrt(12)))

```
%SFIT4  IEEE-STD-1241
Standard four parameter
fit of a sine wave to
measured data
```



ENOB=10.5 @ 10.625MHz



Bancs de test statique

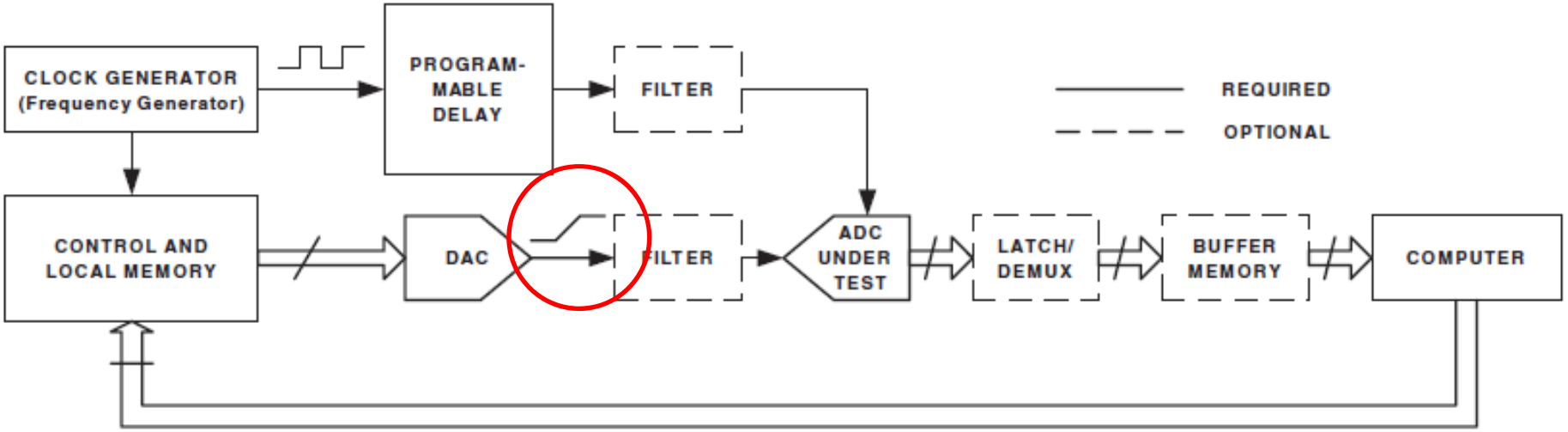


Figure 4—Setup for arbitrary signal testing

Variation lente du signal d'entrée par rapport à la fréquence d'horloge.

Signal arbitraire = signal rampe

Source: Norme IEEE [IEEE]

Test avec un signal Rampe

- Temps de montée de la rampe >> période de l'horloge
- Δv entre chaque cout d'horloge de l'ADC << au pas de quantification (pour déterminer la DNL)

Ex: ADC 12bits @ 40MHz sur 1V → Δv en 25ns << 250µV
Avec Δv=100µV, durée de la rampe: 25ns * 1V/100µV = 250µs

- Si possible, faire *n* mesures sur chaque palier pour réduire le bruit de $\sqrt{n}$.

4.1.6.2.1 Comments on number of samples to be averaged per transition level for a given confidence level

The precision of the measured values of the code transition levels depends on the total number of histogram samples measured. Increasing the number of samples decreases the uncertainty while ramping the input. The larger the total, the lower the uncertainty. Nonlinearity of the ramp input signal would produce errors in the code transition levels. Noise on the ramp signal or the ADC under test will cause uncertainty in the measured code transition levels. Specifically, the uncertainty in LSBs due to noise in the estimate of a transition level is approximated by Equation (61).

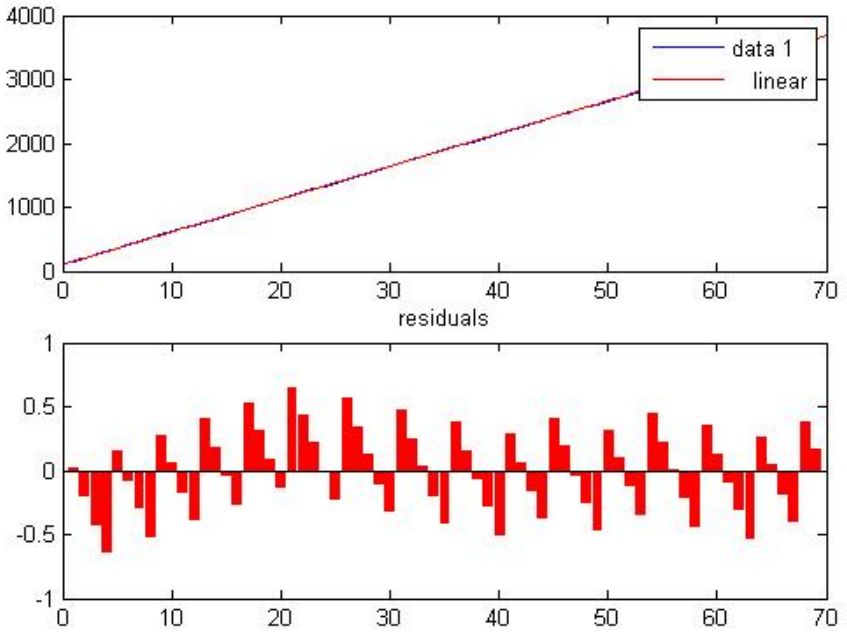
$$\varepsilon \approx \sqrt{\frac{\sigma}{H}} \qquad (61)$$

where

σ is the standard deviation of the noise, in units of ideal code bin widths (LSBs),

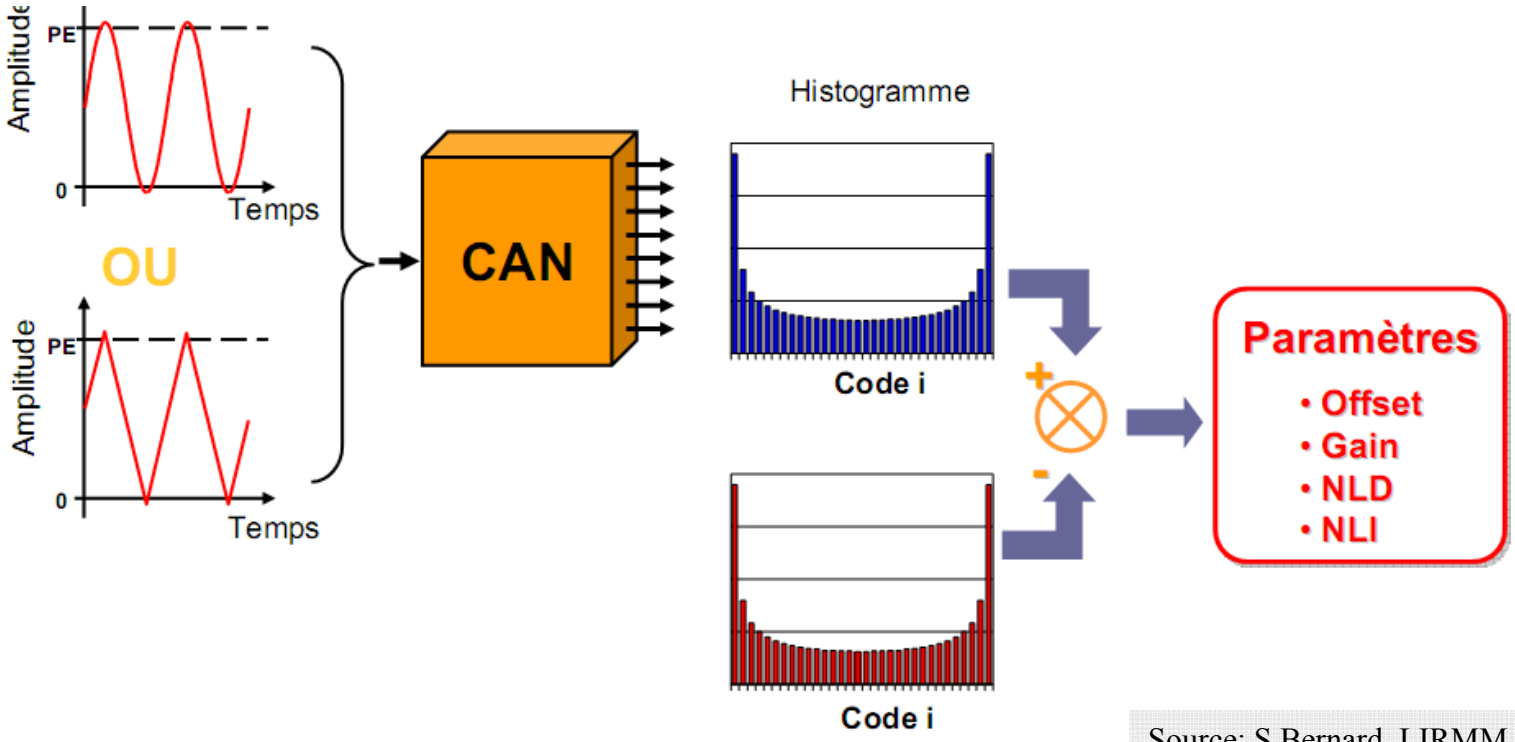
H is the average number of histogram samples received in each of the code bins that share the given transition level.

Source: Norme IEEE [IEEE]



Test par histogramme

- **Principe :**
  - ✓ Signal d'entrée sinusoïdal ou linéaire (triangle, rampe)
  - ✓ Construire l'histogramme expérimental = Fréquence d'apparition des codes de sortie
  - ✓ Comparer cet histogramme avec l'histogramme idéal



Source: S.Bernard, LIRMM [BER]

Test par histogramme

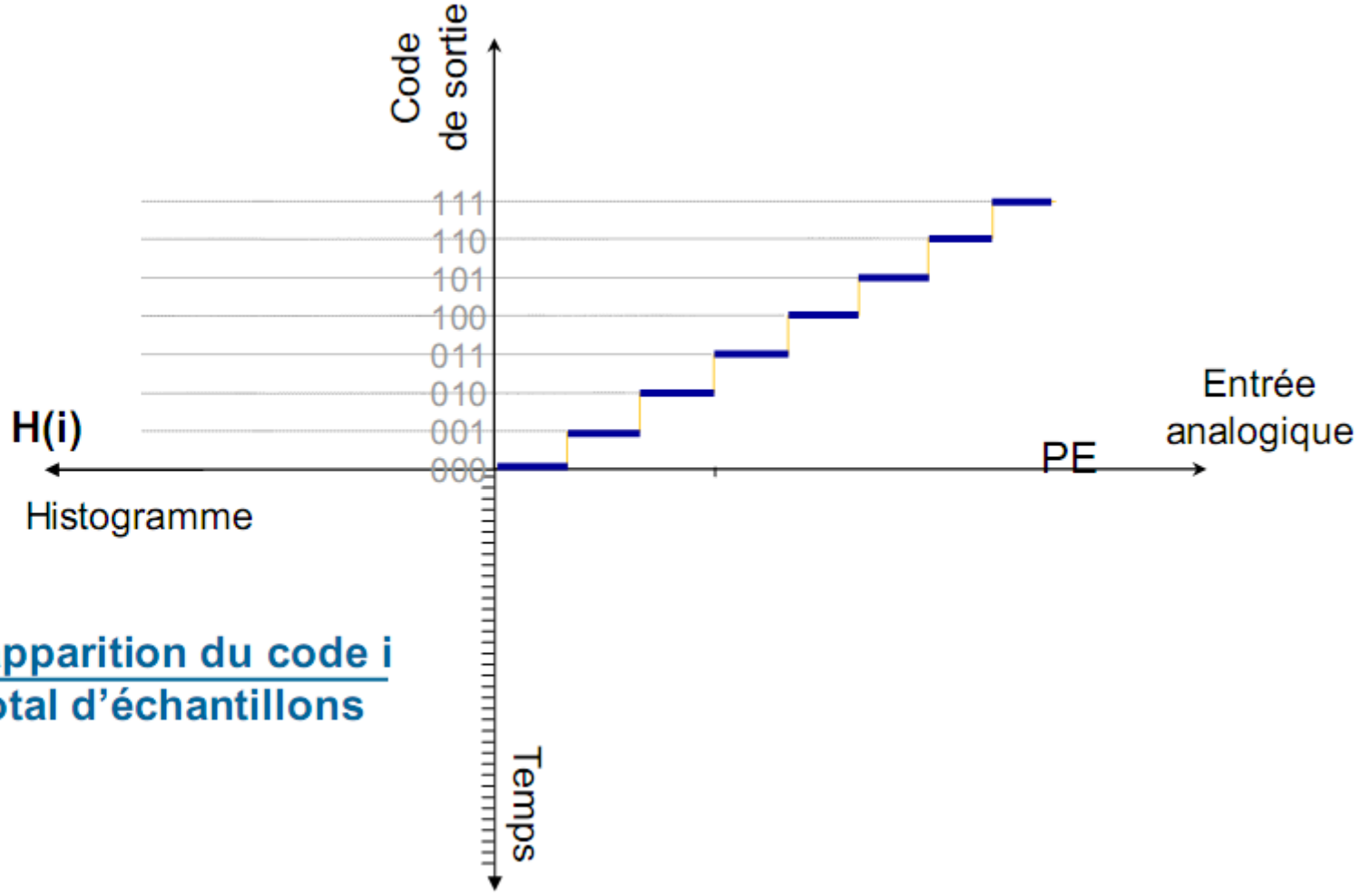
- **Principe :**
  - ✓ Signal d'entrée sinusoïdal ou linéaire (triangle, rampe)
  - ✓ Construire l'histogramme expérimental = Fréquence d'apparition des codes de sortie
  - ✓ Comparer cet histogramme avec l'histogramme idéal

☹ Nombre d'échantillons
☹ Pas de paramètres Dyna.

☺ Précision
☺ Application Indus.

Source: S.Bernard, LIRMM [BER]

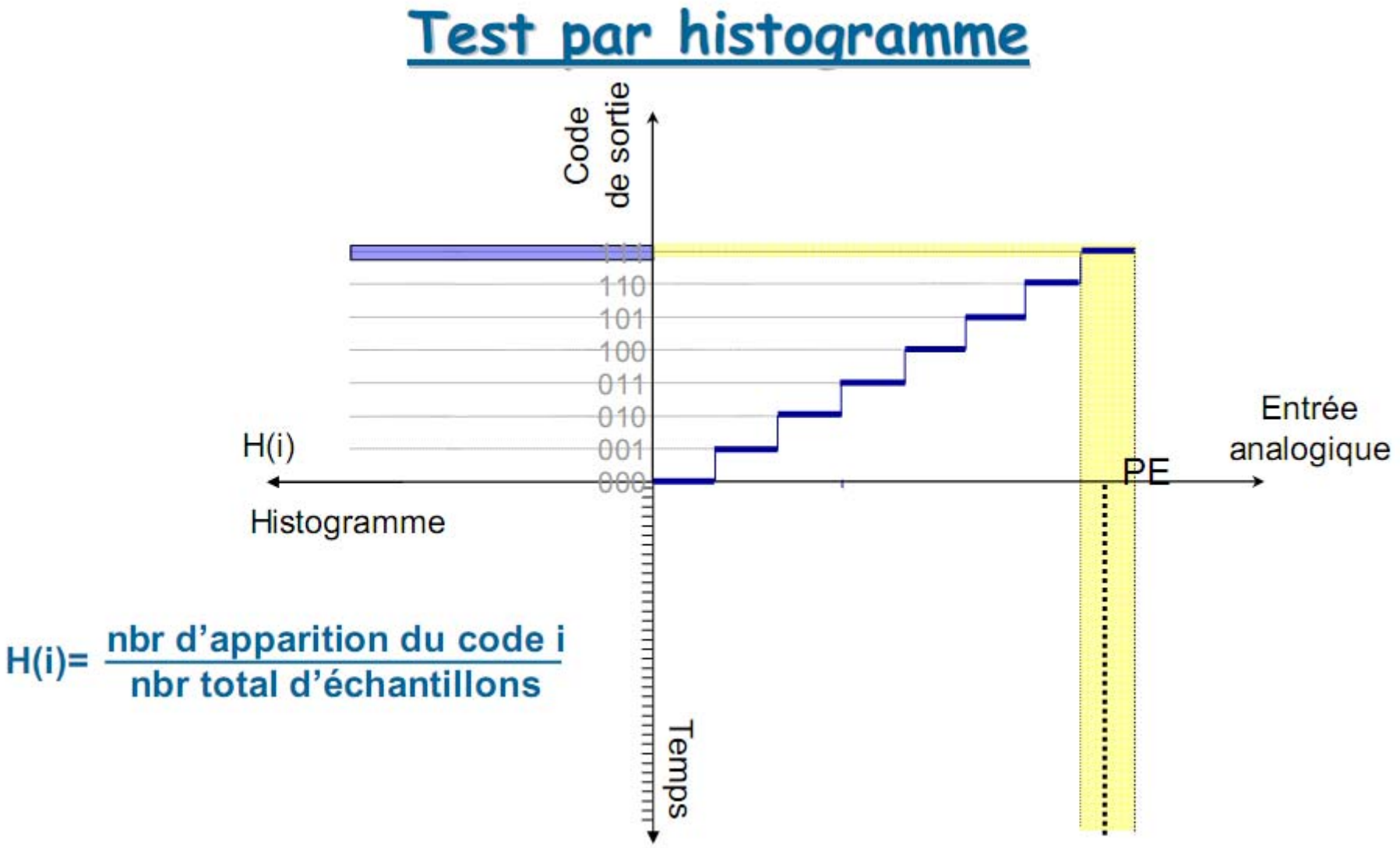
Test par histogramme



$$H(i) = \frac{\text{nbr d'apparition du code i}}{\text{nbr total d'échantillons}}$$

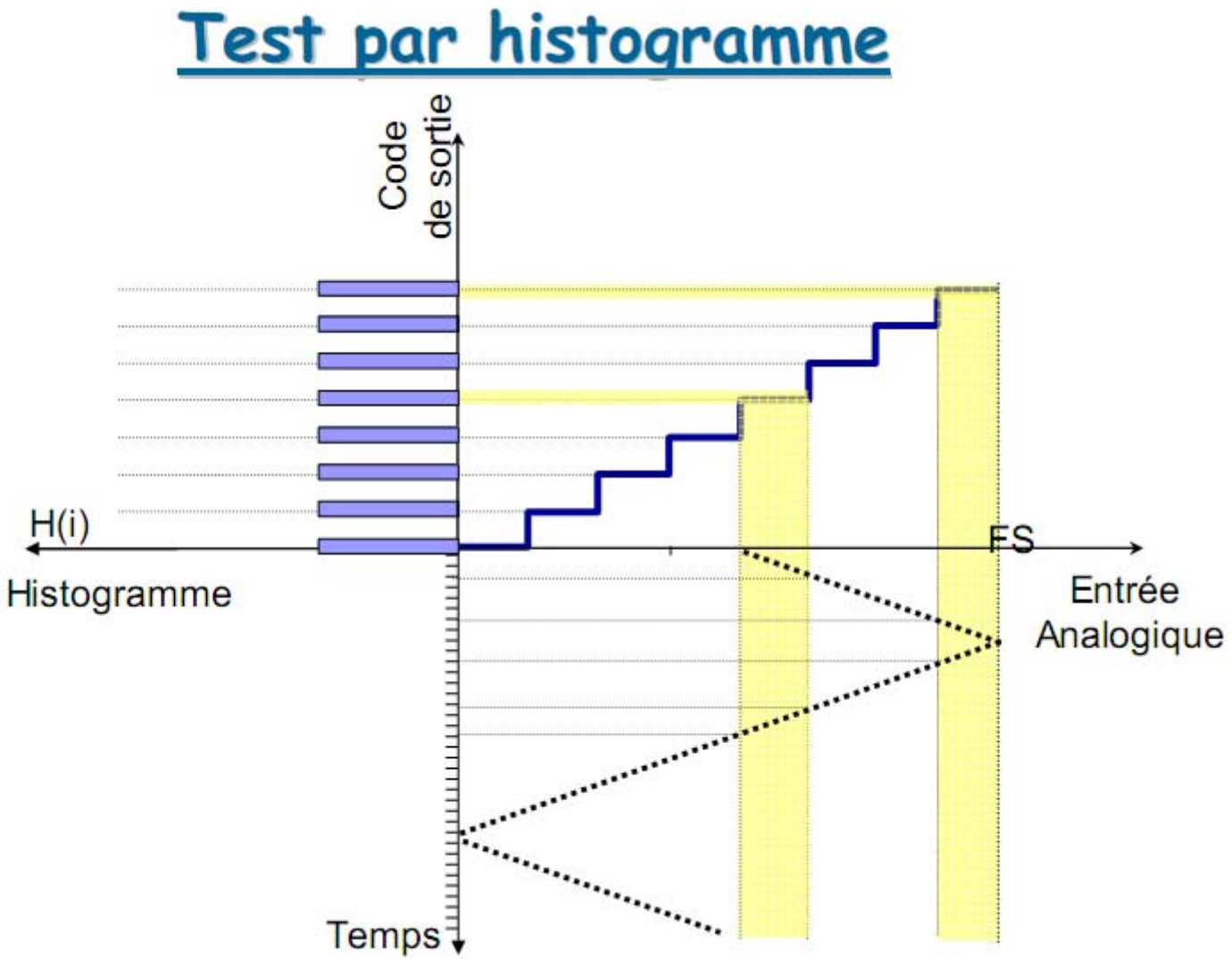
Source: S.Bernard, LIRMM [BER]

Test par histogramme



Source: S.Bernard, LIRMM [BER]

Test par histogramme



Source: S.Bernard, LIRMM [BER]

Test par histogramme

4.1.6.2 Alternate code transition location method based on ramp histogram

In this approach, a histogram of code occurrences is generated in response to an input signal level which ramps linearly between the extremes of the full-scale range of the ADC. After a sufficiently large number of samples [determined from Equation (61)], the histogram of the output provides an accurate measure of the differential nonlinearity of the ADC. Integral nonlinearity can be directly computed by numerically integrating the differential nonlinearity data.

The input ramp should be generated synchronously with the sampling clock, by a high-resolution DAC or arbitrary waveform generator with suitable linearity. Absolute signal level measurements can be made at the terminal codes to compute offset and gain errors. The statistics of this process, as noted in the comments below, can be used to calculate how many hits per bin should be used to achieve a given confidence level based on the equivalent input noise level.

The location of the code transitions, $T[k]$, can be extracted by manipulating the data that is collected in a histogram test with a ramp input. The code transition levels are given by Equation (56)

$$T[k] = C + A \cdot H_c[k-1] \qquad \text{for } k = 1, 2, \ldots, (2^N - 1) \tag{56}$$

where

A is a gain factor,

C is an offset factor,

Source: Norme IEEE [IEEE]

Test par histogramme

$H_\Sigma[j]$ is equal to $\sum_{i=0}^{j} H[i]$,

$H[i]$ is the number of histogram samples received in code bin i,

S is equal to $\sum_{i=0}^{2^N-1} H[i]$ = the total number of histogram samples.

The values of C and A can be computed directly from the collected data and the direct measurement of $T[1]$ and $T[2^N-1]$. The expressions for A and C are given by Equation (57) and Equation (58).

$$A = \frac{(T[2^N - 1] - T[1])}{(S - H[2^N - 1] - H[0])} \quad (57)$$

$$C = T[1] - \left(\frac{H[0] \times (T[2^N - 1] - T[1])}{(S - H[2^N - 1] - H[0])} \right) \quad (58)$$

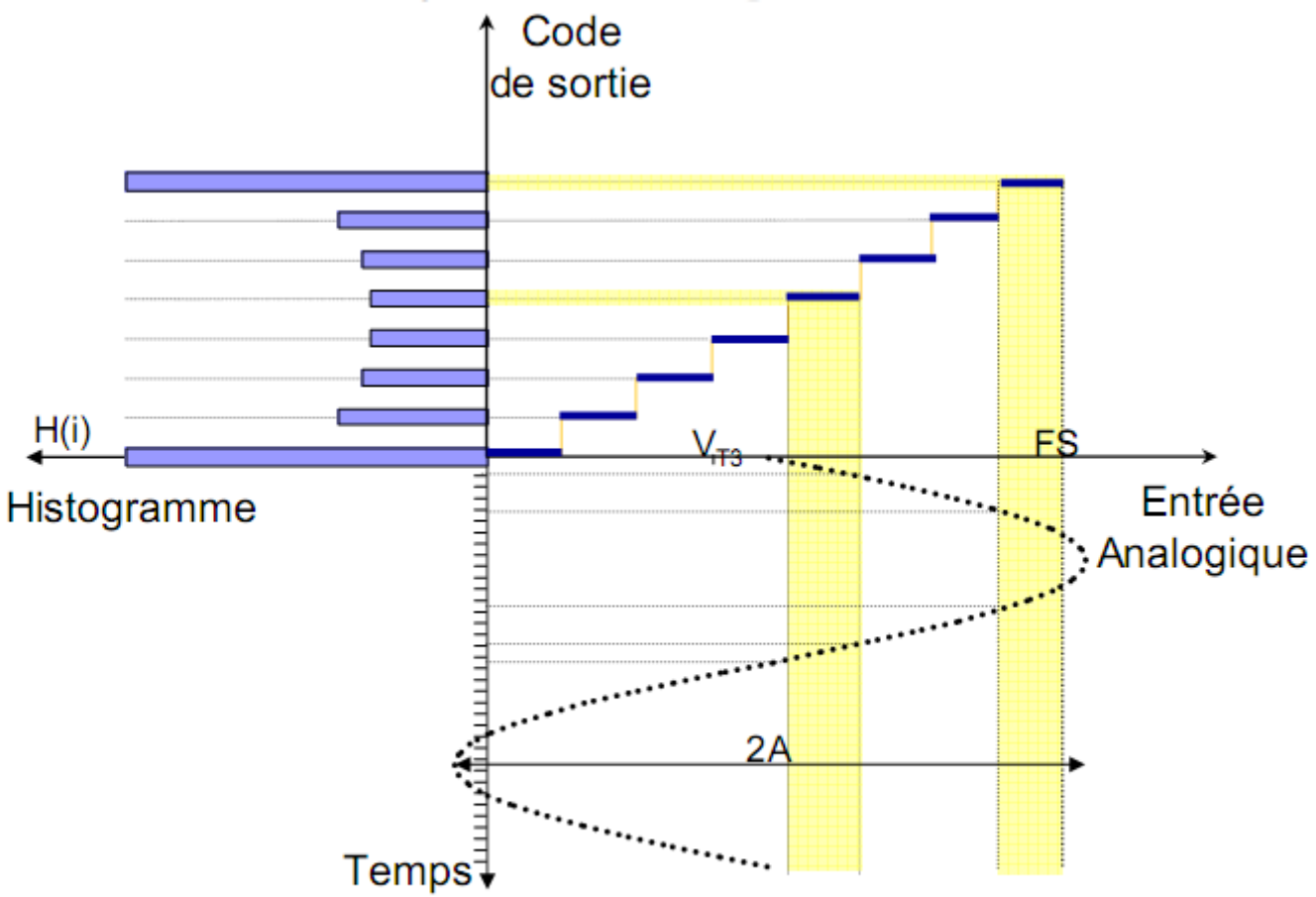
It should be noted that if code bins 0 and 2^N-1 are excluded (defined as having zero width) then the expressions reduce to Equation (59) and Equation (60).

$$A = \frac{(T[2^N - 1] - T[1])}{S} \quad (59)$$

$$C = T[1] \quad (60)$$

Source: Norme IEEE [IEEE]

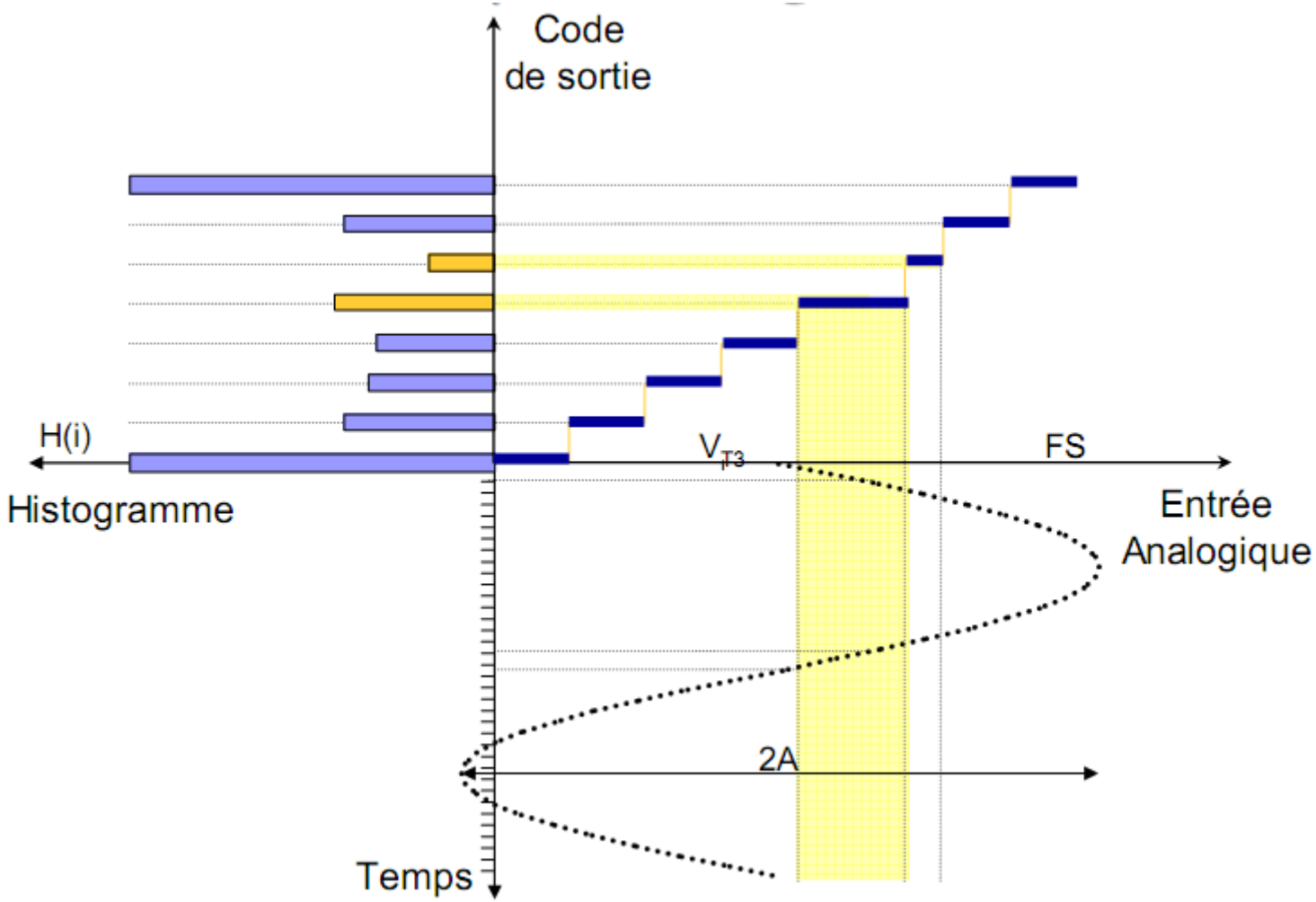
Test par histogramme



$$H^{réf}(i) = \frac{N_T}{\pi}\left(\arcsin\left[\left(\frac{2i-2^n}{2^n}\right)\cdot\frac{PE}{A_{in}}\right] - \arcsin\left[\left(\frac{2i-2^n-2}{2^n}\right)\cdot\frac{PE}{A_{in}}\right]\right)$$

Source: S.Bernard, LIRMM [BER]

Test par histogramme



Source: S.Bernard, LIRMM [BER]

Autres bancs de test

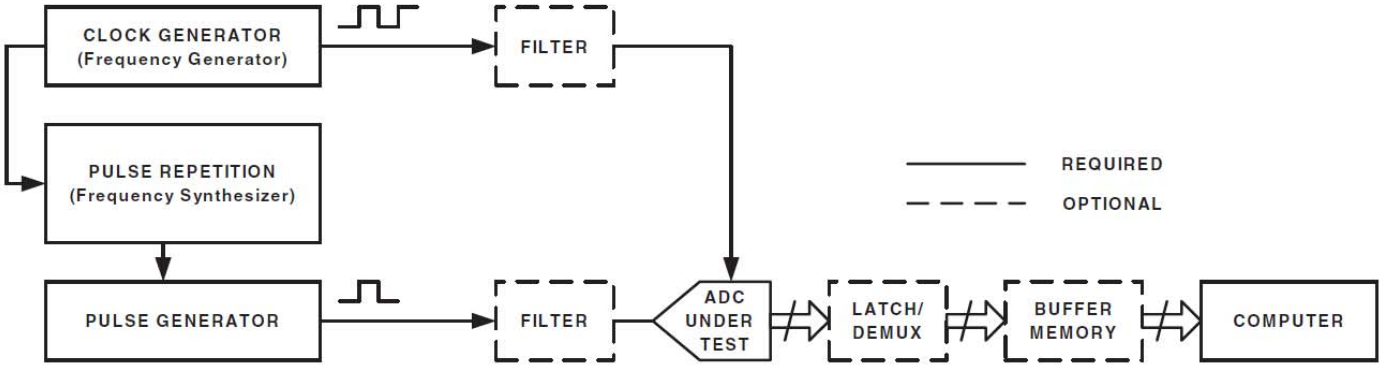


Figure 5—Setup for pulse and step signal testi

Locating code transitions using a feedback loop

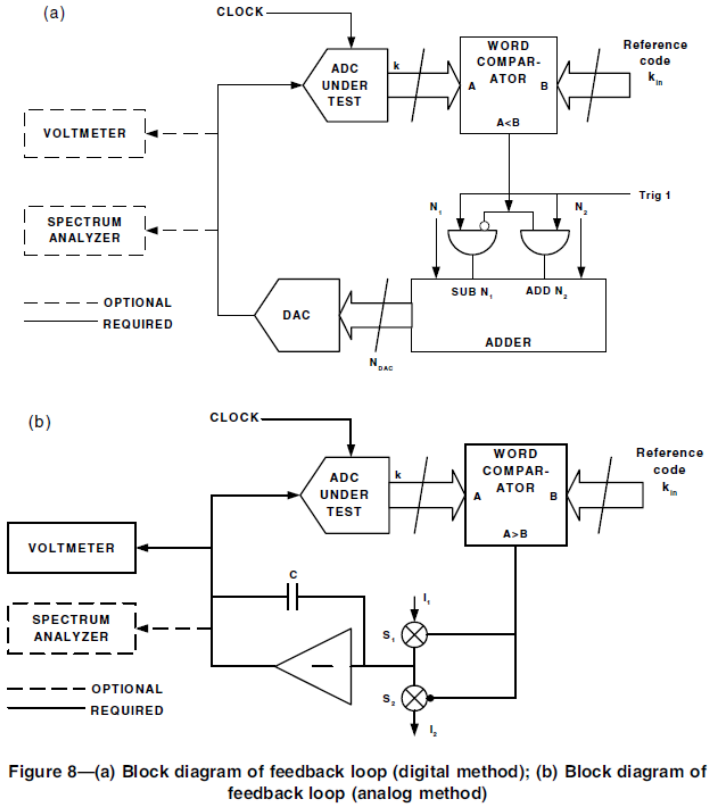
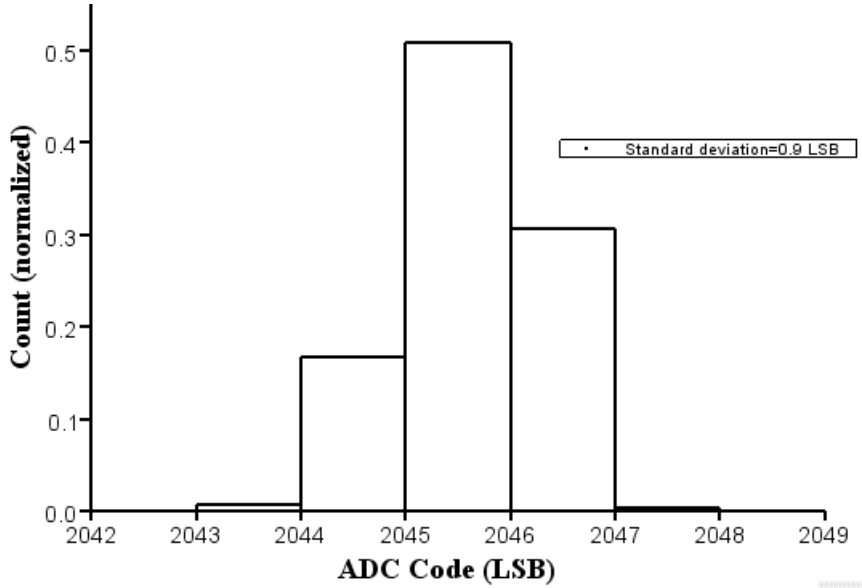


Figure 8—(a) Block diagram of feedback loop (digital method); (b) Block diagram of feedback loop (analog method)

Mesure du Bruit

Méthode utilisée @ LPC-Clt:

- Mettre un signal fixe à l'entrée de l'ADC; filtrer très basse fréquence
- Acquérir les données en sortie de l'ADC
- Tracer l'histogramme de distribution des codes; déterminer la déviation standard
- Effectuer cette mesure pour différentes valeurs de tension d'entrée.
- Cette mesure de bruit peut être réalisée sur toute la gamme avec le test de la rampe et *n* mesures par paliers

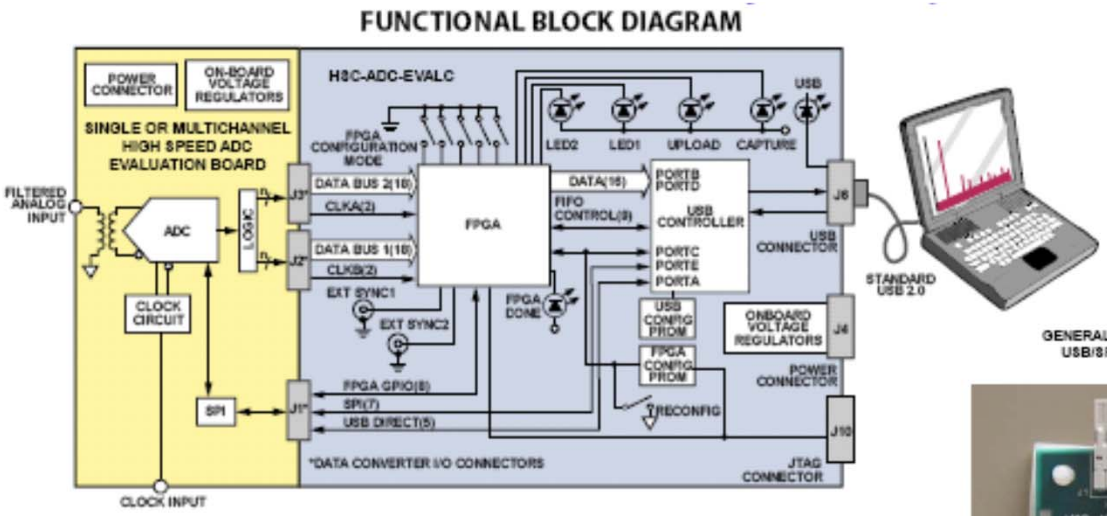


Source: LPC-Clermont

2. Evaluer un ADC:

⇨ des cartes d'évaluation

Exemple de carte d'évaluation: AD



- **1 carte support de l'ADC à tester + 1 carte générique d'acquisition**
- **Logiciel d'analyse/affichage des données: VisualAnalog**

VisualAnalog.exe

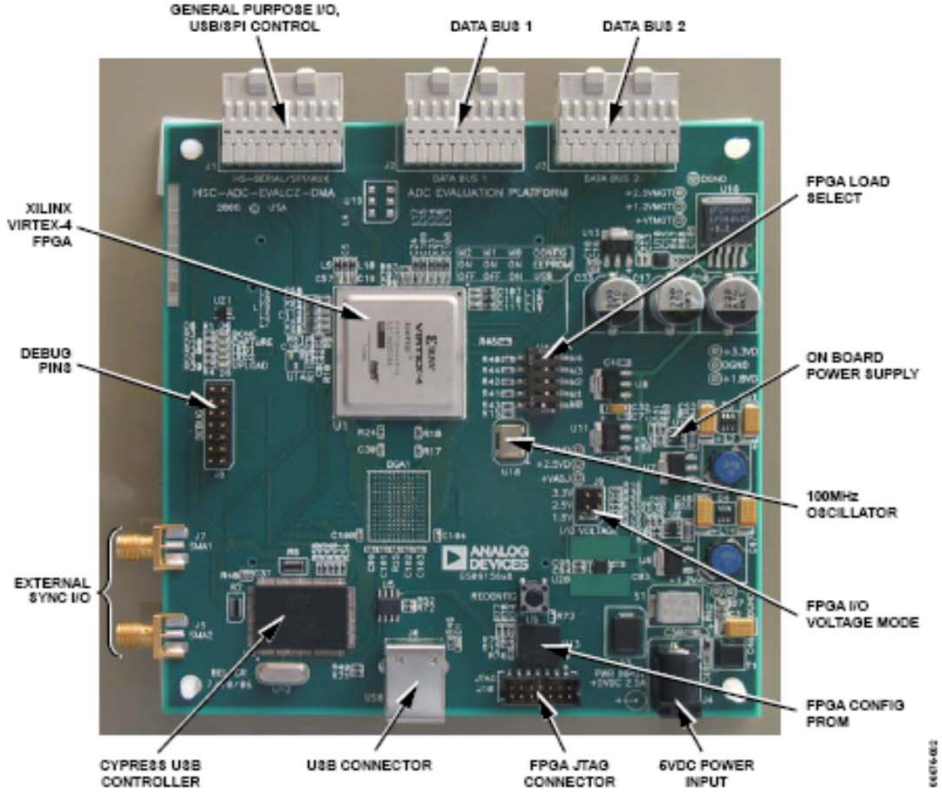


Figure 3. HSC-ADC-EVALC Components (Top View)

Exemple de carte d'évaluation: Linear T. & Maxim

- **Linear Technology: DC718B - QuickDAACS USB Controller for QuickEval-II Evaluation Kits**

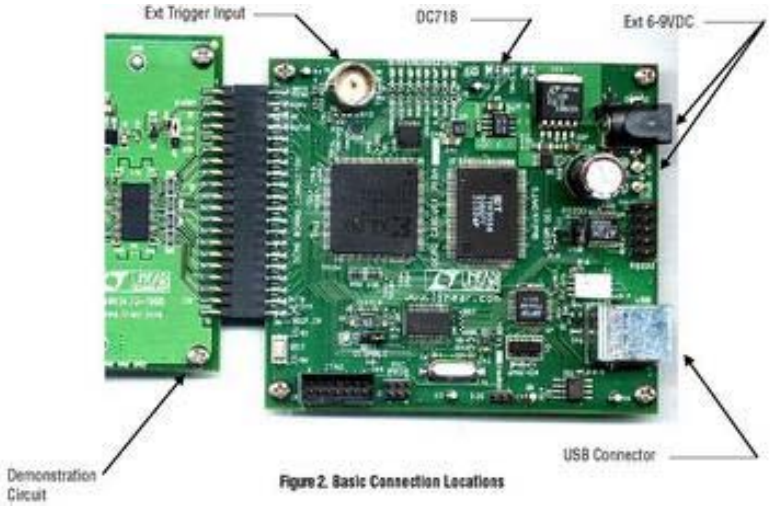
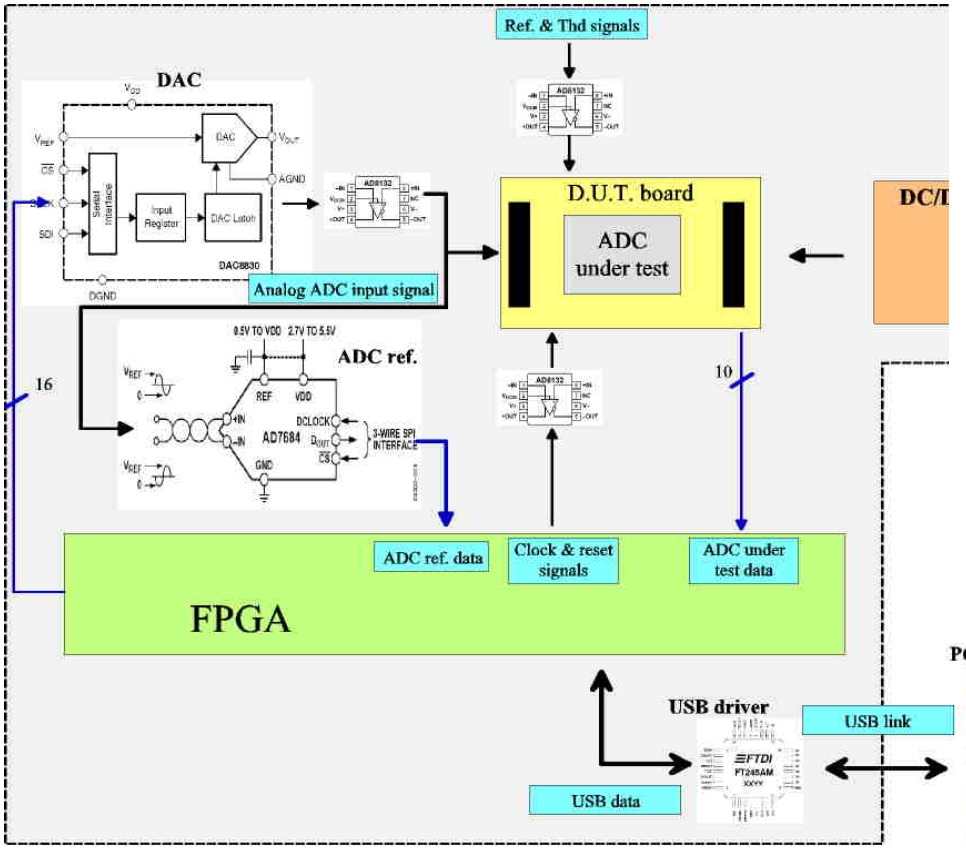


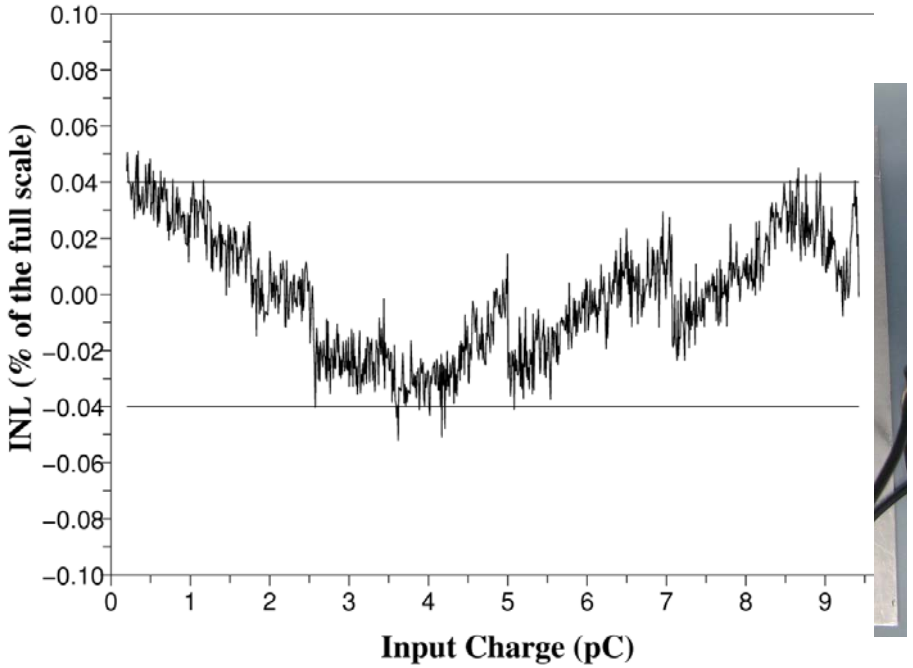
Figure 2. Basic Connection Locations

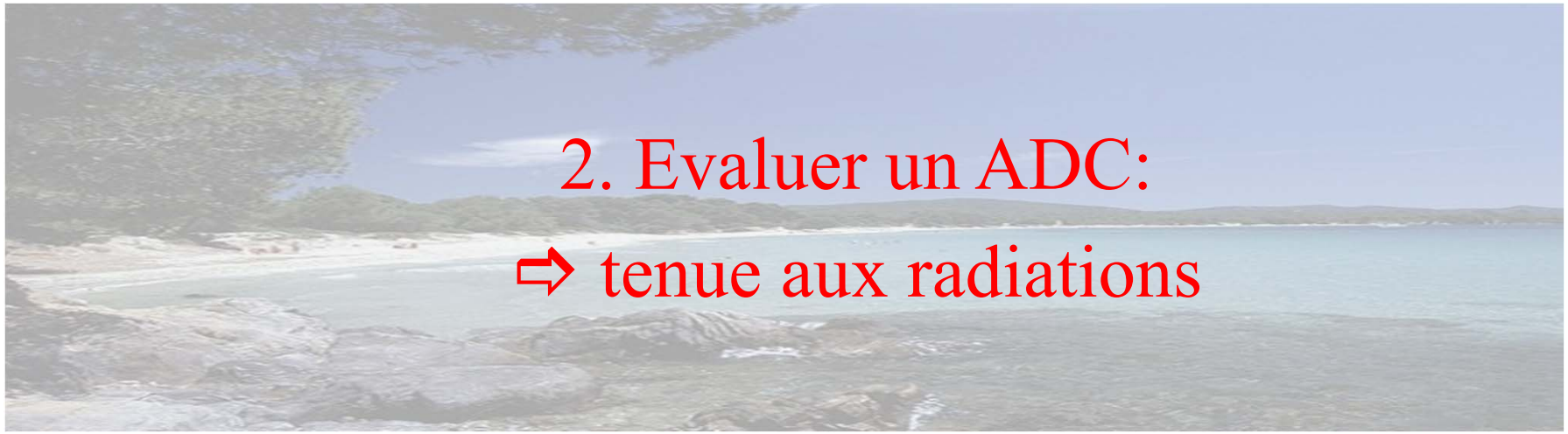
- **Maxim: *68HC16 Module***

Banc de test dédié @ LPC Clermont

- Banc de test générique, piloter par PC/LabView via USB, avec:
  - ADC AD7684 différentiel, 16 bits, 100kS/s → ADC de référence
  - DAC 16 bits + FPGA +USB driver → signal d'entrée type « rampe »







2. Evaluer un ADC:

⇨ tenue aux radiations

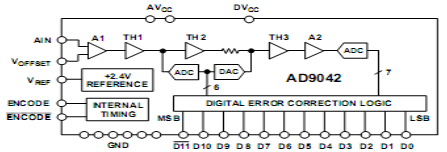
Tenue aux radiations

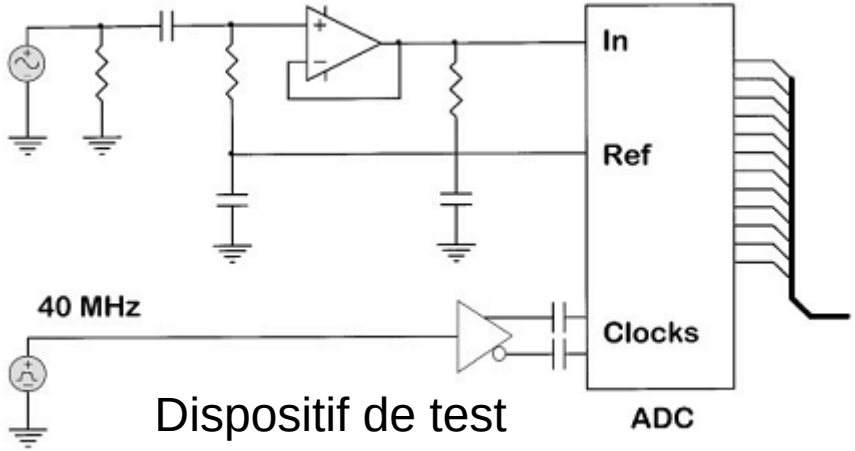
- Les ADC en milieu radiatif sont sensibles:
  - à la dose ionisante:
    - ✓ dérive de la consommation en courant
    - ✓ dérive de la précision
    - ✓ du temps de conversion
    - ✓ de la référence de tension interne
    - ✓ …
  - aux phénomènes de latch-up (SEL: Single Event Latch-up) si la technologie est CMOS (la plus répandue aujourd'hui) ou BiCMOS
  - aux SEU (Single Event Upset)
  - aux SET (Single Event Transient)
  - aux SEFI (Single Event Fonctional Interrupt)

Source: D.Danglan et F.Malou (CNES) [DAN]

Tenue aux radiations: exemple de l'AD9042 (1)

- ADC AD9042 12bits - 40MS/s utilisé pour les calorimètres électromagnétiques d'Atlas et CMS
  - architecture pipeline
  - technologie bipolaire XFCB 1.0 (eXtra Fast Complementary Bipolar).
  - doit tenir à dose jusqu'à 300 krad pour Atlas et 1 Mrad pour CMS
  - Définition avec Analog Devices du processus de test:





Dispositif de test

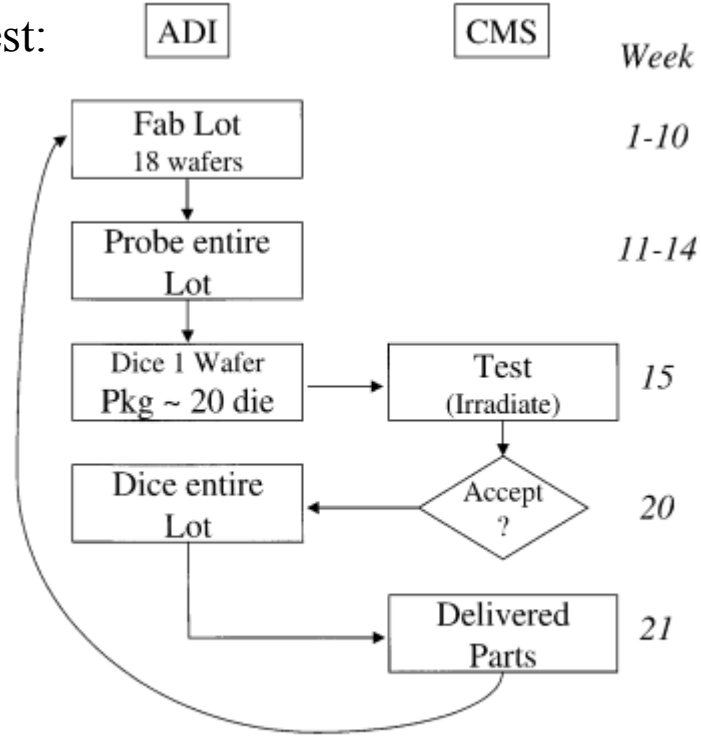


Fig. 1. ADC process flow for CMS.

Source: P.Denes [CMS2]

  - 1 cycle = 21 semaines
  - 32 ADC x 16 wafers = 512 ADC testés

Tenue aux radiations: exemple de l'AD9042 (3)

❑ Mesure du gain

✓ Augmentation de la tension de référence avec la dose → baisse du gain ADC

✓ Utilisation possible d'une référence externe rad-hard et/ou correction off-line

10^{13}p/cm^2 ⇔ 1Mrad

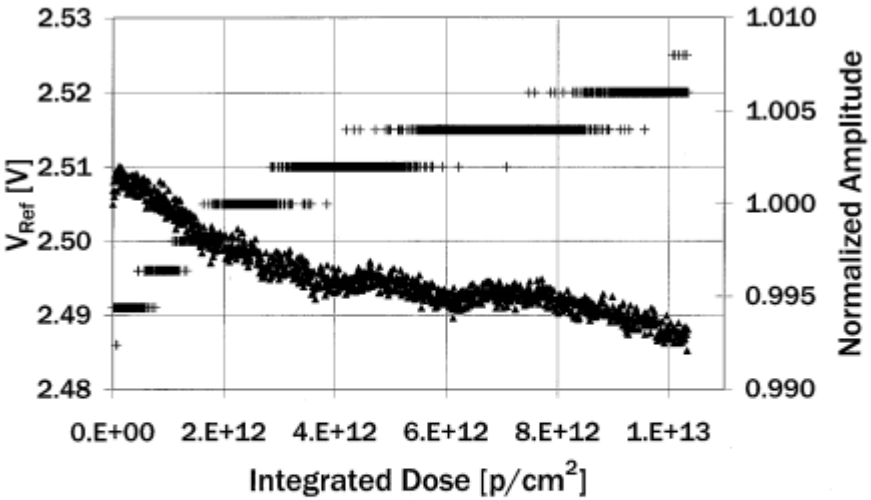


Fig. 7. Amplitude and voltage reference change during irradiation. The crosses indicate the measured value of the ADC voltage reference on the left-hand scale, and the triangles indicate the normalized change in amplitude for a 5 MHz full-scale sine wave on the right-hand scale.

Source: P.Denes [CMS2]

Tenue aux radiations: exemple de l'AD9042 (4)

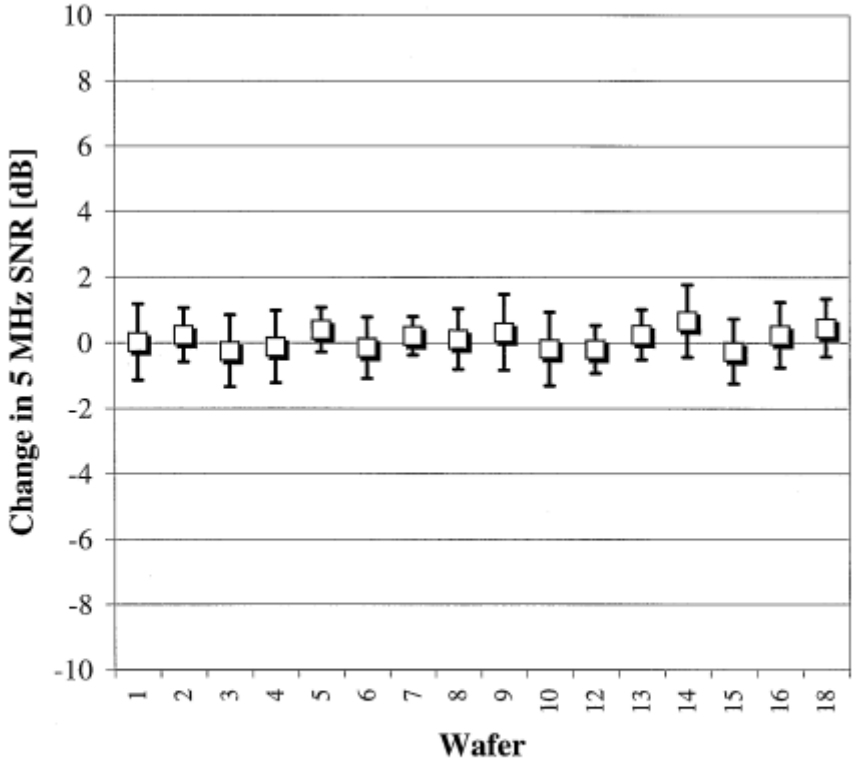


Fig. 5. Change in 5 MHz SNR for ADCs exposed to 10^{12} p/cm^2 as a function of wafer number. The open squares represent the average of the ADCs irradiated, and the error bars the RMS.

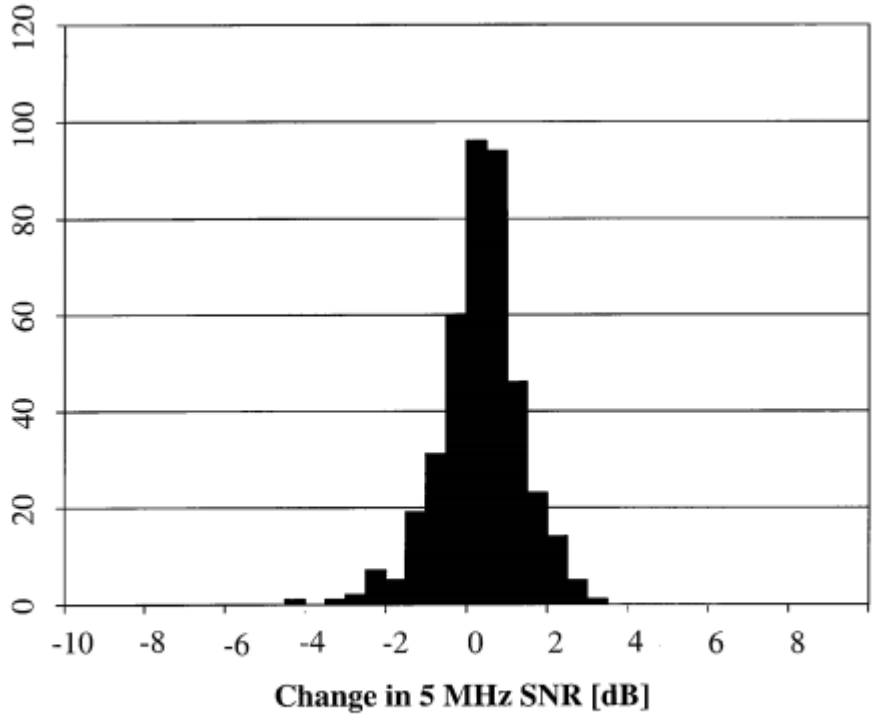


Fig. 6. Change in 5 MHz SNR for all ADCs exposed to 10^{12} p/cm^2, i.e. a histogram of the data in Fig. 5.

10^{13}p/cm^2 ⇔ 1Mrad

SNR moyen mesuré de 63 dB contre 68 dB théorique

➢ système de test à améliorer

Source: P.Denes [CMS2]

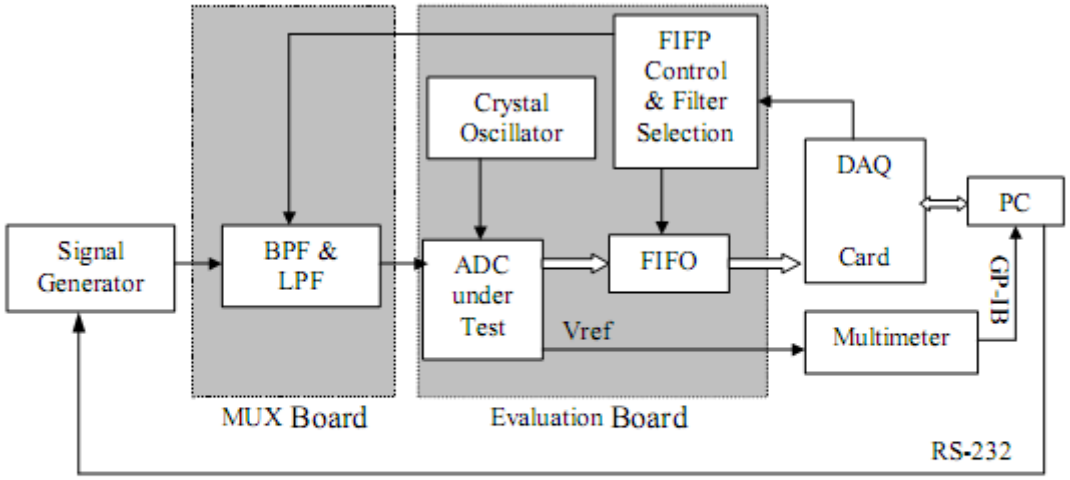
Tenue aux radiations: exemple de l'AD9042 (2)

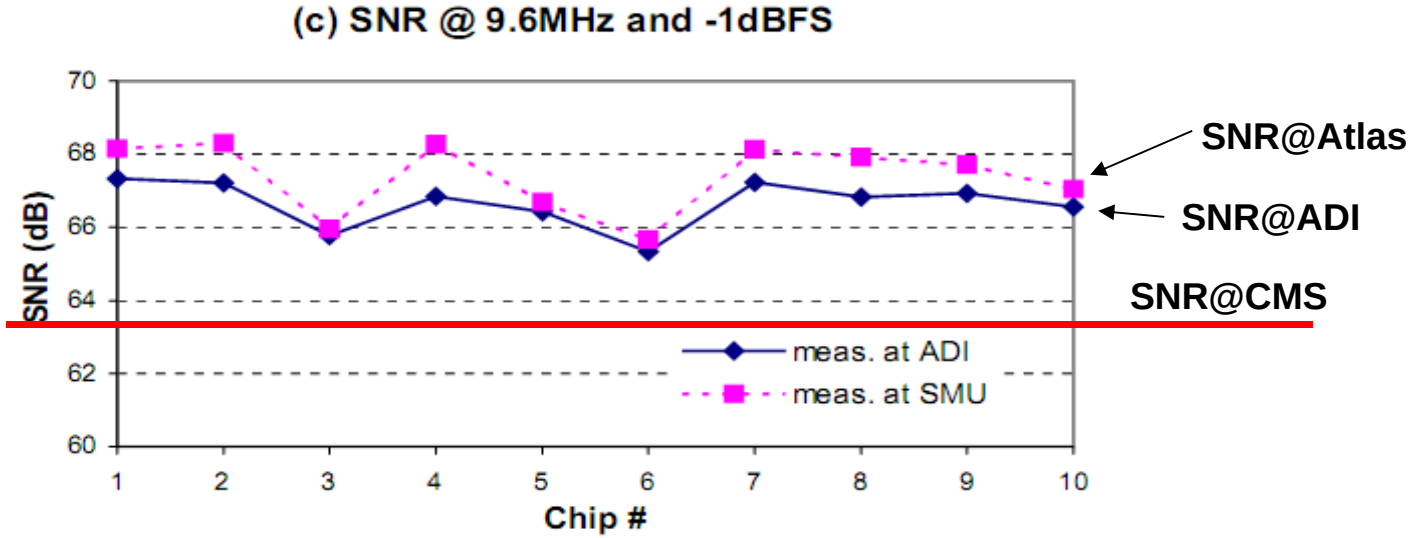
- Mesure du SNR de l'ADC AD9042:
  - le SNR de l'ADC est de 68 dB; le banc de test doit donc être très bas bruit:
    - ✓ signal d'entrée très bas bruit et très faibles harmoniques
      - → générateur Rohde-Schwartz + filtre passe-bande
    - ✓ très faible jitter de l'horloge (4 ps rms: bruit équivalent de 1 LSB)
      - → XO-400 crystal oscillator (Vectron International): jitter de 0.5 ps rms
      - → 1:2 buffer MC10EP11 de On Semiconductor C. jitter de 0.2 ps rms
    - ✓ très bas bruit du PCB et système complet
      - → PCB 4 couches: 1 plan de masse, 1 plan d'alim. divisé en 2 (analog & digital)
      - → support de qualité
      - → connectique SMA

Source: T.Liu et al. [SMU]

Tenue aux radiations: exemple de l'AD9042 (5)

- Amélioration du dispositif de test de circuits :





Exemple d'ADC certifié « spatial »

- ADC AT84AS008 de e2v (ex ATMEL):
  - Principales caractéristiques:
    - ✓ 10 bits – 2.2GS/s – Techno. SiGe
    - ✓ ENOB: 8bits@1.7GS/s, 7.7bits@2.2GS/s
    - ✓ SNR: 51 dB à 2.2G/s
    - ✓ 4,2W/±5V
    - ✓ prix: 1300$/1000 pièces

  - Evaluation spatiale:
    - ✓ évaluation performances entre -55/+125°C et Vcc min et Vcc max
    - ✓ endurance 3000h à 125°C sur 20 pièces
    - ✓ chocs mécaniques et thermiques, vibrations, cycles thermiques
    - ✓ essais en radiations en dose cumulée jusqu'à 150krads à un débit de 50rad/h
    - ✓ essais en radiations sous ions lourds: SEL, SEFI, SEU

Source: e2v [AT84] et D.Danglan/F.Malou (CNES) [DAN]

3. Utiliser un ADC:

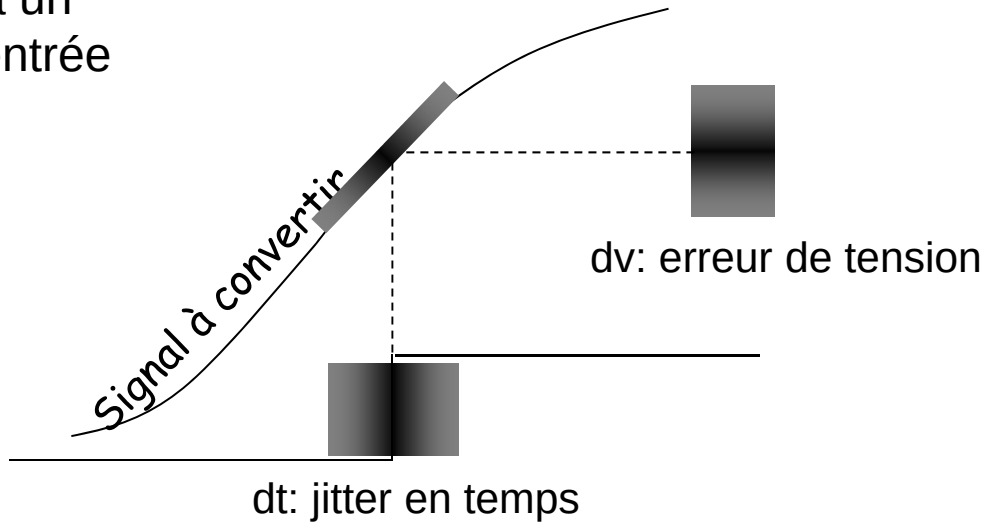
⇨ la fluctuation de l'instant d'échantillonnage

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Définitions

APERTURE (SAMPLING) DELAY: délai de temps entre la commande d'ouverture de l'interrupteur d'échantillonnage et son ouverture effective.

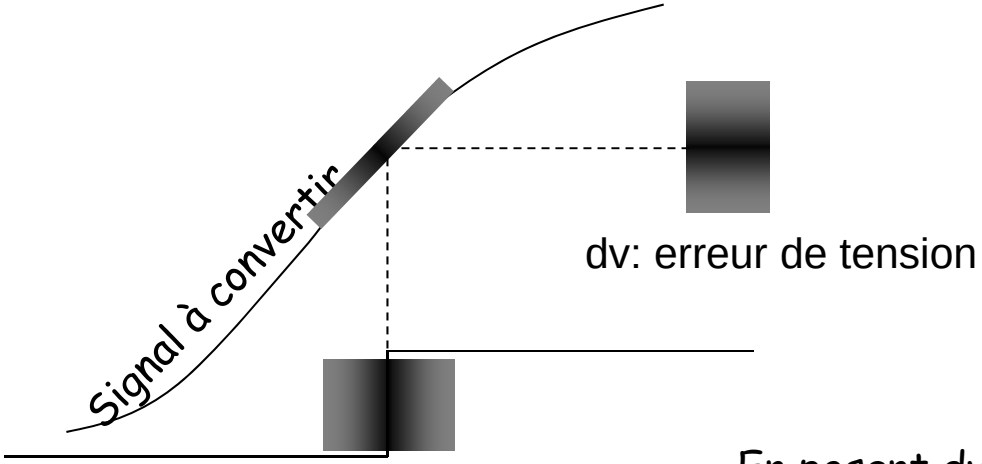
APERTURE JITTER: variation du Apperture delay d'un échantillon à un autre. Cette variation est vue en entrée comme un bruit.



Source: B.Brannon et A. Barlow (AD) [BRA] et J.Lecoq [LEC]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Relation entre l'erreur d'instant d'échantillonnage et l'erreur de tension échantillonnée



Considérons un signal d'entrée v(t) sinusoïdal:

$$v(t) = A\sin(2\pi \cdot f \cdot t)$$

L'erreur de tension est la dérivée en temps:

$$\frac{dv}{dt} = A \cdot 2\pi \cdot f \cos\cdot(2\pi \cdot f \cdot t)$$

L'erreur est max pour cos(2πft)=1 soit t=0:

$$\left.\frac{dv(0)}{dt}\right|_{MAX} = A \cdot 2\pi \cdot f$$

En posant dv = V_{ERR}, l'erreur de tension introduite par la variation de temps dt = t_a est donnée par (valeurs rms) :

$$V_{ERR} = A \cdot 2\pi \cdot f \cdot t_a \quad \text{ou} \quad t_a = \frac{V_{ERR}}{A \cdot 2\pi \cdot f}$$

- L'erreur augmente linéairement avec la fréquence du signal d'entrée.
- L'origine de la fluctuation en temps t_a est le bruit du signal d'horloge.

Source: B.Brannon et A. Barlow (AD) [BRA] et J.Lecoq [LEC]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Détermination de l'erreur d'instant d'échantillonnage maximale acceptable pour un ADC

Soit un signal Vin = A.sinωt converti avec un ADC de résolution N.
L'erreur maximale tolérable est:

$$V_{ERR}\big|_{\max} = \frac{2 \cdot A}{2^N}$$

$$t_a = \frac{V_{ERR}}{A \cdot 2\pi \cdot f} \quad \Rightarrow \quad t_a\big|_{\max} = \frac{V_{ERR}\big|_{\max}}{A \cdot 2\pi \cdot f} = \frac{1}{2^N \cdot \pi \cdot f}$$

Exemples !

L'audio: 20kHz, 16 bits..... Δt=200 ps
La vidéo: 100MHz, 8 bits ..... Δt=12 ps
La Hi-Fi: 20kHz, 20 bits..... Δt=12 ps
NEW audio.....24 bits..... Δt=0,8 ps
Oscillo. 2GHz, 8 bits..... Δt=0,5 ps

Source: B.Brannon et A. Barlow (AD) [BRA] et J.Lecoq [LEC]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Contribution de l'erreur d'instant d'échantillonnage sur le SNR

$$SNR = -20\log\left[(2\pi \cdot f \cdot t_a)^2 + \left(\frac{1+\varepsilon}{2^N}\right)^2\right]^{1/2}$$

contribution du jitter

autres contributions (DNL, bruit quantification, bruit thermique…

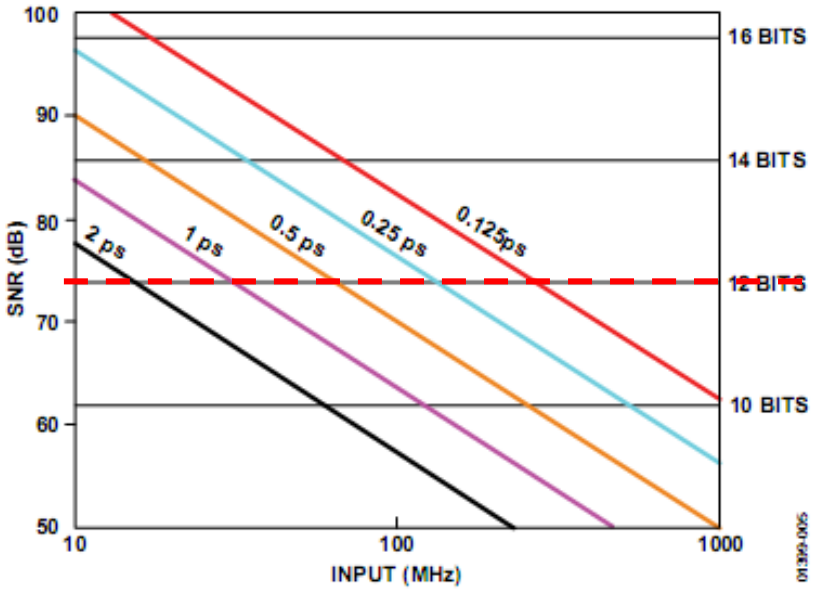


Figure 5. Signal-to-Noise Ratio Due to Aperture Jitter

SNR (dB) max. théorique pour un ADC à N bits (bruit de quantification):

SNR= 6,02 . N + 1,76

soit 74 dB pour un ADC 12 bits

Limite théorique SNR ADC 12 bits

Source: B.Brannon et A. Barlow (AD) [BRA]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Détermination de t_a à partir des mesure de SNR

$$SNR = -20\log\left[\underbrace{(2\pi \cdot f \cdot t_a)^2}_{} + \underbrace{\left(\frac{1+\varepsilon}{2^N}\right)^2}_{}\right]^{1/2}$$

La valeur de t_a peut être évaluée en effectuant 2 mesures de SNR.
Avec f suffisamment bas:

$$SNR\big|_{low\cdot f} \approx -20\log\left(\frac{1+\varepsilon}{2^N}\right)^2 \quad \Rightarrow \quad \varepsilon \approx 2^N \cdot 10^{\frac{-SNR}{20}} - 1$$

A haute fréquence on obtient:

$$t_a = \frac{\sqrt{\left(10^{\frac{-SNR\big|high\cdot f}{20}}\right) - \left(\frac{1+\varepsilon}{2^N}\right)^2}}{2\pi \cdot f}$$

Source: B.Brannon et A. Barlow (AD) [BRA]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Exemple d'évaluation de t_a

- ADC AD9256, 14 bits à 125MS/s
- kit d 'évaluatation Analog Devices

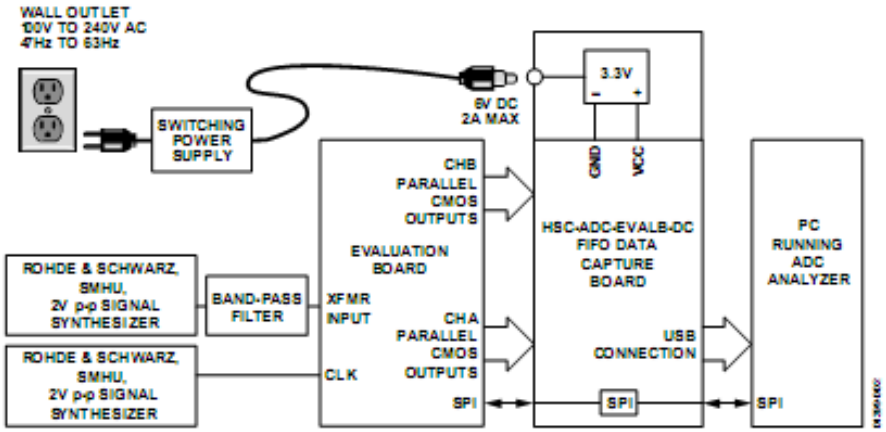


Figure 2. Aperture Uncertainty Measurement Setup with AD9246 Customer Evaluation Board

A partir des 2 mesures on obtient: t_a = 197 fs

Remarque: la valeur obtenue t_a est la somme quadratique des contributions du générateur et de l'ADC lui-même. Si la contribution du générateur est connue, on peut en déduire celle de l'ADC.

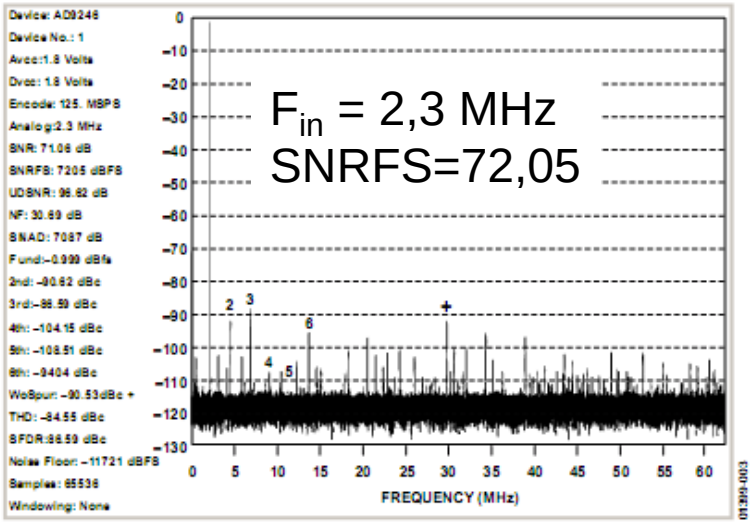


Figure 3. 2.3 MHz FFT

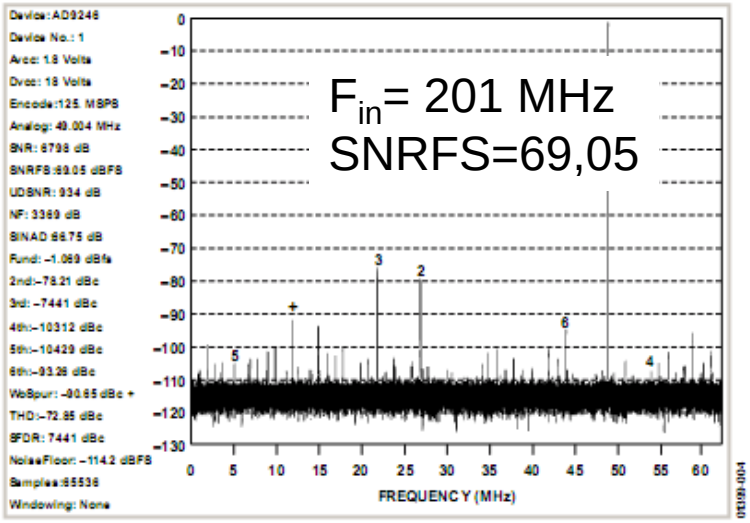


Figure 4. 201 MHz FFT

Source: B.Brannon et A. Barlow (AD) [BRA]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Dégradation du SNR vs aperture jitter

- SNR (dB) max. théorique pour un ADC à N bits (bruit de quantification):

  SNR= 6,02 . N + 1,76 soit 49,9 dB pour un ADC 8 bits

- Dégradation du SNR vs *clock jitter:*

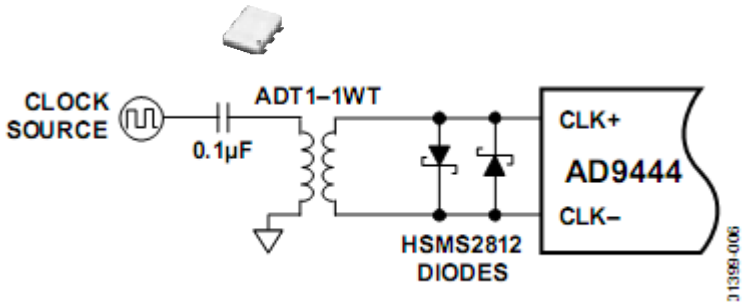
Allowable Clock Jitter (fs.)	Total SNR Due to Quantization Noise and Jitter (dB) $SNR = 10 \log \left(\frac{1}{\frac{1}{10^{\frac{SNR_J}{10}}} + \frac{1}{10^{\frac{SNR_Q}{10}}}} \right)$
142	48.5
259	48.2
354	47.8
447	47.4
541	46.9
640	46.4
747	45.8
862	45.2
989	44.5

Source: J.Catt (NS) [CATT]

Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Mise en œuvre de l'horloge

- Signal d'horloge sinusoïdal différentiel
  - recommandé pour ADC rapide
    - ✓ jitter réduit par rapport signal logique
    - ✓ utilisation de transformateur RF « balun » pour distribution de l'horloge
    - ✓ adaptation d'impédance interne



- Signal d'horloge logique différentiel
  - LVDS jusqu'à 1,5 GS/s ADC rapide (ADC081500 de NS)
  - adaptation d'impédance interne
  - routage sensible des signaux
  - attention au distribution d'horloge
  - utilisation de circuit dédié type AD9510 (jitter 350 fs)

Table 1.

Gate Type	Jitter
FPGA[1]	33 to 50 ps
74LS00	4.94 ps
74HCT00	2.20 ps
74ACT00	0.99 ps
MC100EL16 (PECL)	0.70 ps
AD9510 Clock Synthesis and Distribution	0.22 ps
NBSG16 (Reduced Swing ECL)	0.20 ps

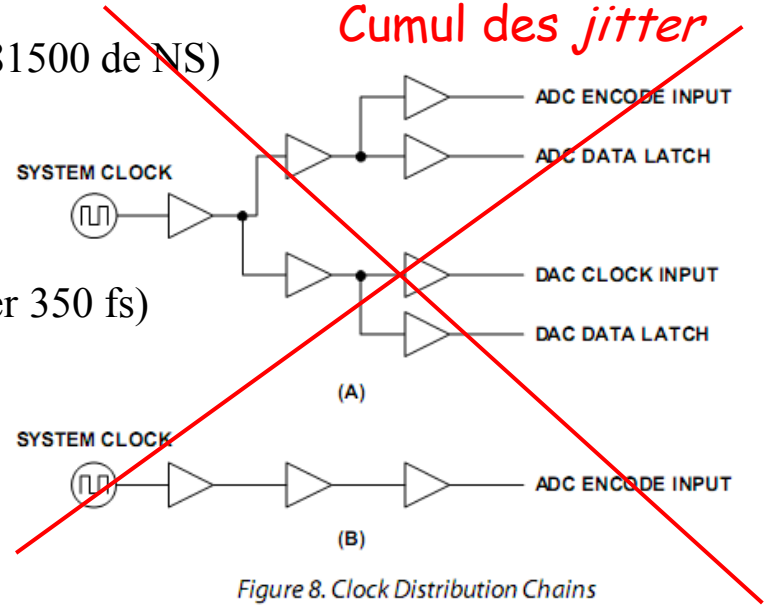


Figure 8. Clock Distribution Chains

Source: B.Brannon et A. Barlow (AD) [BRA] & J.Catt (NS) [CATT]

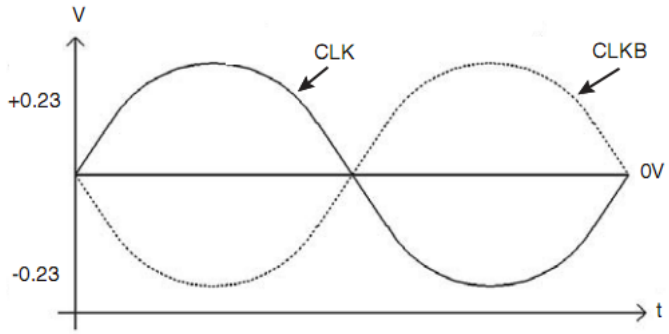
Fluctuation de l'instant d'échantillonnage (Aperture jitter)

Mise en œuvre de l'horloge

- Exemple: ADC AT84AS008 de e2v (Atmel)
  - 10 bits – 2,2 GS/s
  - Extrait datasheet:

Typically, using a sinewave oscillator featuring –135 dBc/Hz phase noise, at 20 KHz from carrier, a global jitter value (including ADC + generator) of less than 200 fs RMS has been measured. If clock signal frequency is at fixed rates, it is recommended to narrow band filter the signal to improve jitter performance.

Figure 8-5. Differential Clock Inputs (Ground Common Mode): Recommended



dBc: in telecommunications, this indicates the relative levels of noise or sideband peak power, compared to the carrier power.

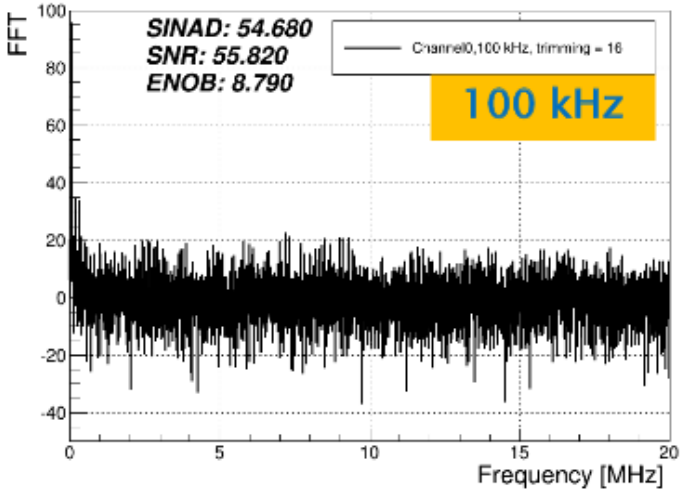
Source: e2v [AT84]

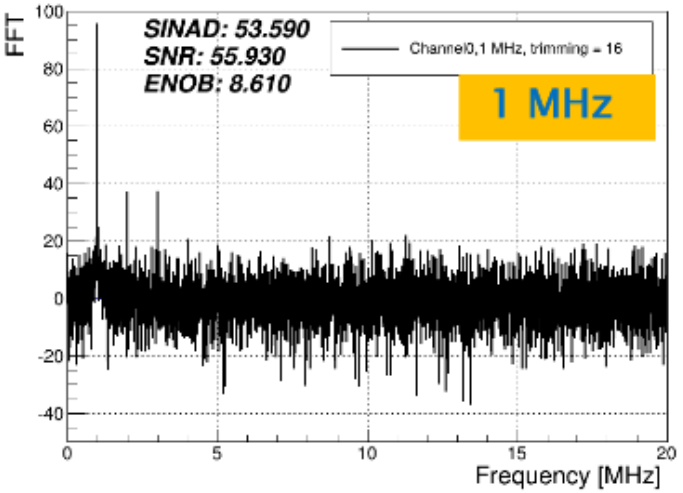
Chercher l'erreur ??

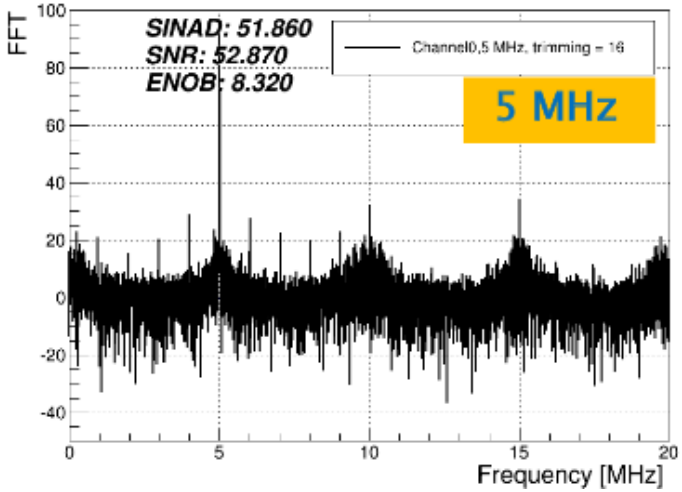
https://indico.in2p3.fr/getFile.py/access?contribId=26&resId=0&materialId=slides&confId=9825

Dynamic specifications

- Dynamic performance of the ADC are determined from the FFT for an incoming sinus signal: 100KHz, 1MHz and 5MHz
- These results integrate all the limitations:
  - Reduce dynamic range
  - Spikes
  - Jitter (next slides)





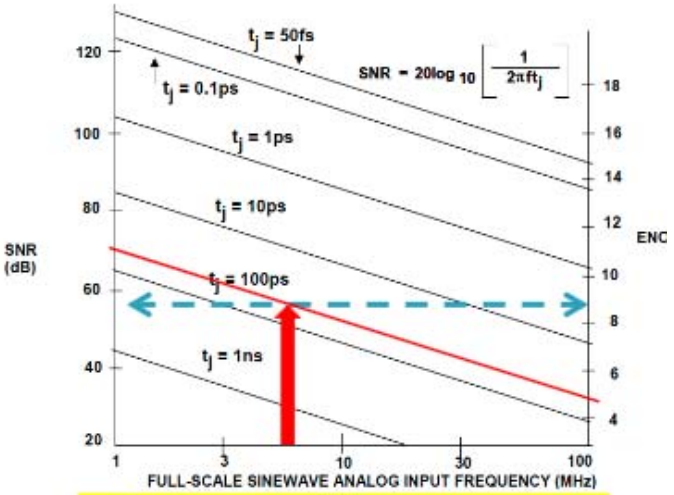


Chercher l'erreur ??

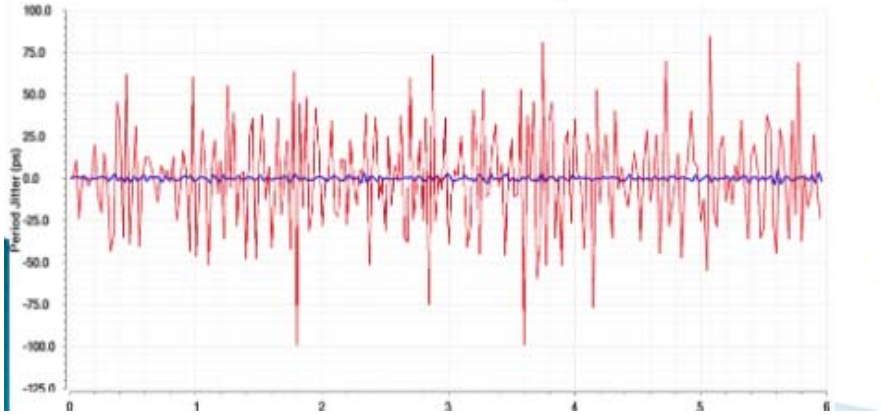
https://indico.in2p3.fr/getFile.py/access?contribId=26&resId=0&materialId=slides&confId=9825

ENOB: Source & Solutions

- Source of ENOB reduction
  - ➔ sampling clock jitter
    - 1 to10 ps jitter is needed to reach expectations
    - Simulation studies of 2nd prototype:
      - RMS jitter **30 ps** or ±100 ps peak to peak
- Solution:
  - Modifying the architecture of the sampling pulse generator inside the chip



Theoretical limitations as a function of jitter



Present problem for jitter
New jitter simulated

3. Utiliser un ADC:
⇨ la CEM

Quelques notions de CEM

Quelques conseils d'un experts CEM: Alain Charoy AEMC en 2005

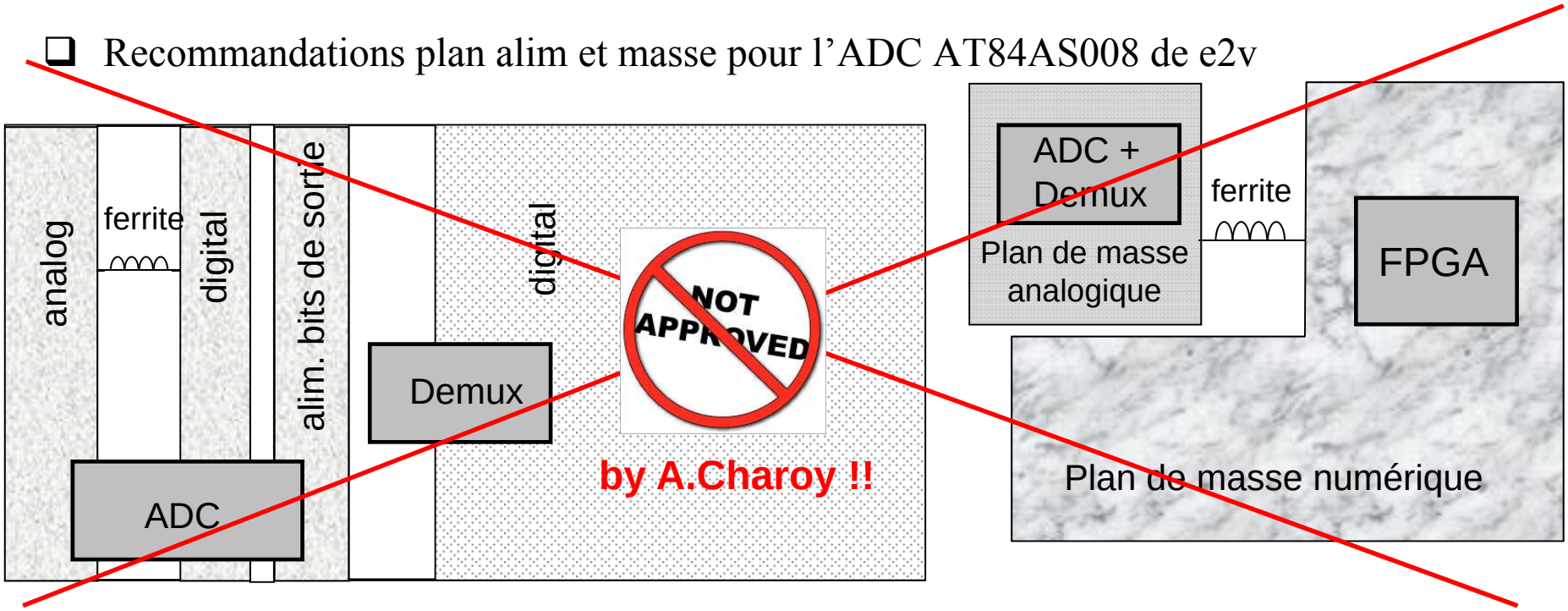
« Méfions-nous à priori des data-sheets !... »

- « Un **plan de masse** non fendu sous le convertisseur est souhaitable !
  (fente de 1cm ⇨ self ≈ 1nH) »
- « Le bruit des ADC est minimal quand AGND, DGND, REF, COM, … et capas de découplage de +Vcc et –V directement au plan 0V ! »
- « Pour permettre une conversion stable […] alimenter la partie analogique via la partie numérique. »
- « Le timing d'un convertisseur rapide est essentiel: sur un signal à 10MHz, un jitter de 10 ps génère une erreur dynamique d'une amplitude supérieure au LSB d'un ADC 12 bits. »
- « La broche d'entrée d'un échantillonneur-bloqueur injecte des charges à chaque commutation. Pour une conversion à fréquence élevée, un amplificateur rapide et stable (tel un driver vidéo par ex.) est nécessaire. »
- « Limiter les capacités des sorties numériques (ajouter des résistances série ≈ 68Ω ou un buffer « calme » pour réduire le « ground bounce »). Pour un convertisseur lent, une interface de sortie série est conseillée. »

Source: Charoix, AEMC [CHAR99] [CHAR05]

PCB pour ADC rapides

- Recommandations plan alim et masse pour l'ADC AT84AS008 de e2v

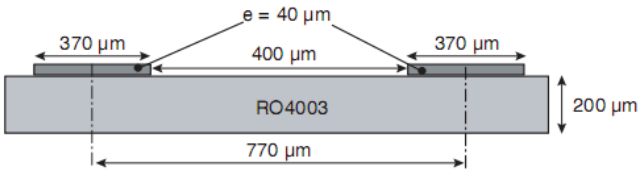


Board Layout Recommendations

It is necessary to ensure that all the lines at the input and output of the ADC are matched to within 2 mm. As all data lines are differential, it is also necessary that each line of a differential pair is matched in length within 1 mm.

Figure 5-3 gives the layout rule used on RO4003 for differential signals.

Figure 5-3. 50Ω Matched Line on R04003 Layout (Differential Signal)



Source: App. note e2v [e2v]

Filtrage/découplage des alimentations

- Même soin de séparation et de découplage des alims à l'intérieur même des circuits intégrés

ADC AT84AS008

112 pins sur 148 pour alim !!

Figure 5-1. AT84AS008 Pinout of CBGA152 Package (Bottom View)

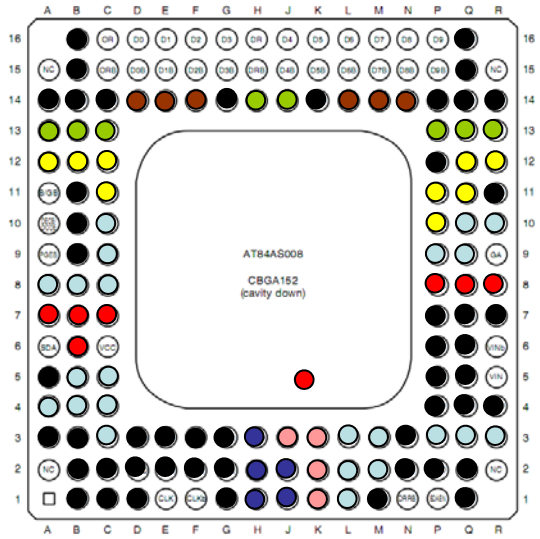
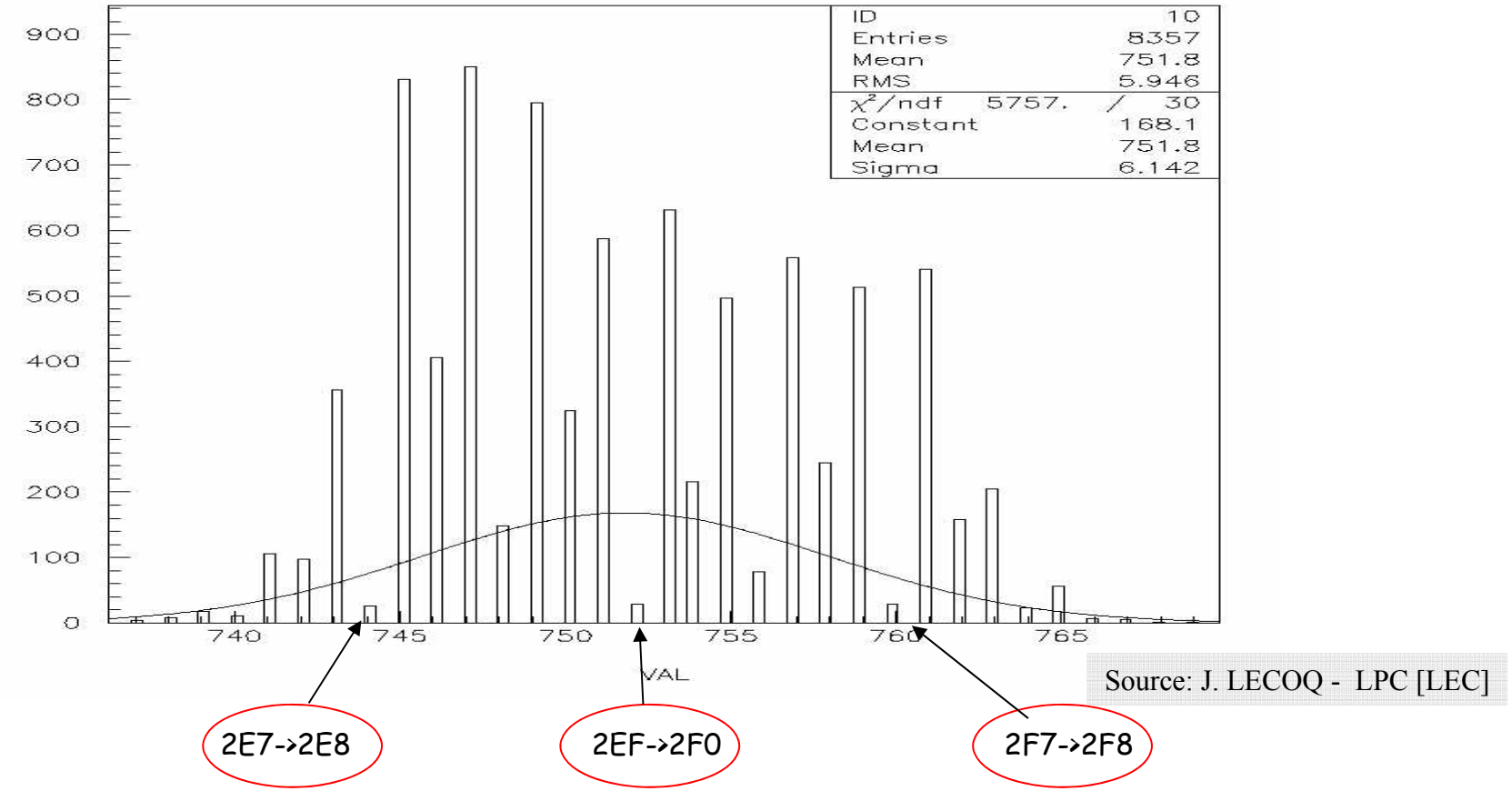


Table 5-1. AT84AS008-EB Pin Description

Symbol	Pin Number	Function
Power Supplies		
V_{CC}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	+5V analog supply
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analog ground
V_{EE}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	-5V analog supply
V_{PLUSD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
DV_{EE}	A13, B13, C13, P13, Q13, R13, H14, J14	-5V or -2.2V digital supply

Gestion des alimentations: le mauvais exemple

- ASIC: ADC à rampe
- Alim. analogique et numérique communes dans la puce
  - di/dt alim numérique ➔ dv/dt alim. analogique ➔ Codes de sorties erronés lors du changement d'états simultanés de plusieurs bits
  - Intérêt du compteur Gray (un seul changement d'état à la fois)

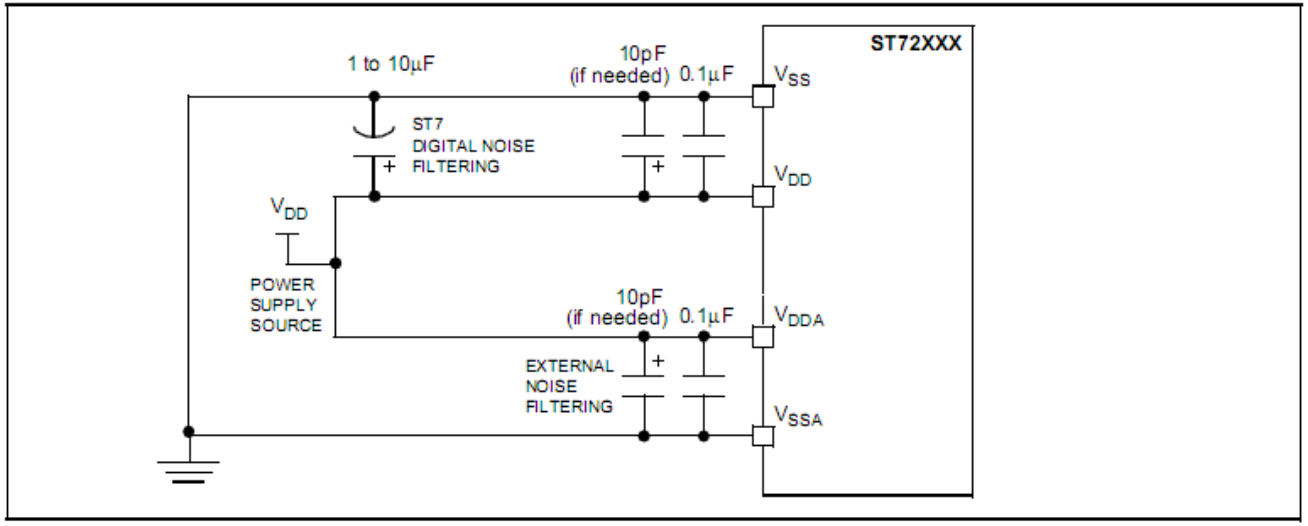


Source: J. LECOQ - LPC [LEC]

Filtrage/découplage des alimentations: rappels

- Exemple recommandations de ST Micro.

Figure 14. Power supply filtering



The capacitors allow the AC signals to pass through them. The small value capacitors filter high frequency noise and the high value capacitors filter low frequency noise. Ceramic capacitors are generally available in small values (1pf to 0.1 µf) and small voltages 16V to 50V. It is recommended to place the ceramic capacitors close to the main supply pins (V_{DD} & V_{SS} and analog supply pins (V_{DDA} & V_{SSA}). These filter the noise induced in the PCB tracks. Small capacitors can react fast to current surges and discharge quickly for fast current requirements. Tantalum capacitors can also be used along with ceramic capacitors.

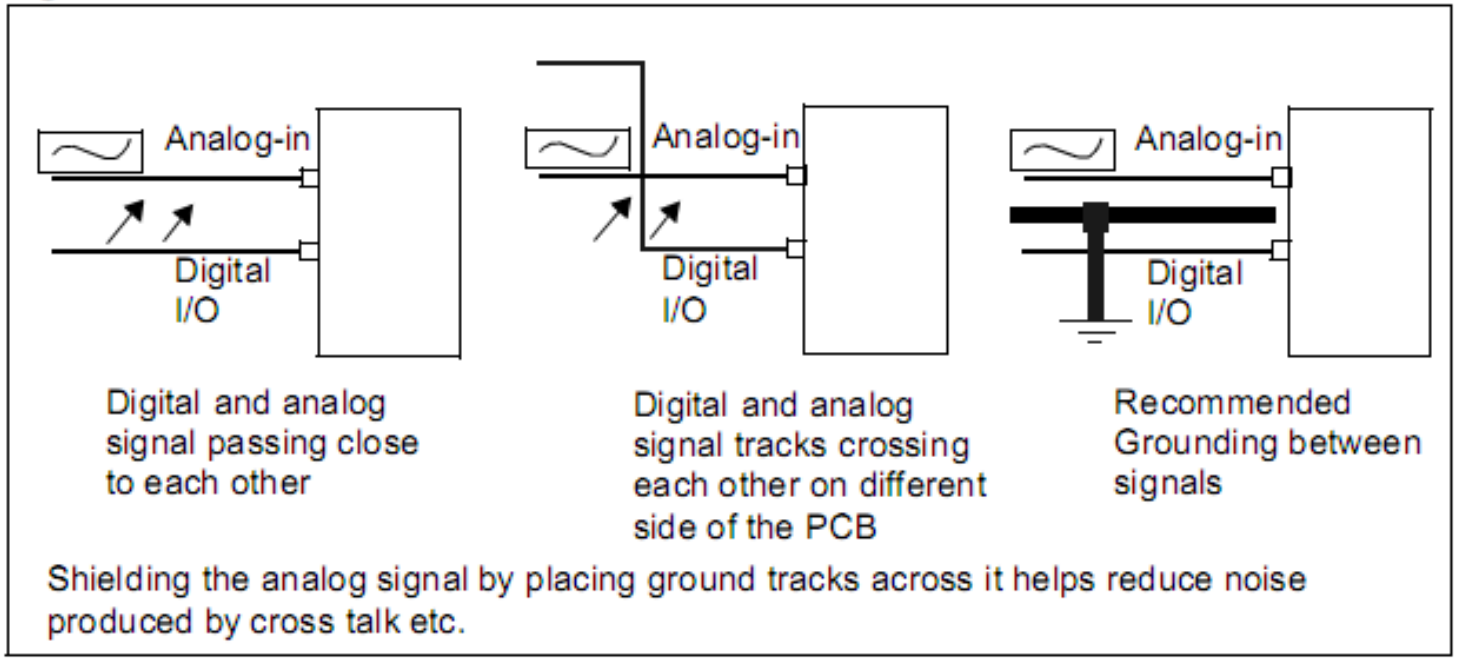
High value capacitors (10µf to 100µf) which are generally electrolytic, you can use them to filter low frequency noise. It is recommended to put them near the power source. You can also filter high frequency noise using a ferrite inductance in series with the power supply. Ferrites cause low DC loss (negligible) unless the current is high. This is because the series resistance of the wire is very low. But for high frequency, the impedance offered is high.

Source: App. note ST [AN1636]

Rappel: séparation des signaux analogiques et numériques

Analogique et numérique: une cohabitation difficile

Figure 22. Cross-talk between I/Os



Source: App. note ST [AN1636]

3. Utiliser un ADC:

⇨ l'impédance d'entrée

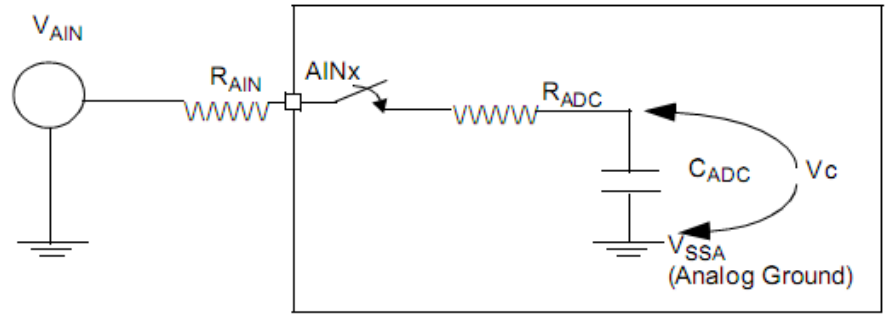
Temps de charge de la capa C_{ADC}

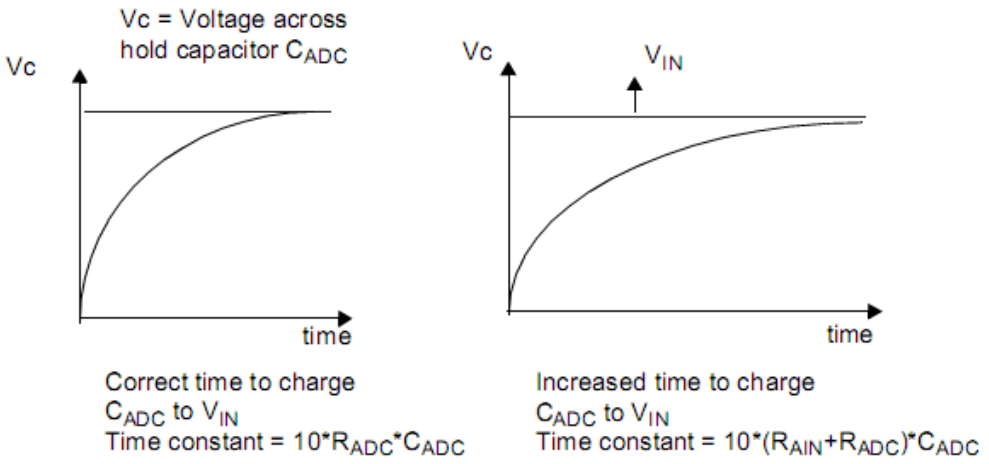
- L'impédance de sortie de la source se rajoute à l'impédance d'entrée de l'ADC:

$$\tau = (R_{ADC} + R_{AIN}) * C_{ADC}$$

- Grande R_{AIN} affecte THD

- Ex: AD7684 16 bits
  - Précision1 LSB/16 bits: 1/65536
    → précision atteinte à 11 τ
  - R_{ADC} = 600 Ω, C_{ADC} = 30 pF
  - 11 x τ = 200 ns

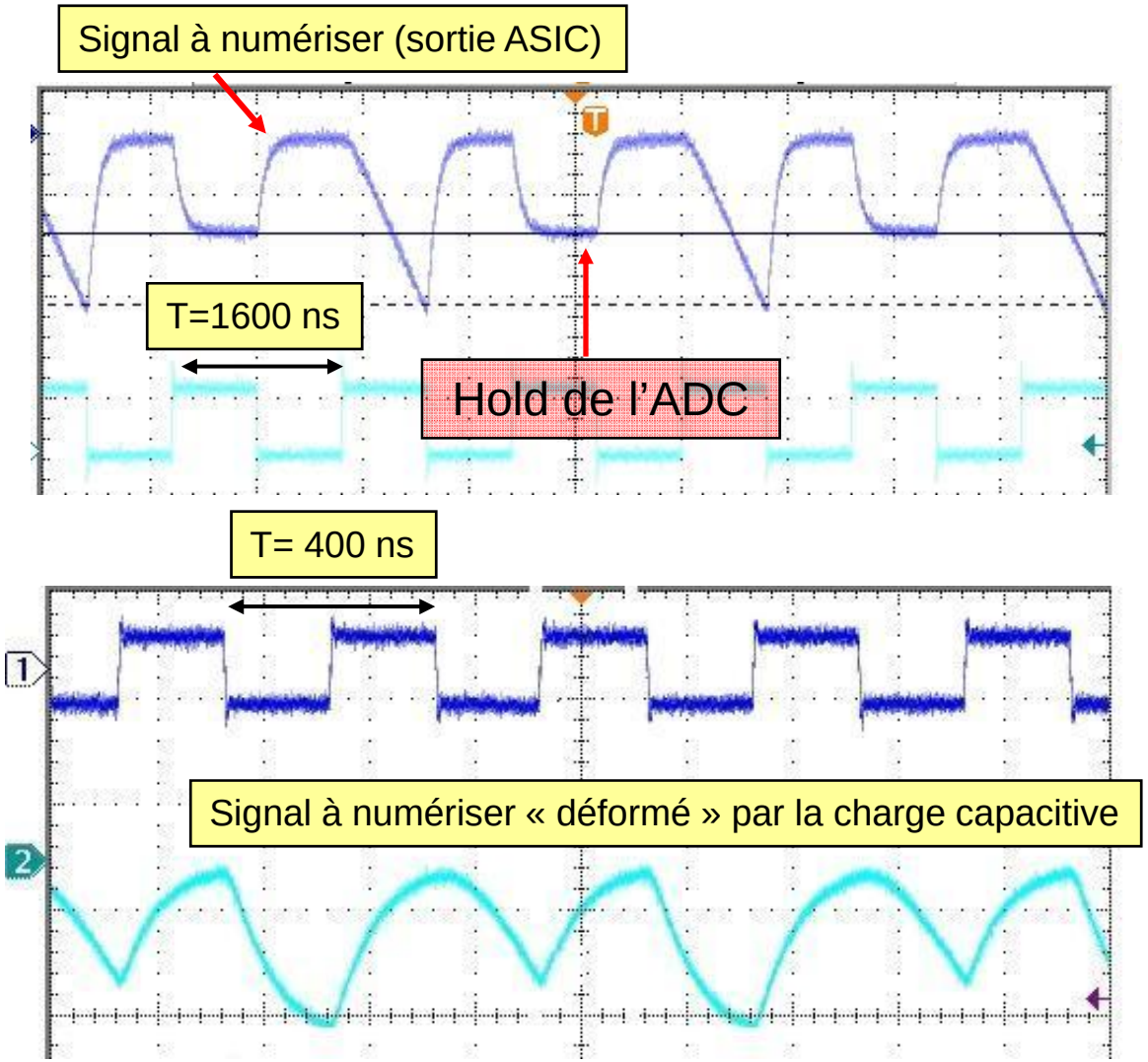




AINx = analog input pin
C_{ADC} = the hold capacitor of the ADC
Refer to datasheet for values for R_{ADC} and C_{ADC}

Source: App. note ST [AN1636]

Exemple de driver mal adapté

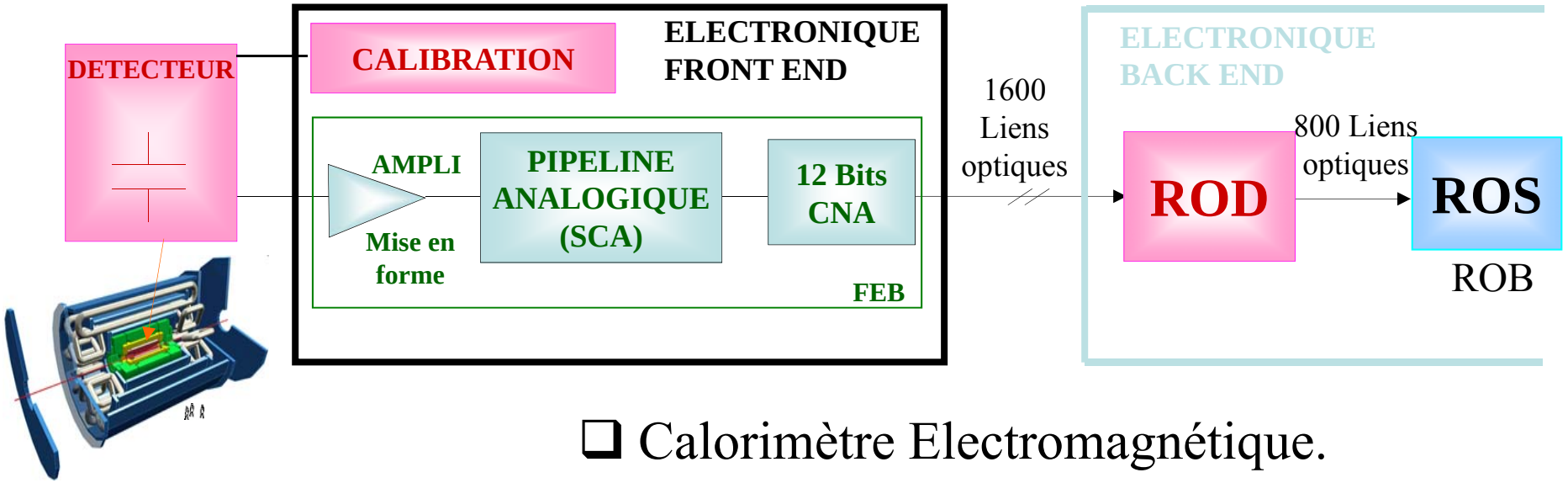


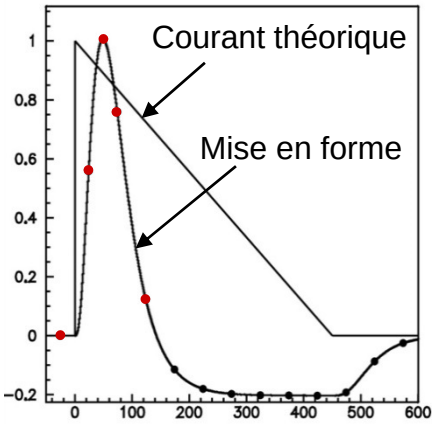
- Utilisation de l'ADC AD7684 pour numériser un signal délivré par un ASIC (mémoire analogique Made in LPC Clermont)
- Un driver interne à l'ASIC
- Pas de driver externe
- A la période nominale T= 400ns le signal n'a pas le temps de s'établir

Source: F.Collange (LPC Clermont)

4. Quelques exemples d'utilisation d'ADC @ IN2P3

FEE du calorimètre électromagnétique d'Atlas



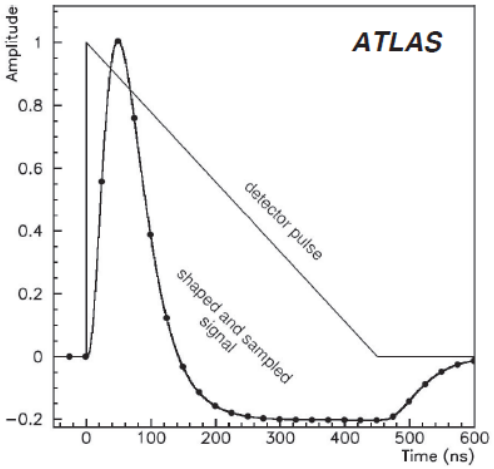


- Calorimètre Electromagnétique.
  - 200.000 Cellules
  - 1600 Modules FEB
  - 200 Modules ROD
  - 120 Modules de Calibration

Source: G.Perrot - LAPP[PER]

FEE du calorimètre électromagnétique d'Atlas

- Cartes Front-End du calorimètre à argon liquide d'Atlas (FEB)
  - ≈ 200 000 voies → 128 voies par cartes
  - dimensions: 400x500 mm^2 !!
  - 1629 cartes produites
  - Utilisation d'un ADC AD9042 par voie
  - Mesures, sous irradiation, de la dérive de:
    - ✓ la consommation en courant
    - ✓ la précision
    - ✓ du temps de conversion
    - ✓ la référence de tension interne



Source: [Atlas_Lar]

Carte FEB 128 voies

Source: T.Liu et al. [SMU]

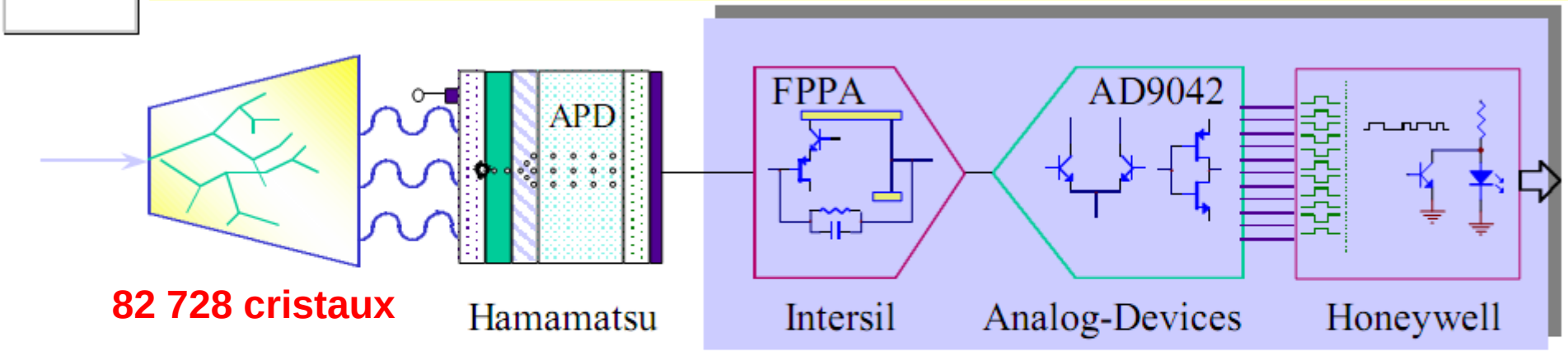
Figure 25. The amplitude vs. time for the triangular pulse shape from the LAr calorimeter, overlaid with the bipolar-shaped and sampled pulse shape.

FEE du calorimètre électromagnétique de CMS

CMS

ELECTROMAGNETIC CALORIMETER

FRONT-END ELECTRONIC CHAIN



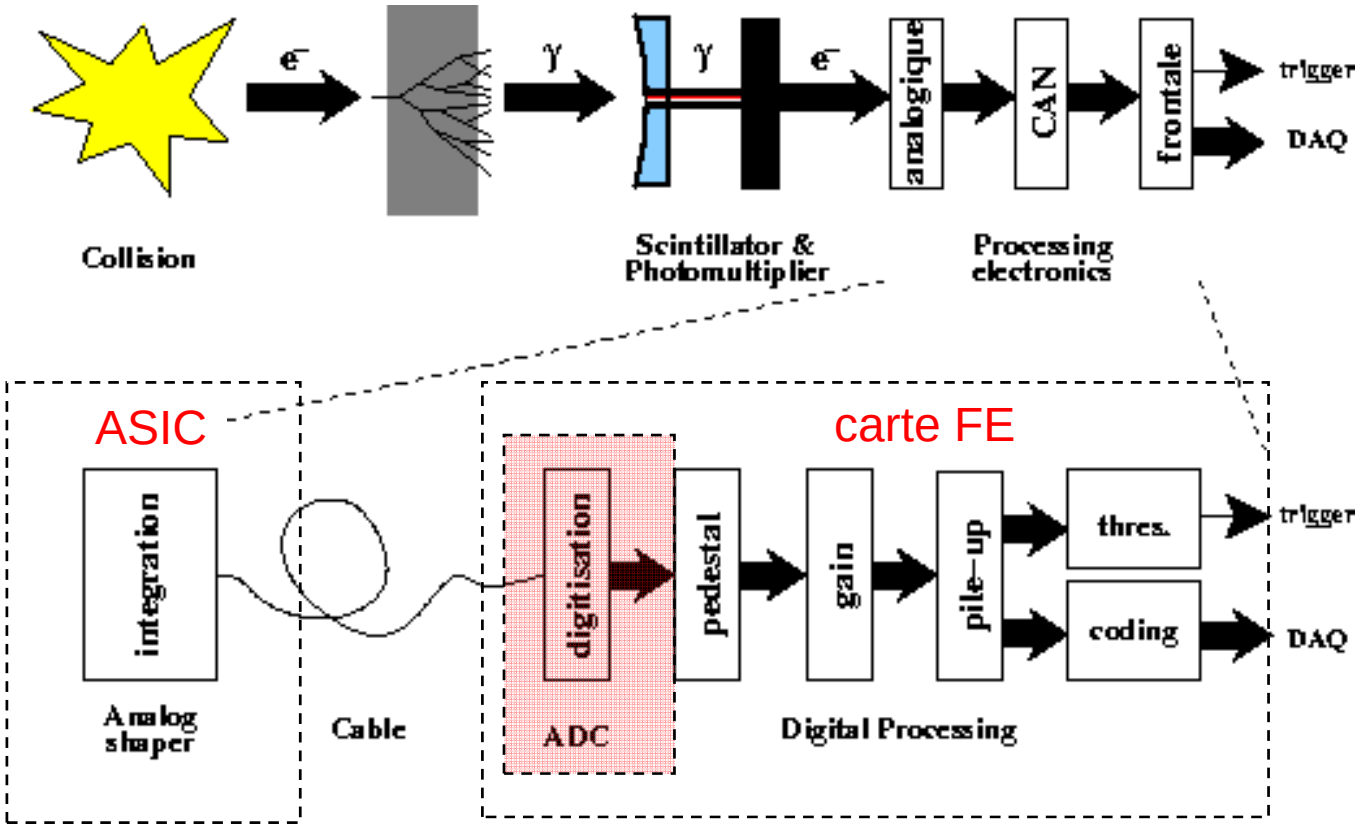
Full custom Ctrl Chip (not shown)	Type of IC	Full custom ASIC	Commercial ADC	Full custom ASIC
DMILL	Process	UHF1X	XFCB	CHFET

RAD HARD ELECTRONICS, Power dissipation: 1,2 W/channel

10^4 Gy = 1 Mrad

Source: P.Denes [CMS1] & P.Depasse [CMS2]

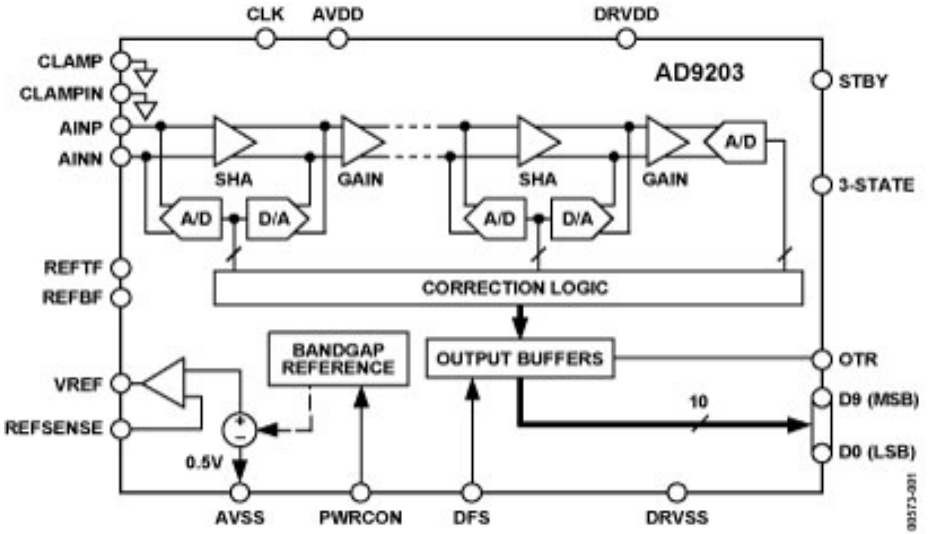
FEE du preshower de LHCb (LPC Clermont)



Source: R. CORNAT - LPC - LECC Colmar - septembre 2002

FEE du preshower de LHCb (LPC Clermont)

- ADC AD9203 (Analog Devices):
  - Architecture: pipeline, différentiel
  - Resolution: 10 bits sur 1V différentiel
  - Sampling rate: 40 MS/s
  - Consommation:74mW/3V



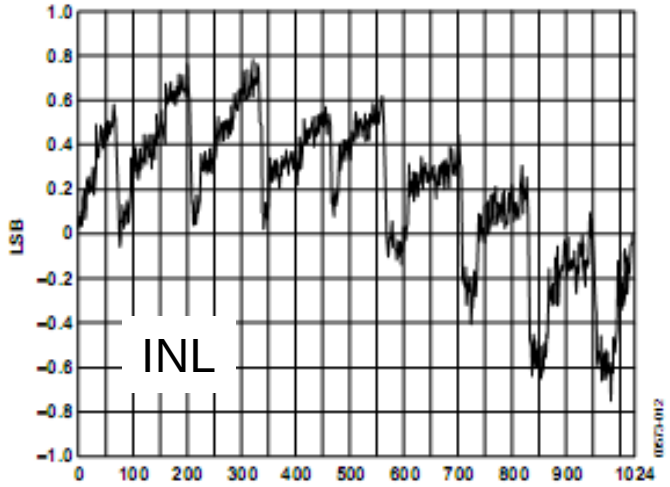


Figure 12. Typical INL Performance

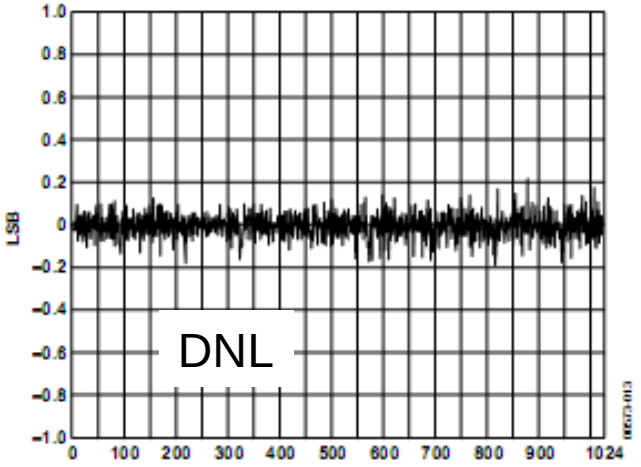
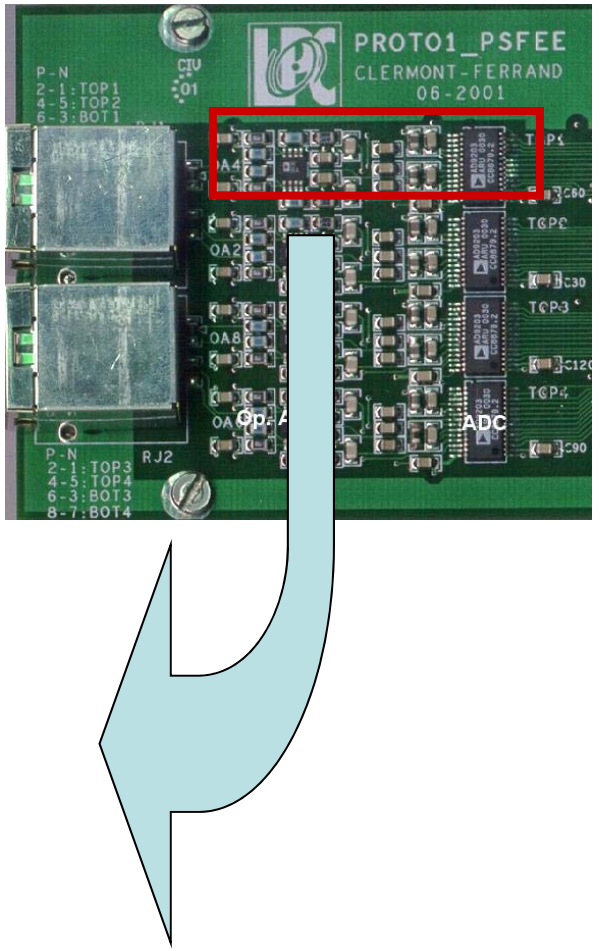


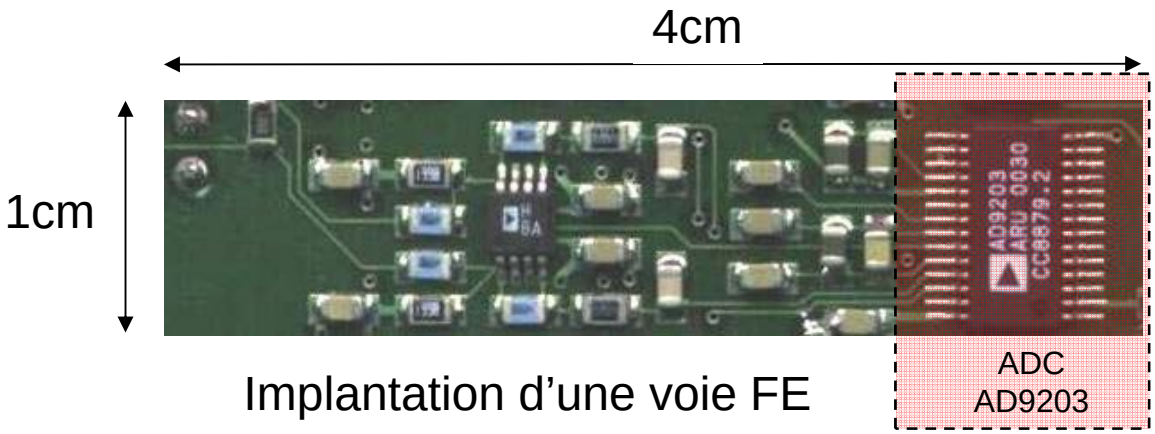
Figure 13. Typical DNL Performance

Source: Analog Devices

FEE du preshower de LHCb (LPC Clermont)

- 64 voies par carte format 9U
  - Surface max. d'une voie: 1 cm x 4 cm
- Bruit <1 LSB (1mV) grâce:
  - Plan de masse
  - Signaux analogiques différentiels
  - Horloge différentielle LVDS
  - Routage précautionneux des pistes sensibles



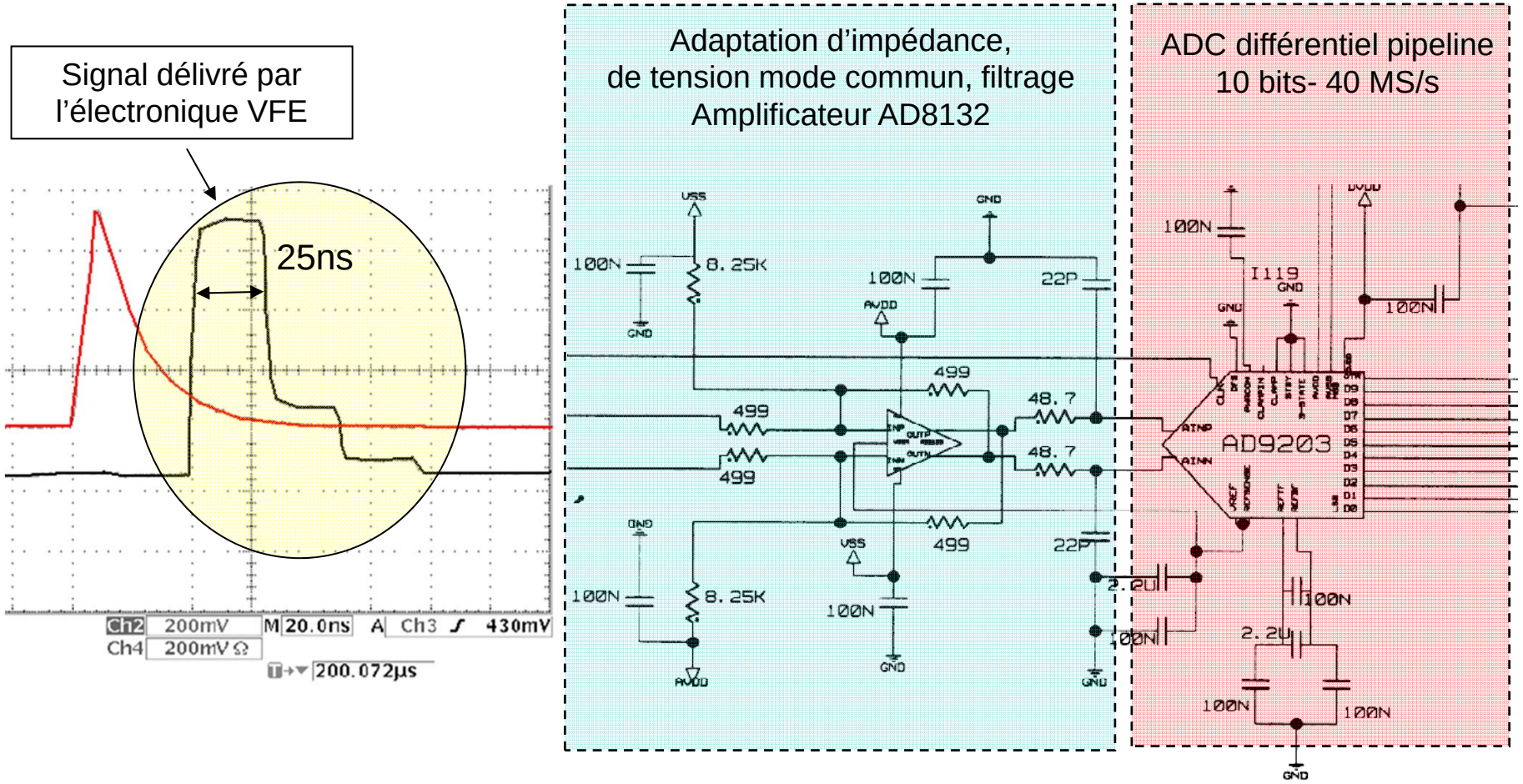


Implantation d'une voie FE

Source: R. CORNAT - LPC - LECC Colmar - septembre 2002

FEE du preshower de LHCb (LPC Clermont)

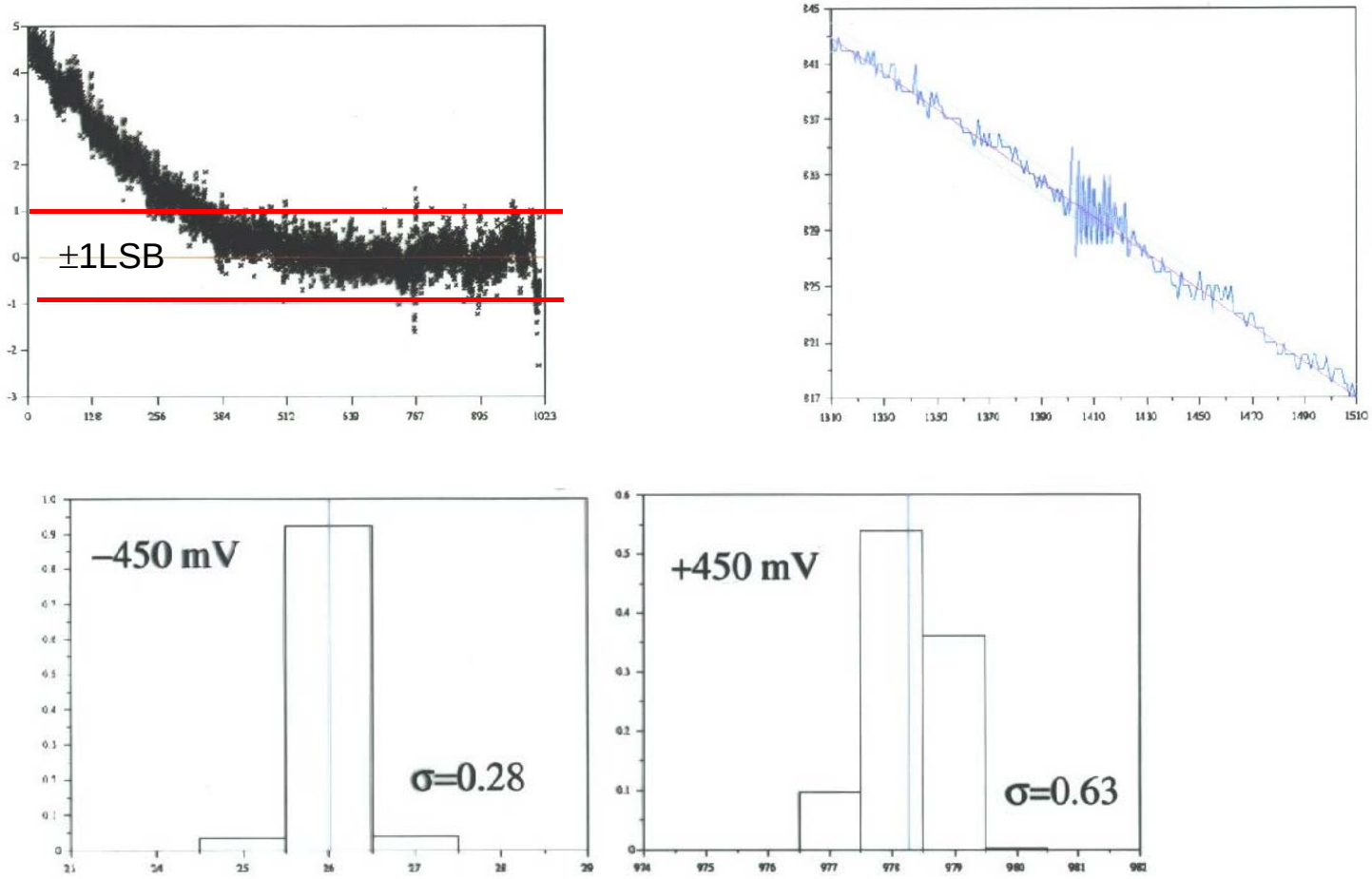
- Schéma d'une voie front-end



Source: R. CORNAT - LPC - LECC Colmar - septembre 2002

FEE du preshower de LHCb (LPC Clermont)

- Résultats de mesure d'une voie complète (VFE + FE)



Source: J. LECOQ - LPC

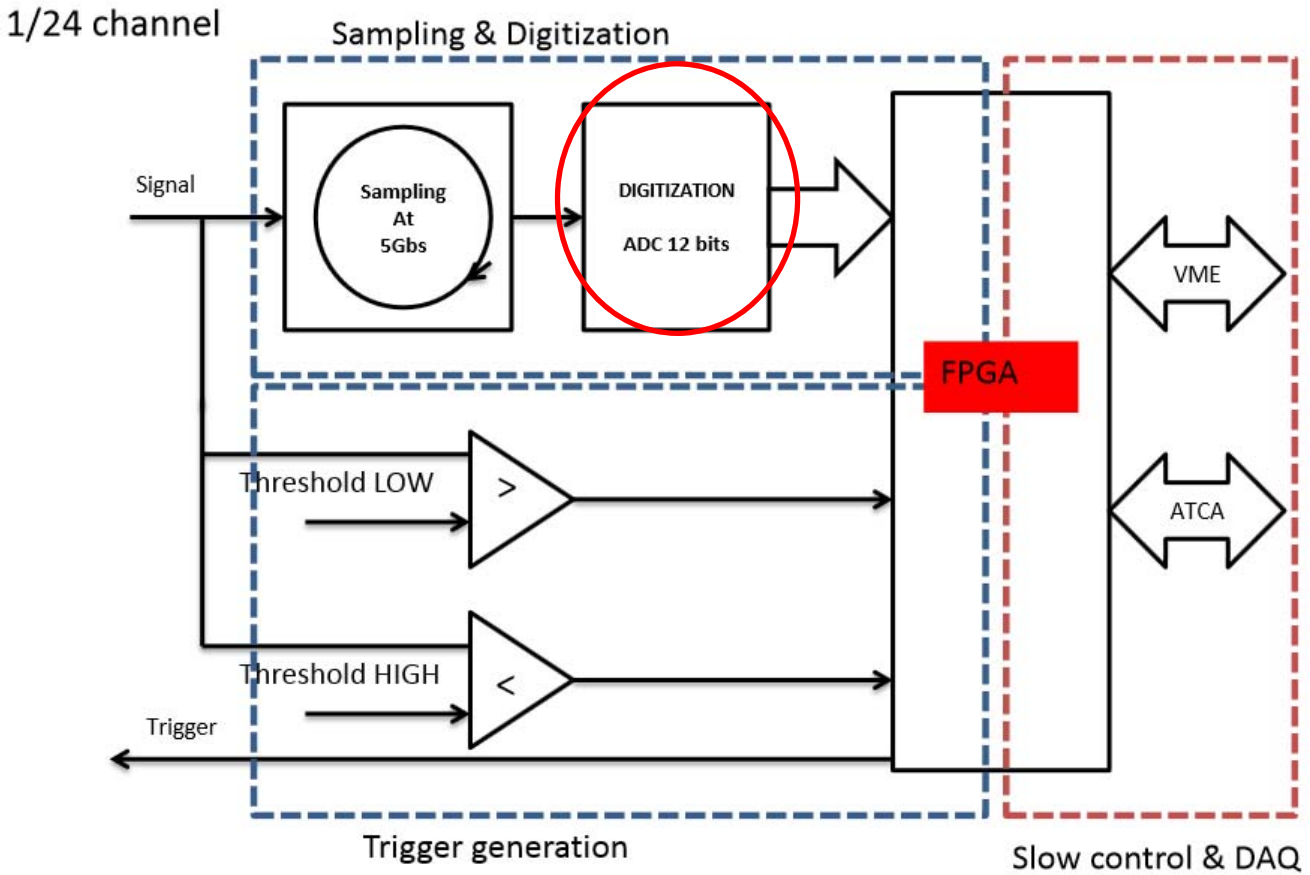
Aperçu @ IN2P3

Journées VLSI - FPGA - PCB de l'IN2P3
de mercredi 11 juin 2014 au vendredi 13 juin 2014
à **CPPMarseille**

https://indico.in2p3.fr/conferenceOtherViews.py?view=standard&confId=9825

Carte d'échantillonnage pour une application TEP en hadronthérapie

Board functional diagram



The USB_WaveCatcher board (V6)

Pulsers for reflectometry applications

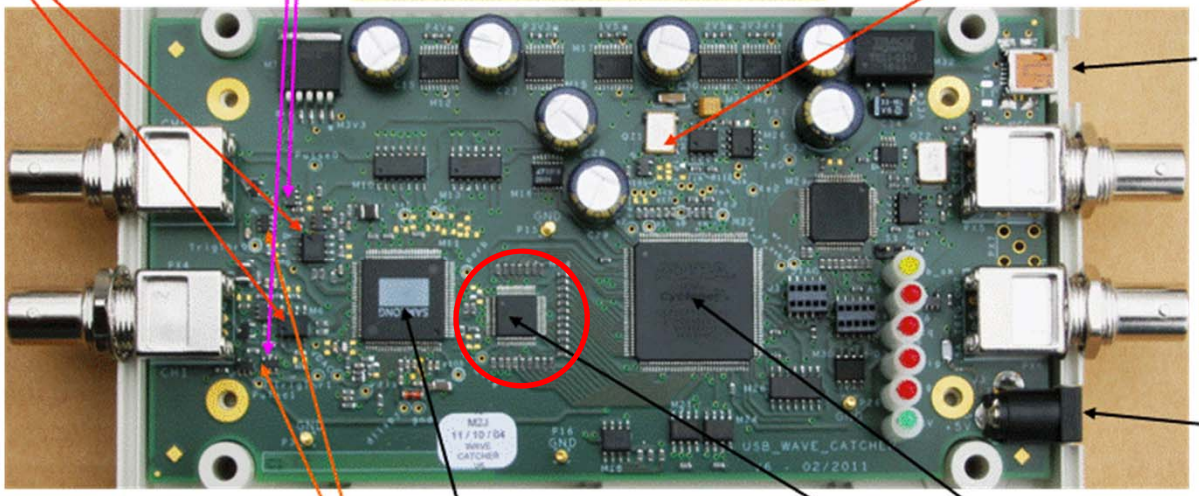
1.5 GHz BW amplifier.

Board has to be powered by USB
=> power consumption ≤ 2.5W

Reference clock:
200MHz => **3.2GS/s**

2008/2010

2 analog inputs.
DC Coupled.



µ USB

Trigger input

Trigger output

+5V Jack plug

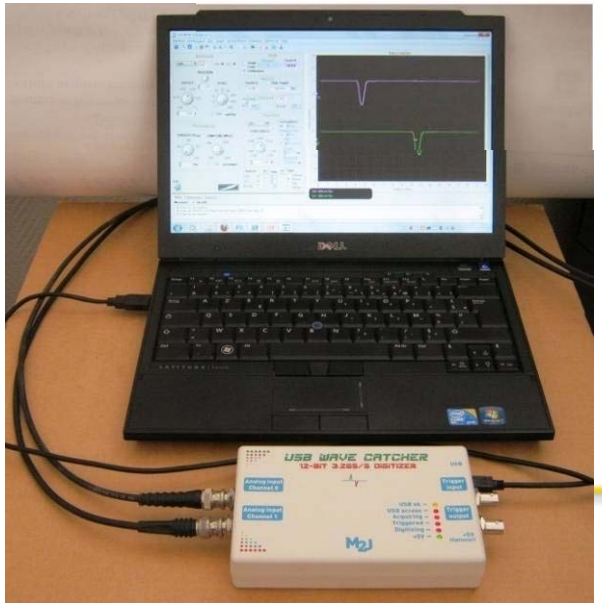
Cyclone FPGA

SAM Chip

Trigger discriminators

Dual 12-bit ADC

The autonomous test bench



The historical 2-Channel module

Système d'acquisition pour caractérisation d'un imageur à multiplication électronique intra-pixel emCMOS

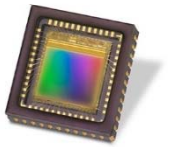
Remi Barbier, Timothée Brugière, David Chaize, Sylvain Ferriol, Cyrille Guérin, William Tromeur, Lionel Vagneron

Projet dans le cadre d'une collaboration E2V / IPNL

E2V

http://www.e2v.com

- Développement de matrices de nouveaux pixels avec multiplication électronique intra-pixel (emCMOS)

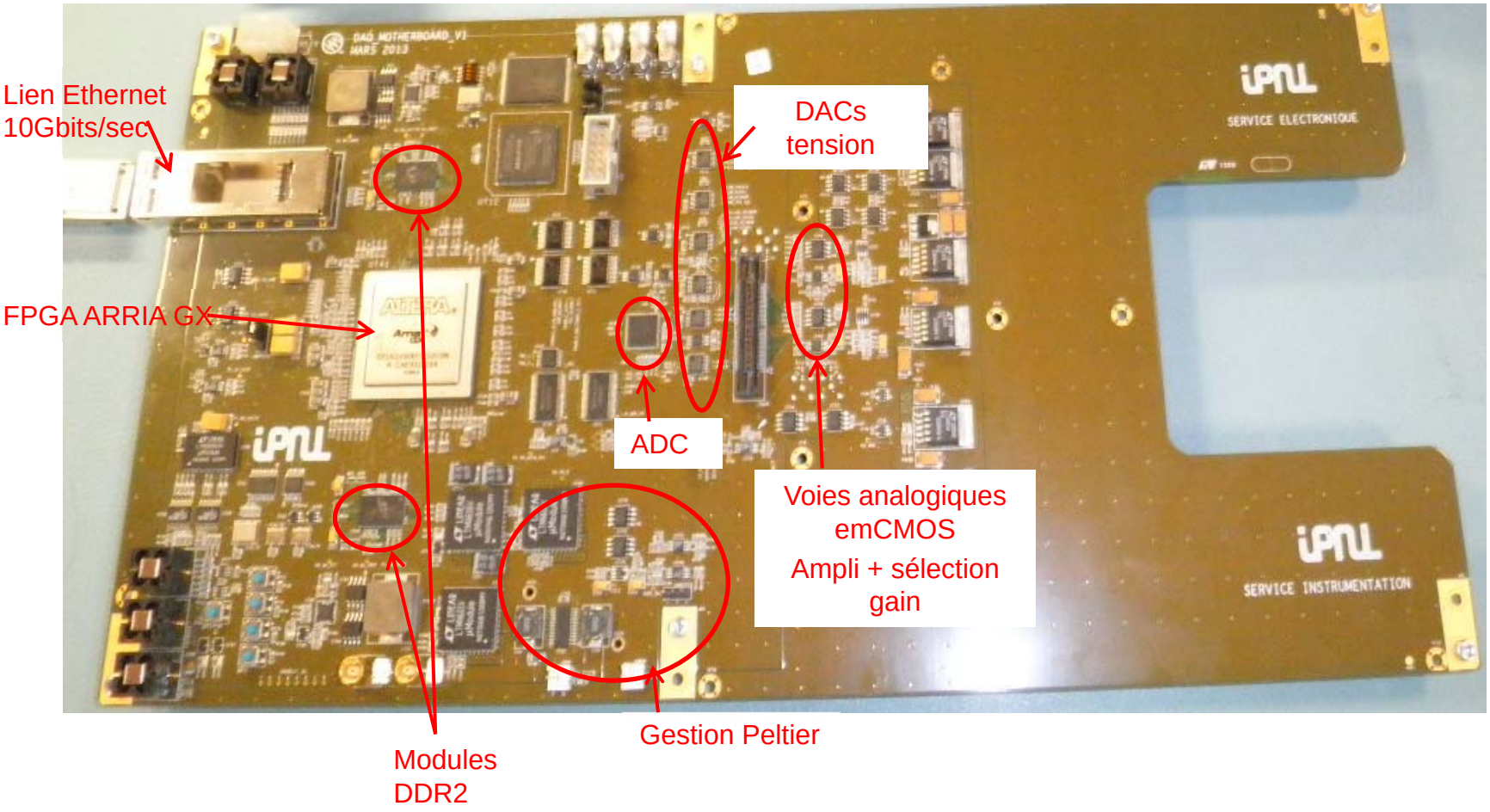


IPNL

- Conception du système d'acquisition
- Validation et caractérisation du système
- Caractérisation des matrices de nouveaux pixels sur banc optique

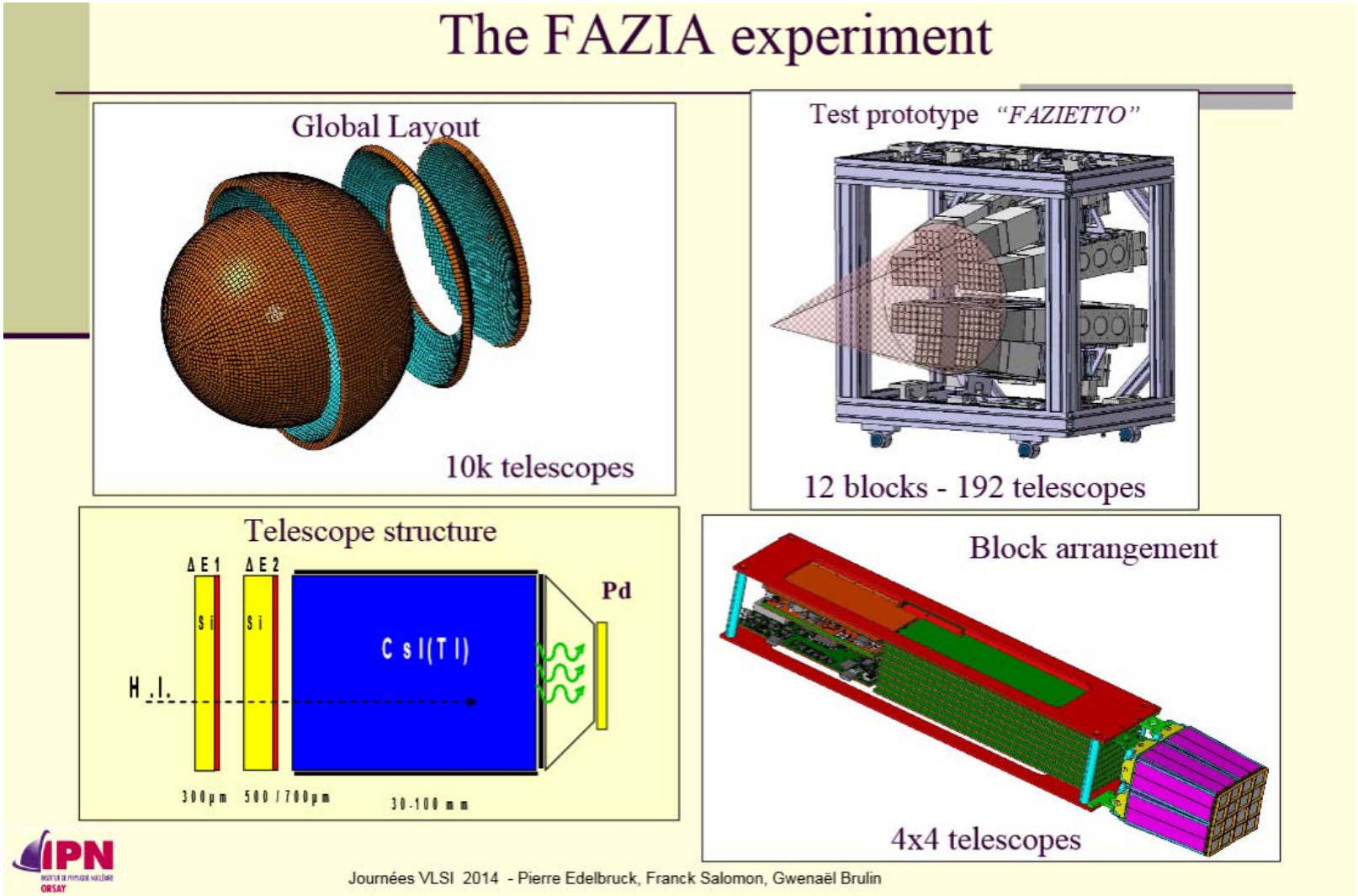
5. Présentation des cartes

➢ Carte mère

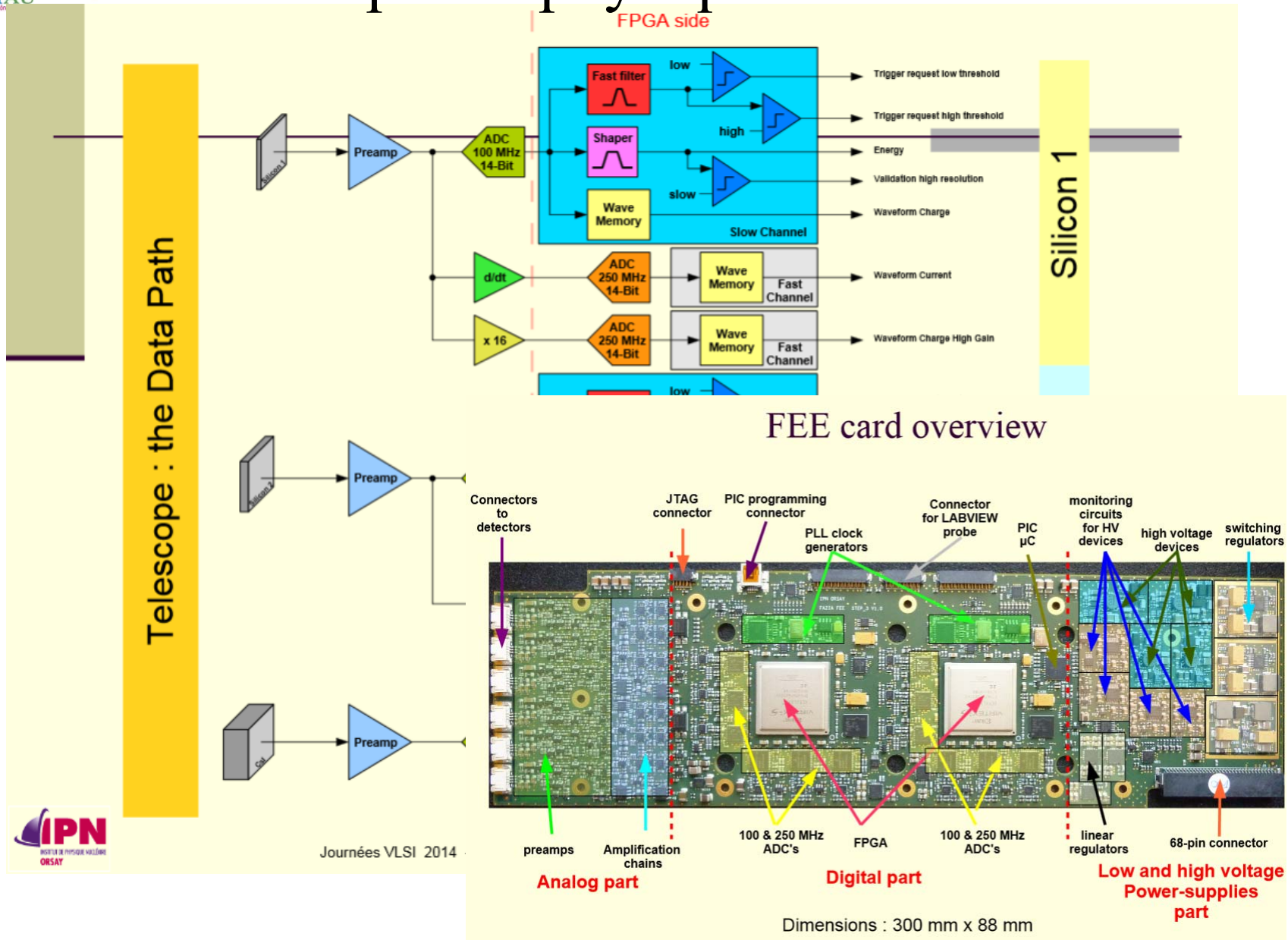


Exemple en physique nucléaire: FAZIA

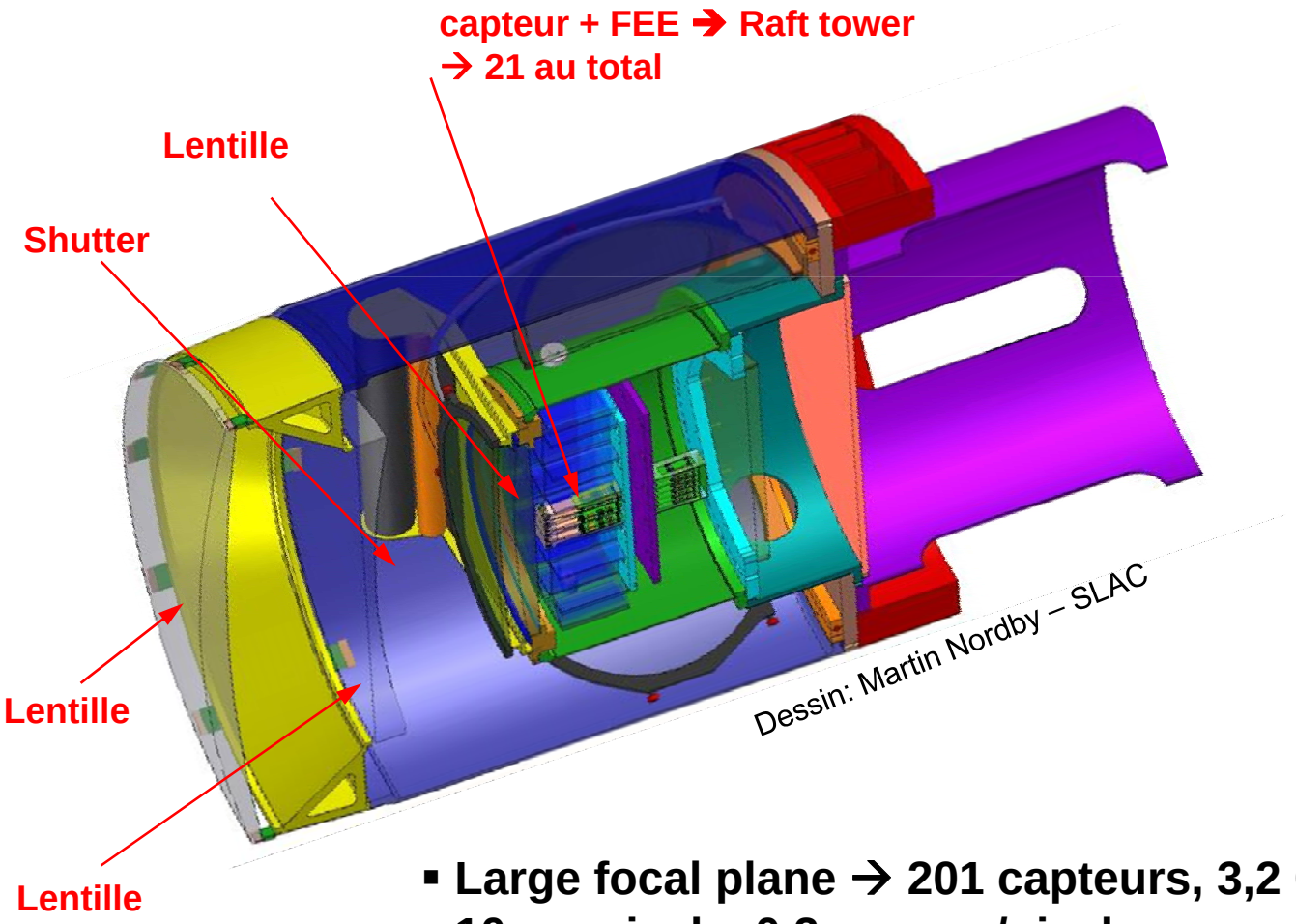
FAZIA est un multidétecteur de nouvelle génération pour les particules chargées, prévu pour servir dans le domaine des collisions d'ions lourds autour et au-dessous de l'énergie de Fermi (10-100 MeV par nucléon).



Exemple en physique nucléaire: FAZIA



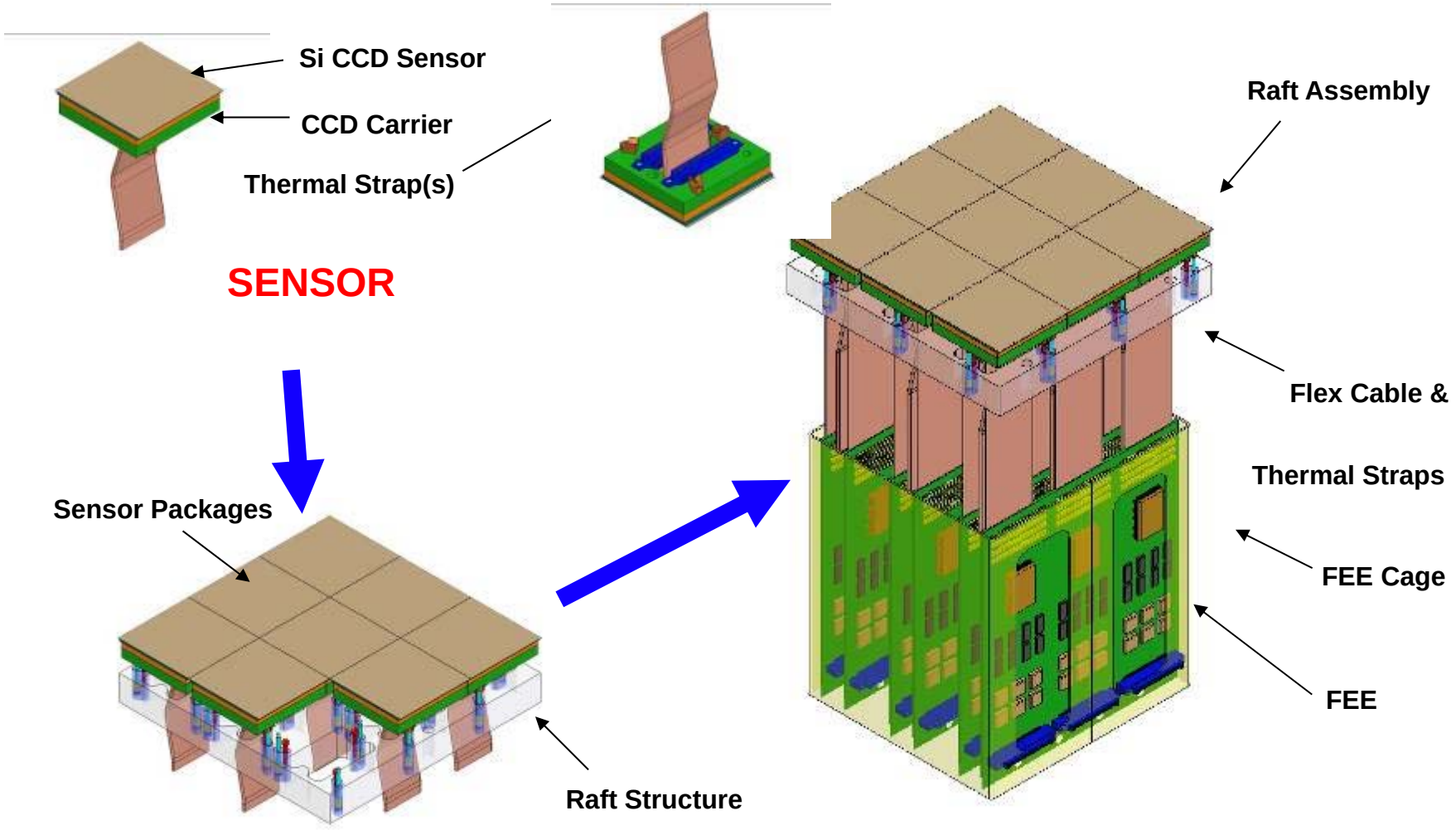
Large Synoptic Survey Telescop (LSST)



- **Large focal plane ➔ 201 capteurs, 3,2 Gpixels, 64 cm plan focal**
- **10 µm pixels, 0.2 arc-sec/pixel**
- **Chaque image: équivalent 40 lunes pleines**
- **Une image complète du ciel en 3 nuits**

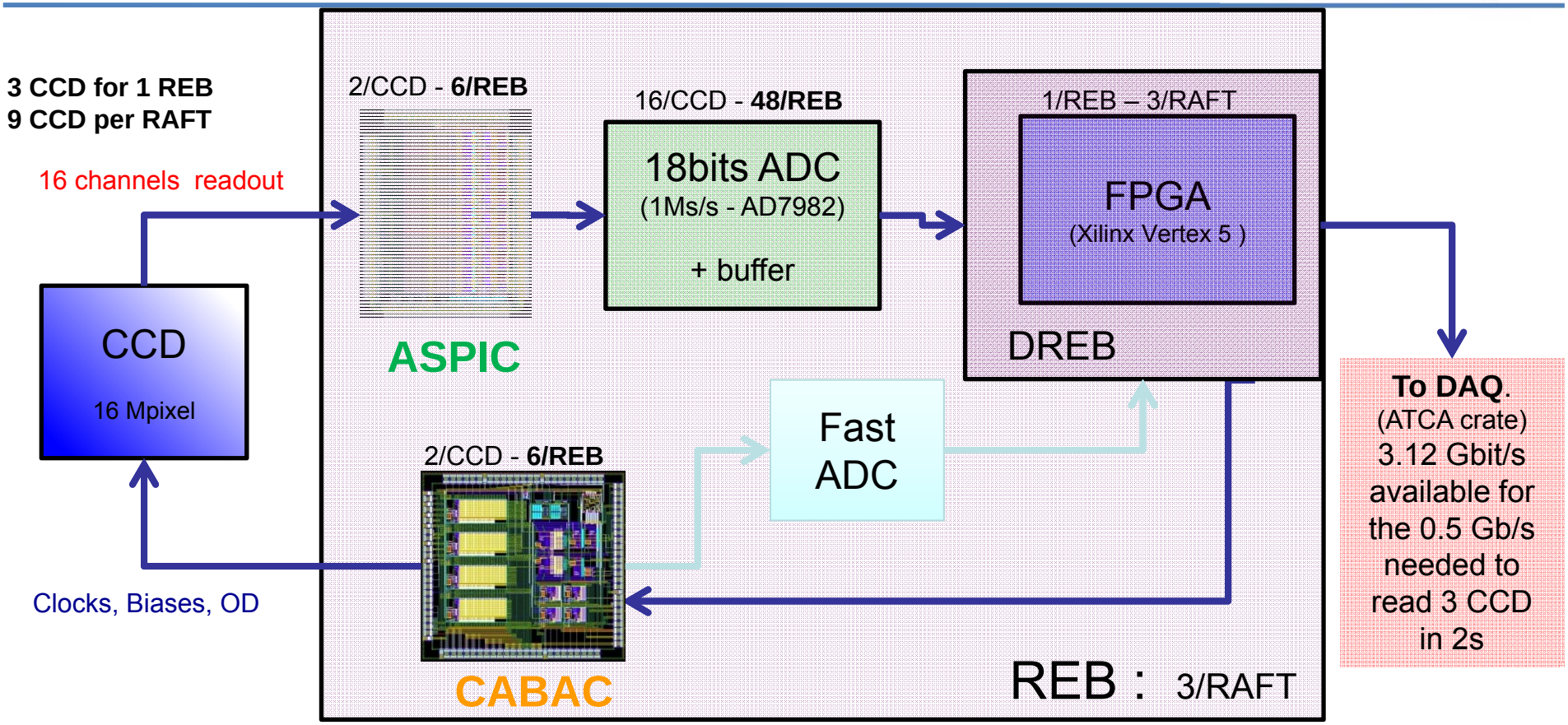
Source: K.Gilmore [LSST1] & J.Oliver [LSST2]

Large Synoptic Survey Telescop (LSST)



Source: K.Gilmore [LSST1] & J.Oliver [LSST2]

Camera Electronics : Raft Electronic Board



ASPIC a pour fonction d'amplifier les signaux analogiques provenant des 16 sorties de chaque CCD

16 sorties /CCD x 189 =

↳ **3024 voies d'électronique**

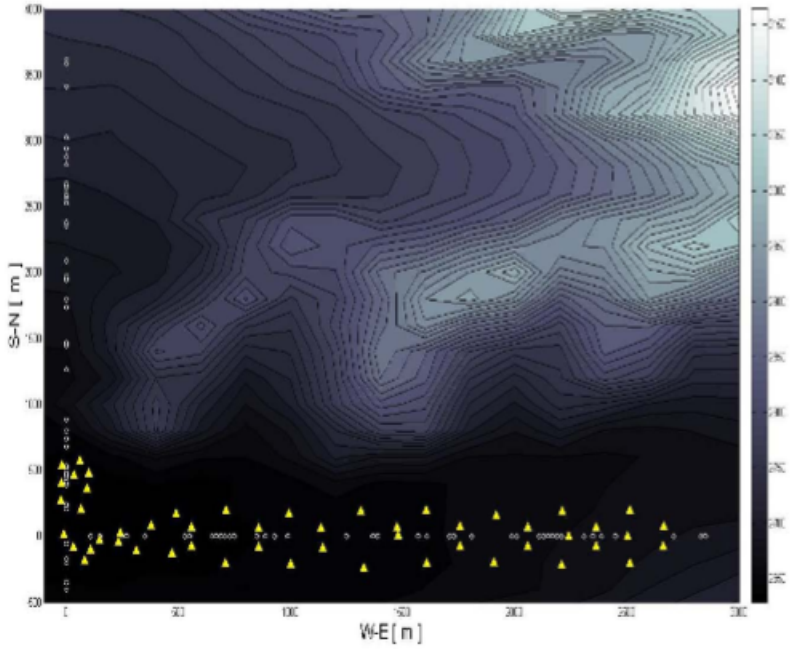
CABAC a pour fonction de fournir

- l'alimention (OD) de l'étage de sortie du CCD les polarisations : RD, OG, GD/SC
- Horloges "images" (parallel)
- Horloges "registres" (serial)

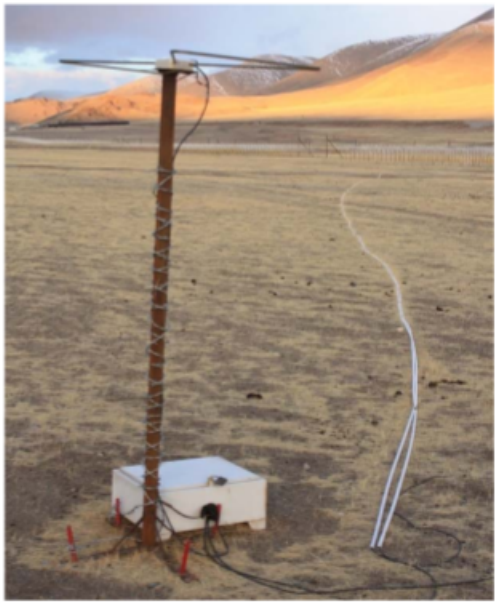
Expérience radio: TREND

INTRODUCTION TO THE TREND

- The aim of the Tianshan radio experiment for neutrino detection (TREND) is to build a large radio array to search for ultra high energy (UHE) neutrinos. The first results of TREND has already been announced (Astroparticle Physics, 2011, 34: 717-731).
  - Distribution of TREND 50 Pods



  - One pod

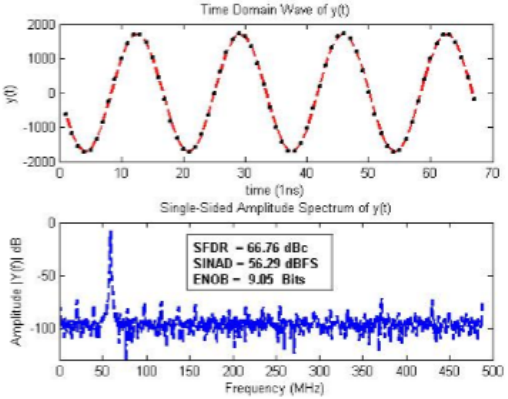


THE SELF-TRIGGERING FRONT-END STATION(CONT.)

DFADC Board:

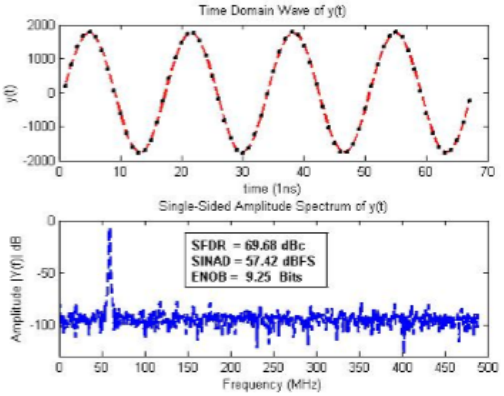
- Spartan 6 FPGA
- 12bit 1Gbps ADC(2 chns)
- 1Gb DDR2 RAM(2 Chips)
- 2 optical Link(3.125Gbps)
- USB host/peripheral Interf
- ...

ADC1



-1.3dBFS 60MHz sine signal input

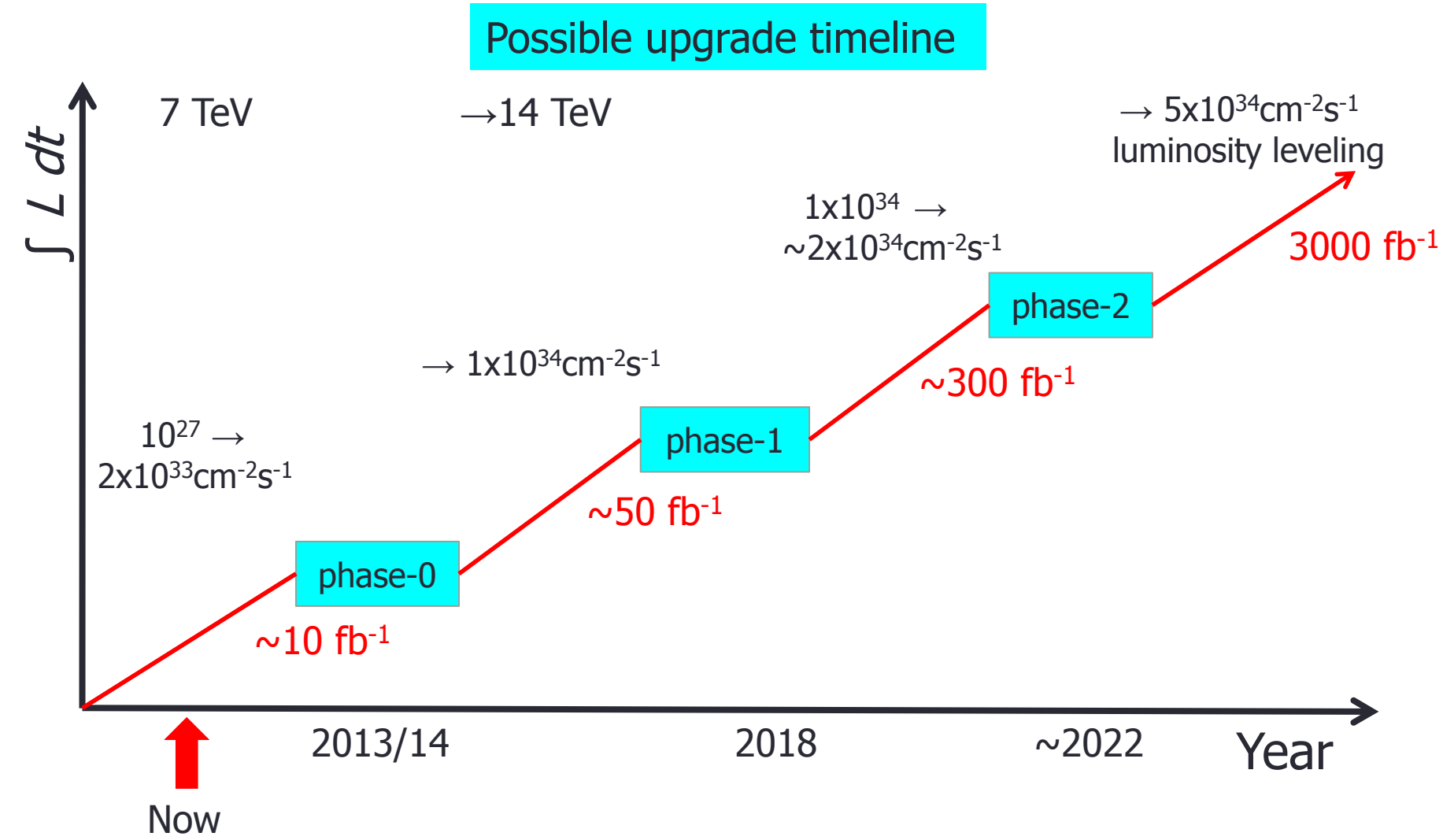
ADC2



-1.3dBFS 60MHz sine signal input

5. Perspectives: vers plus d'intégration ??

LHC and ATLAS upgrade



T. Kawamoto, TIPP2011, Chicago, USA

Le High Luminosity LHC [2]

- Toutes les expériences auront besoins d'effectuer des mises à jours afin de s'adapter à la nouvelle luminosité et aux nouvelles fréquences de fonctionnement des trigger/DAQ

LS1
2013-2014

ATLAS/CMS complèterons leur détecteurs « originels »,
préparations/début des upgrades

Phase 1a

CMS a prévu des upgrades pendant l'arrêt technique de fin d'année

LS2
2018

Upgrades majeurs de LHCb et Alice
ATLAS/CMS terminent leurs upgrades pour une plus forte luminosité

Phase 1b

Dégradation des performances de détection d'ATLAS et de CMS due aux dommages liés aux radiations

LS3
2022-2023

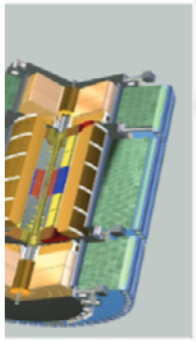
Upgrade majeur d'ATLAS/CMS afin de correspondre à la luminosité du HL-LHC
Remplacement de détecteurs/composants pour augmenter leurs longévités

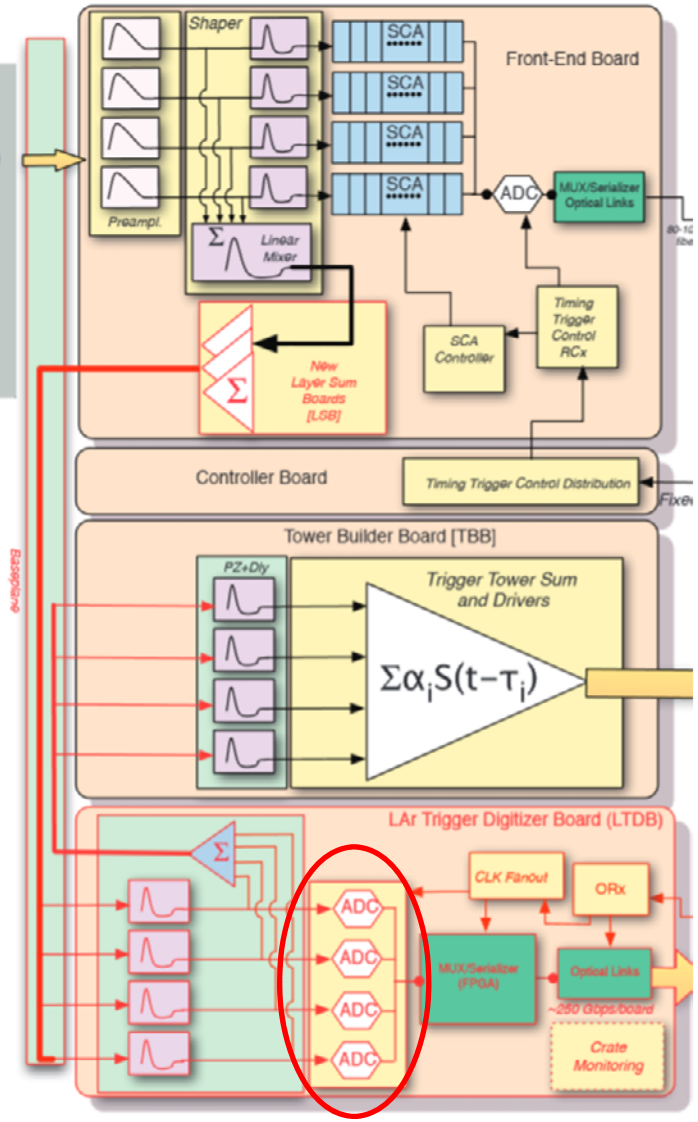
Phase 2

Fin de mise à jour pour ATLAS et CMS

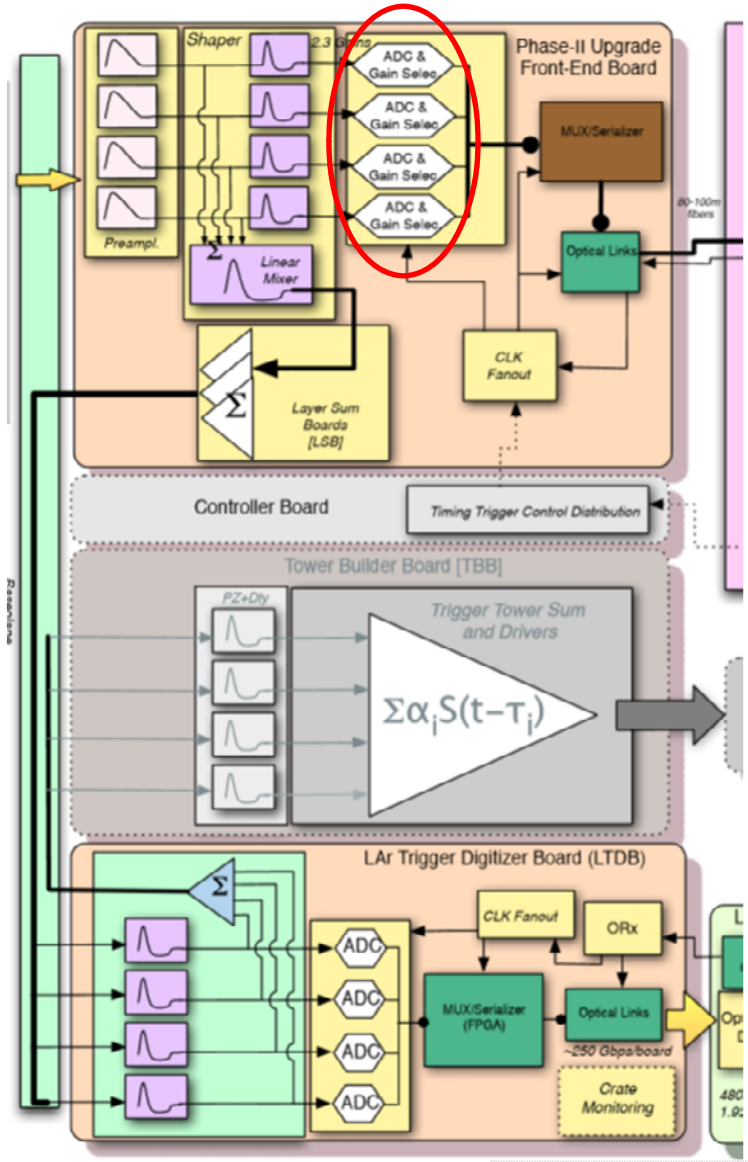
Atlas Liquid Argon Calorimeter upgrade

Upgrade phase I





Upgrade phase II



Source: [Atlas_Lar]

- FEB (nouvelle version)
  - Plus de pipeline analogique.
  - Eventuellement pipeline numérique (solution de replis à la transmission totale des datas vers le ROD).
  - ADC fonctionnant à la fréquence des BC (Commercial ? ou ?).
  - Multiplexage des ADC (4*16bits-40 MHz ou 8*16bits 20 Mhz)→ 16 bits 160 MHz
  - Sérialisation et transmission optique vers ROD (3,2 Gbits/s)
  - 32 ou 16 fibres optiques par FEB.
  - Des tests sont en cours avec des HFBR-772 (12 fibres, 2,7 Gbits/s) et un ADC du commerce (TI ADS 5272: 8 channels, 65 MSPS 12-bit ADC with multiplexed LVDS outputs) à Nevis (USA??).

Source: G. Perrot – LAPP [PER]

Atlas Liquid Argon Calorimeter upgrade

The development of high-precision fast ADCs for the LAr readout has been pursued for several years with future electronics upgrades (through Phase-II) in mind. The main challenge is to cover the full 16-bit dynamic range with one or more ADCs per channel. In any case, the low power requirement is essential; this has been the main purpose of the LAr custom ASIC R&D efforts and will continue to drive the design effort for the main readout of the calorimeter in Phase-II. This long-term development has given rise to the design of a fully operational multi-channel 12-bit device that could be used for the Phase-I trigger electronics upgrade with the potential for a significant reduction in power consumption. However, given the uncertainty and cost associated with a custom chip design, an extensive search has been conducted for a commercial off-the-shelf (COTS) option meeting the electrical and radiation requirements.

There are two custom ASIC developments, based on the IBM CMOS8RF (130 nm) technology, which has been chosen because of its established CERN procurement contract, its radiation tolerance for digital circuits, and its anticipated use for LHC upgrades, enabling sharing of experience and re-use of building blocks developed by others. The two ASIC approaches are at different stages of prototyping and are described below. A COTS option (the Texas Instruments ADS5272) has been also identified as candidate for the LTDB. A demonstrator LTDB is being designed with this ADC (see Appendix D).

The LAr Collaboration will make the final decision on the ADC for the LDTB when test results are available from the two ASIC ADCs and experience is obtained with the system implementation of the ADS5272. The schedule for this decision is discussed in Chapter 6.

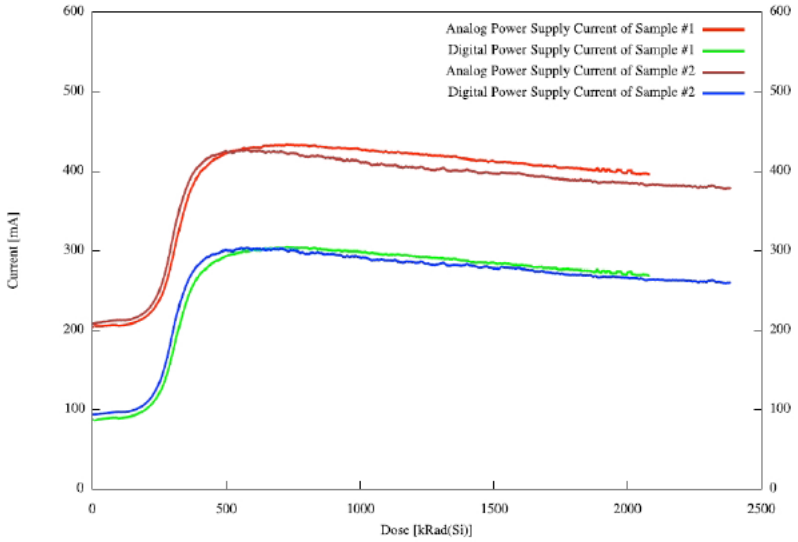
Table 10. Specifications for the ADC. The ADC must have a serial output using either standard LVDS or SLVS technology. The ADC word must be either 12-bit or 16-bit in one frame, with a frame clock at 40 MHz and a bit clock at 480 MHz (12-bit case) or 640 MHz (16-bit case). The latency is the time between the first sample and the last bit out. The power consumption is given per ADC channel at 40 MSPS. For comparison, values for the COTS TI ADS5275 ADC are given in the third column.

Parameters	Requirement	ADS5272
Sampling rate	≥ 40 MSPS	40 MSPS
Dynamic range	12 bits	12 bits
Resolution (ENOB)	≥ 11	11.5
Differential Nonlinearity	≤ 1 lsb	0.3 lsb
Integral Nonlinearity	≤ 1 lsb	0.4 lsb
Latency	≤ 200 ns	162.5 ns
Power consumption	≤ 145 mW	113 mW

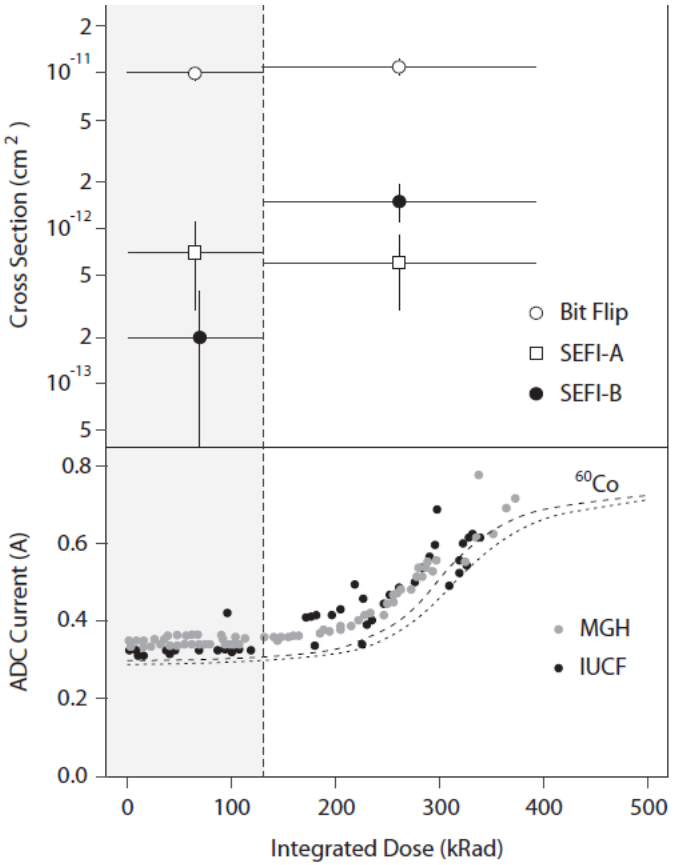
COTS TI ADS5272 ADC

Source: [Atlas_Lar]

Test tenue aux radiations



(a)

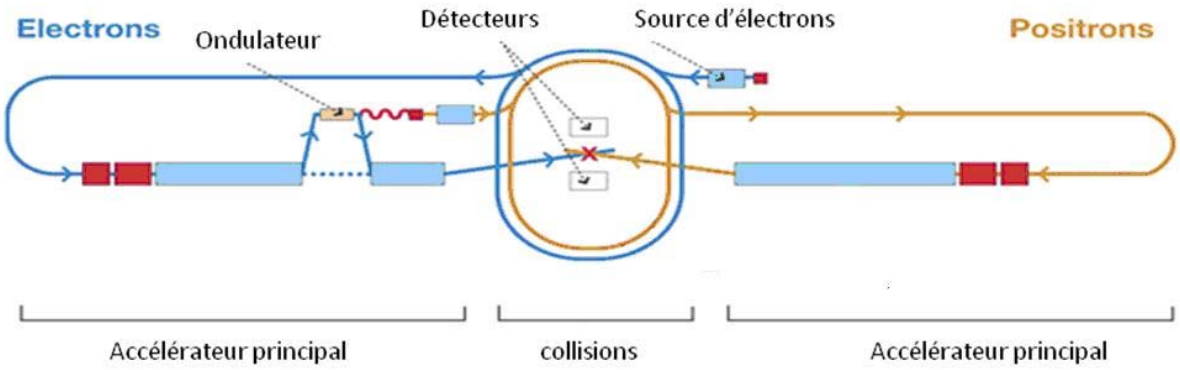


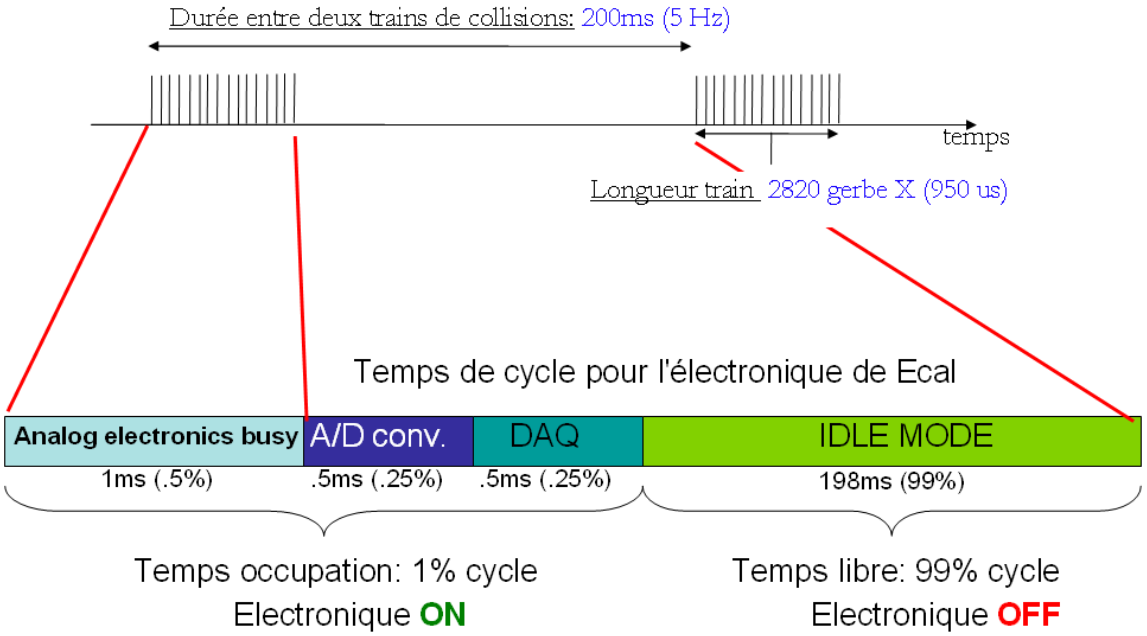
(b)

Figure 33. (a) Current drawn by 2 TI ADS5272 test samples as a function of irradiation dose (^{60}Co). (b) Results of SEE performed at two different 200 MeV high flux protons beam facilities (MGH and IUCF). Besides single bit-flips, both SEFI-A (reset signal recovered upsets) and SEFI-B (power-cycle recovered upsets) were detected during these tests. The increase of power consumption due to the absorbed dose follows the one observed during ^{60}Co irradiation (dotted line).

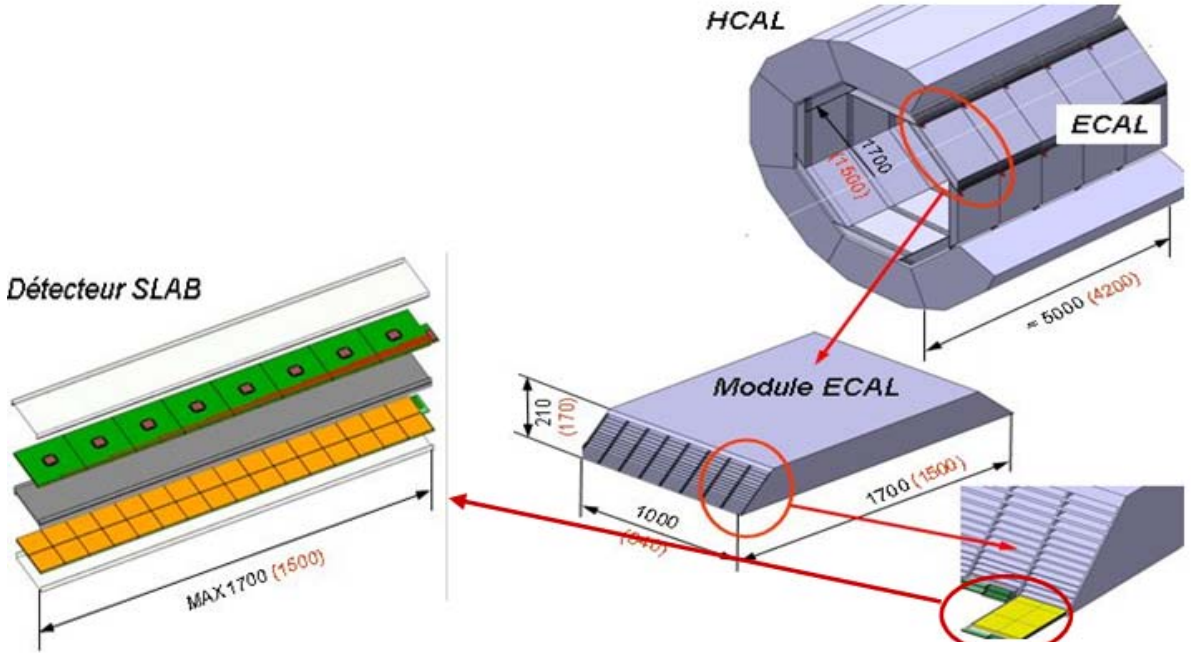
Source: [Atlas_Lar]

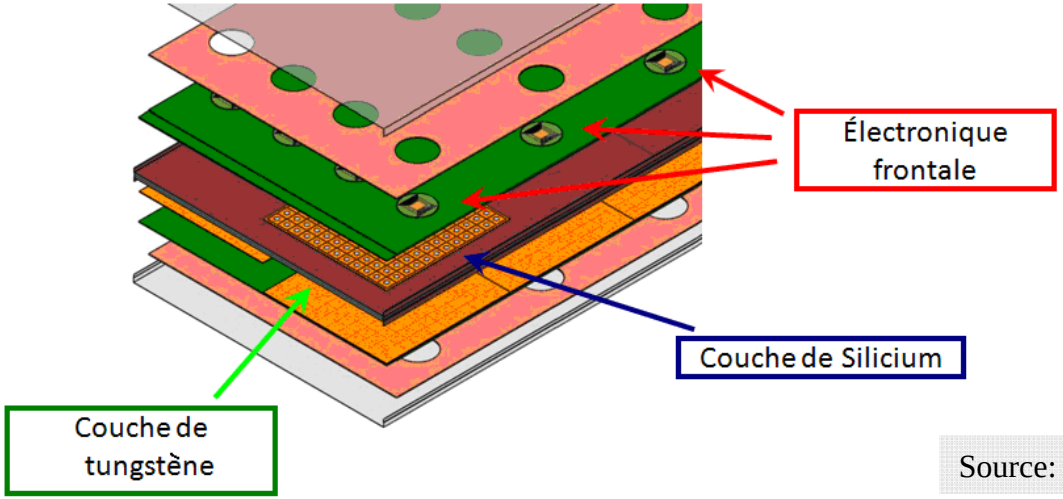
International Linear Collider (ILC)





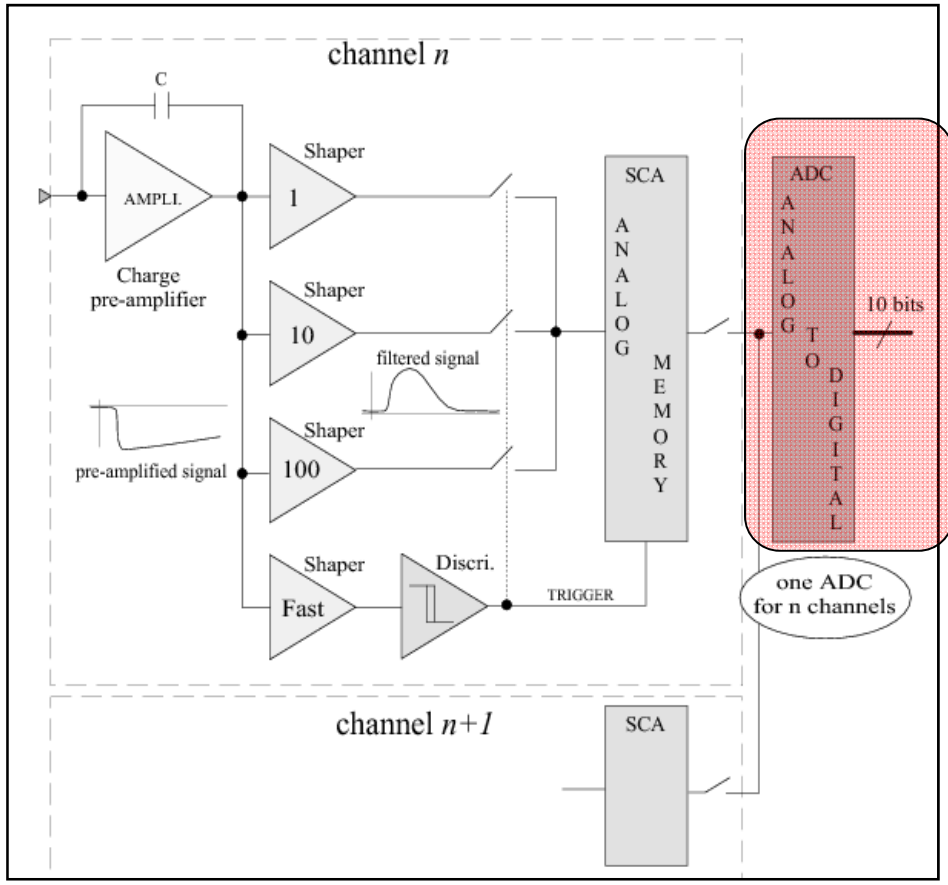
VFE electronics of Si-W Ecal





Source: M. Anduze – LRR

VFE electronics of Si-W Ecal

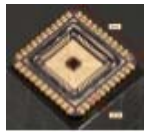


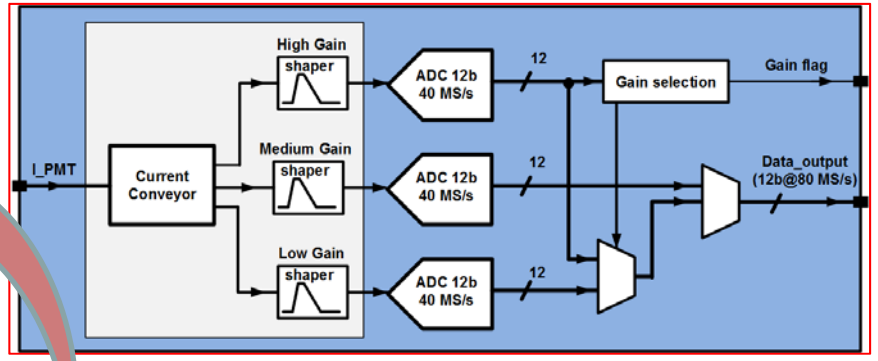
- **Requirements for ADC @ ILC**
  - **100 000 000 channels !!**
  - **Ultra low power:** 25µW/ch **for the whole power-pulsed Very-Front-End electronics, including ADC**
  - **Resolution of ADC:**
    - ✓ 10 bits if 3-gain shaping
    - ✓ 12 bits if 2-gain shaping
  - **Compactness, electronics embedded in detector**

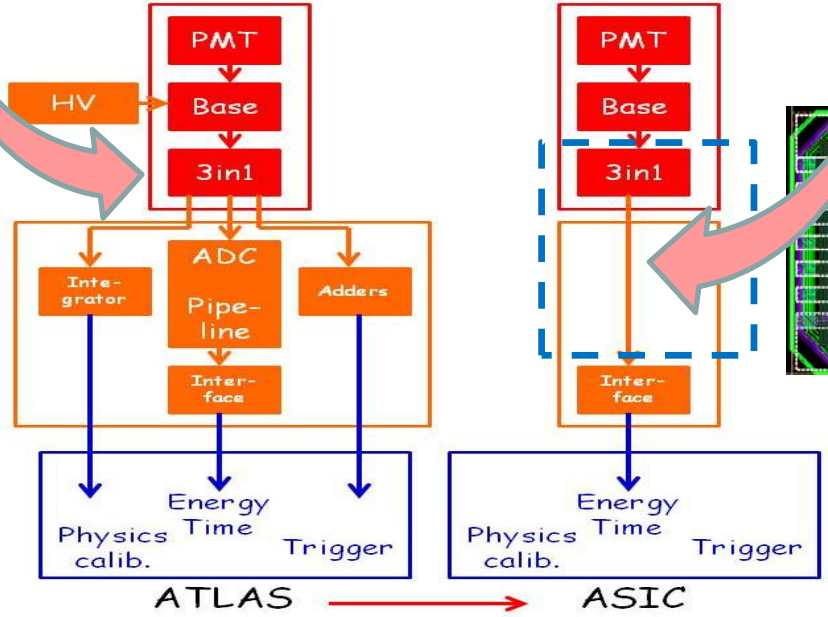
⇨ Intégration de l'ADC dans le VFE

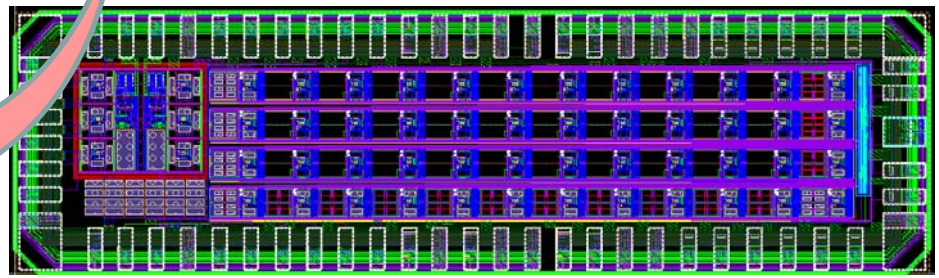
Upgrade du TilaCal d'Atlas

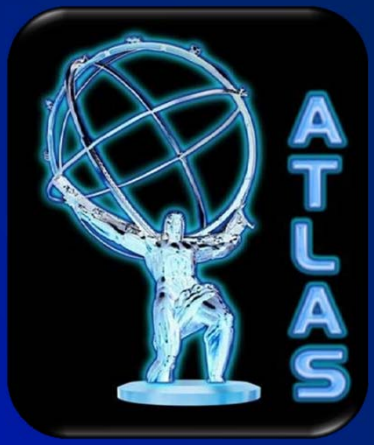
- Changement de la carte de lecture des PMT « 3-en-1 » vers « tout-en-un »
  - ASIC FATALIC4











Trends in Front-End ASICs for Particle Physics

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TIPP - Amsterdam - June 2014

Source: [TIPP]

Evolution of Front-End ASIC Design Groups

In order to **contribute to future PP detectors**
FE ASIC groups need to:

- **grow (30-40%)**
- increase collaborations (know-how exchange)
- develop/acquire "**system-level FE ASIC designer**"
- develop/acquire "**high-density interconnects**“
- **align technologies**
- evolve and **coordinate R&D**

PP community needs to **contribute with 25-30%**

Alternative? Pay companies (hundreds M$)

Source: [TIPP]

Coordinating R&D

R&D on enabling circuits/technologies

keep < 1W/cm^2

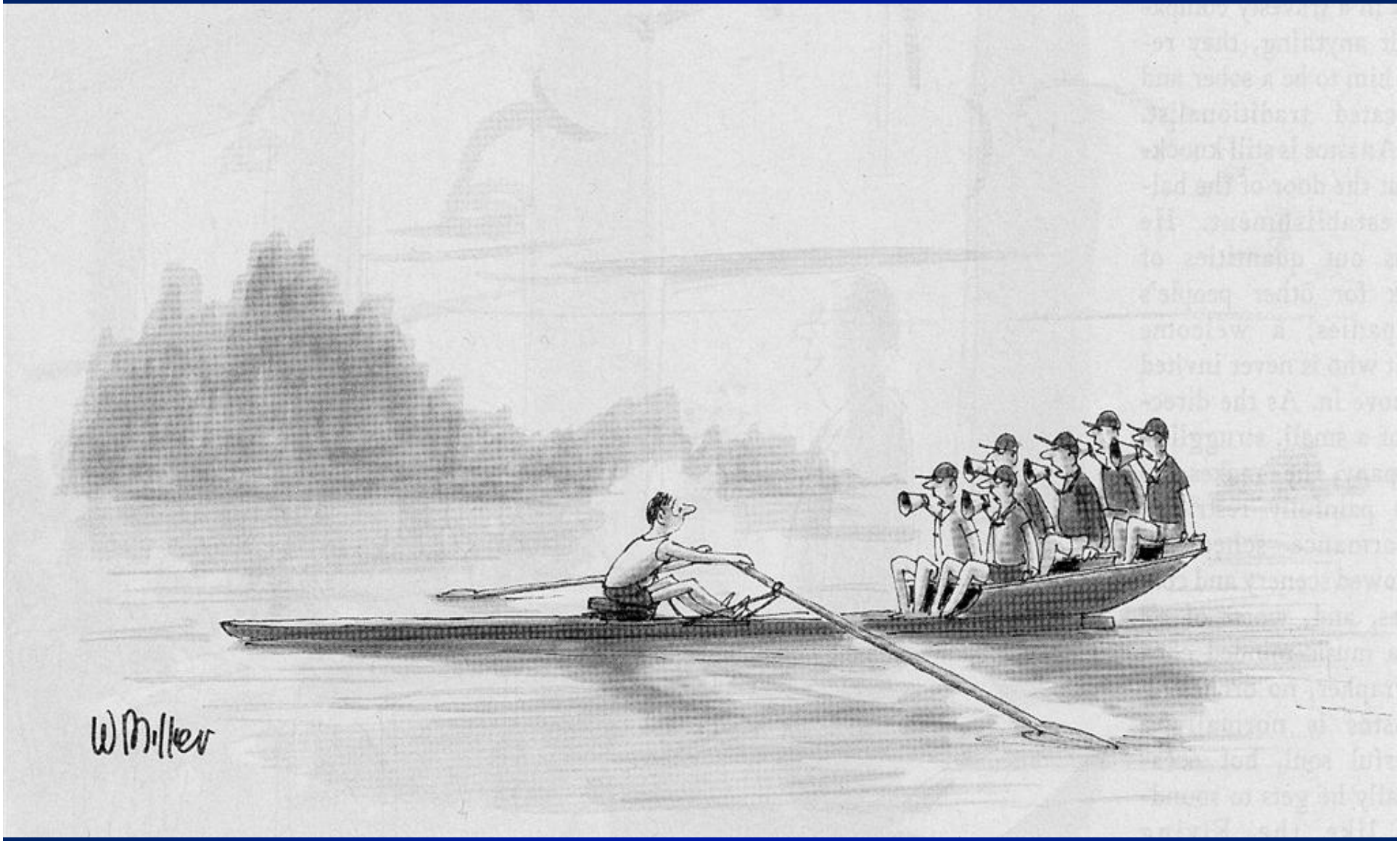
- low-power ADCs
- low-power DSP (auto-calib., data red., program., ...)
- low-power high-speed communication (standards)
- low-power low-voltage analogs
- high dynamic range, waveform sampling
- high-density interconnects (2.5D, 3D - incl. sensors)
- cryogenic
- MAPS
- ...

When to exit/enter a technology ?

- exit too late may result in limited collaborations
- enter too early may result in waste of resources

Source: [TIPP]

IC Designer in a “Collaboration”



Source: [TIPP]

Références (1)

[BRA] "Aperture Uncertainty and ADC System Performance", Brad Brannon et Allen Barlow, AN-501 Analog Devices 2006

[DAN] L'actualité des Composants du CNES, n°26 – 2007, D.Danglan et F.Malou

[AT84] Data sheet et Application Note AT84AS008 de e2v, http://www.e2v.com

[CHAR99] Charoix, AEMC, Ecole d'électronique analogique de Cargèse 1999

[CHAR05] Charoix, AEMC, Ecole de microélectronique de Porquerolles 2005

[AN1636] AN1636: Understanding and minimising ADC conversion errors, ST-2003

[LEC] Cours de J.Lecoq

[CATT] "Clocking High-Speed A/D Converters", National Semiconductor, Application Note 1558, James Catt, January 2007

[LAL] Rapport d'activités du LAL 2005-2007 (http://electronique.lal.in2p3.fr/rapports/Rapport_2007/Rapport_2007.html)

[PER] G.Perrot, Electronique ATLAS LArg pour le SLHC, 13/03/2007 (http://lappagenda.in2p3.fr/cdsagenda/askArchive.php?base=agenda&categ=a0728&id=a0728s9/moreinfo/Elec_Upgrade_SLHC_13mar07.ppt

[SMU] The AD9042 Evaluation System, SMU-HEP-04-04, Tiankuan Liu, Benjamin Wakeland, Xiao Wu and Jingbo Ye, Physics Department, Southern Methodist University, Dallas, USA

Références (2)

[LSST1] SLAC Program Review, Kirk Gilmore, Stanford/SLAC/KIPAC, June 7, 2006

[LSST2] LSST Camera Electronics, John Oliver, 21 août 2006

[CMS1] Pierre Depasse (IPN Lyon) IXth International Conference on Calorimetry In Particle Physics Calor 2000, Annecy, October 9-14 (wwwlapp.in2p3.fr/Calor2000/Contributions/Electronics/pierre_depasse.PDF)

[CMS2] "Radiation hardness evaluation of the AnalogDevices AD9042 ADC for use in the CMS electromagnetic calorimeter", P. Denes*, B. Lev, R. Wixted, Nuclear Instruments and Methods in Physics Research A 417 (1998) 371—376

[BER] "Convertisseurs Analogique/Numérique & Convertisseurs Numérique/Analogique", Serge BERNARD, Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier (LIRMM)

[IEEE] "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters", IEEE Std 1241-2000

[Atlas-Lar] “Atlas Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report", ERN-LHCC-2013-017 / ATLAS-TDR-022, 02/12/2013

[TIPP] Trends in front-end ASICs for particle physics, http://indico.cern.ch/event/192695/session/1/contribution/433