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Jitter Transfer Measurement in Clock Circuits

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Abstract

With increasing transfer rates and lower jitter margins, the performance of clock generation circuits has become of increasing importance. A key measurement of the performance of clock circuits is jitter transfer which is the ratio of the jitter present at the output of a clock generator to the jitter applied at its reference input. This paper will provide a background discussion of jitter transfer as well as the proper techniques for measuring this important parameter on clock generation circuits and will include example measurements on representative hardware.

Author(s) Biography

Michael Schnecker is a Business Development Manager at LeCroy Corporation. Mr. Schnecker specializes in signal integrity measurements including jitter and has been instrumental in specifying and deploying the LeCroy SDA series instruments. He holds a BS degree from Lehigh University and MS degree from the Georgia Institute of Technology both in electrical engineering and has 18 years of experience in the test and measurement industry.

Introduction

Jitter transfer is a measure of the jitter present on a signal at the output of a device under test relative to the jitter applied at its input and is measured as the ratio of these two quantities. This measurement can apply to clock or data signals but for this paper we will concentrate on measuring clock signals. Jitter transfer is measured by applying a known amount of timing deviation at a given rate to the input clock of the DUT and measuring the timing deviation at the same frequency at the DUT output. In order to provide the most accurate measurement, the jitter is measured on both the input and output signals by the same instrument, in this case an oscilloscope. The rate and amplitude of the applied jitter dictate the measurement methods that must be used both to verify the applied jitter and measure the corresponding value at the output of the DUT. For example, long acquisition times are required to measure jitter at low rates while large timing deviations are required at the DUT input at rates where the jitter transfer is very low.

Another important factor in measuring jitter in general and jitter transfer in particular is the observed jitter transfer function of the instrument. Oscilloscopes used for measuring jitter generally use some sort of numerical PLL to track the average signal rate and generate a phase reference for measuring jitter or more specifically time interval error (TIE). The method used to generate this reference results in varying measurement sensitivity as a function of the jitter rate. This variation constitutes the observed jitter transfer function of the instrument (OJTF). The OJTF of the measurement instrument impacts the measured jitter as a function of the rate and must be taken into account when measuring the jitter particularly at the DUT output. The OJTF of typical jitter measurement devices is less sensitive at low jitter rates where the recovered reference clock tracks the jitter of the input signal. In these cases, the numerical PLL must be adjusted or disabled to provide a measurable jitter number at the DUT output.

This paper will discuss the theory of phase locked loops, their transfer functions and how they are used to generate reference clocks for receivers and jitter measurement devices. The observed jitter transfer functions of several common PLL types will be developed as examples. The final section of this paper will present two measurements of jitter transfer function on clock circuits as an example of the measurement method.

Phase locked loops

A simplified clock generation circuit is shown schematically in figure 1. The circuit is a phase locked loop consisting of a reference input, phase detector, gain stage and a low pass filter. The actual components used in practical PLL implementations vary but the overall operation is the same and this circuit can be used to analyze their behavior. The VCO generates a clock output which is proportional to the control voltage applied to its input. The control voltage is, in turn, proportional to the phase difference between the reference signal and the output of the VCO when the loop is closed. The open loop response is given by the cascade of the low pass filter, gain stage and VCO. The phase output of the VCO is the integral of the frequency and is represented by 1/s in Laplace

transform notation. The open loop response is shown in equation 1. The two constants are the phase detector transfer function and VCO transfer function.

$$A(s) = \frac{K_\phi K_{vco} H(s)}{s} \qquad (1)$$

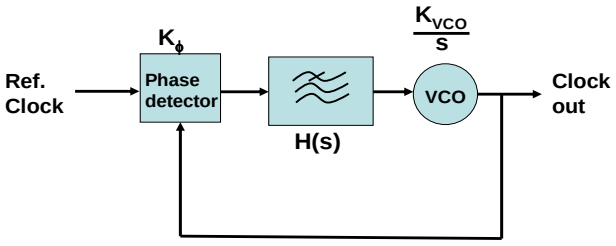

Figure 1: schematic view of a phase locked loop

PLL closed loop transfer function

Phase locked loops are classified by their closed loop response in terms of the class and order. The PLL transfer function given by the closed loop response can be derived from the open loop response by noting that the output phase is the product of the input phase and the open loop response and that the input phase is the difference between the reference phase and the output phase:

$$\begin{aligned} &(\Phi_r - \Phi_o)A(s) = \Phi_o \\ &A(s)\Phi_r = \Phi_o + A(s)\Phi_o \\ &\frac{\Phi_o}{\Phi_r} = \frac{A(s)}{1 + A(s)} \end{aligned} \qquad (2)$$

The simplest form for the open loop transfer function is when the filter in figure 1, H(s) is a constant. In this case, equation 1 reduces to:

$$A(s) = \frac{K_\phi K_{vco} H}{s} = \frac{\omega_1}{s} \qquad (3)$$

The PLL transfer function for this basic case combining equations 2 and 3 is:

$$\frac{\Phi_o}{\Phi_r} = \frac{\omega_1 / s}{1 + \omega_1 / s} = \frac{\omega_1}{s + \omega_1} \qquad (4)$$

Equation 4 is the response of a single-pole low pass filter with a 20 dB/decade roll off above the cutoff frequency, ω_1. This simple form of PLL is not generally used for clock

generation circuits but it has wide application in instrumentation as a reference clock generator for jitter measurements. In these applications, equation 4 describes the transfer function of a "golden" PLL and the cutoff frequency is set by the gain terms in the open loop response to a ratio of $\omega_i/1667$ where ω_i is the frequency of the reference input.

The VCO in figure 1 has one integrator (division by s in the Laplace domain). The number of integrators in the open loop transfer function determines the type of the PLL. The order is determined by the number of poles in the closed loop response. The golden PLL discussed above is a type 1 first order PLL.

Another important PLL type is formed by adding a zero to the open loop response. In this case, the open loop transfer function becomes

$$A(s) = \frac{\omega_1}{s}\left(1 + \frac{\omega_2}{s}\right) = \frac{\omega_1 s + \omega_1\omega_2}{s^2} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2}$$
$$\omega_n = \sqrt{\omega_1\omega_2}, \zeta = \frac{1}{2}\sqrt{\frac{\omega_2}{\omega_1}} \qquad (5)$$

This type of PLL is known as 2nd order type 2 because there are two integrations in the open loop response. The transfer function of this PLL is

$$\frac{\Phi_o}{\Phi_i} = \frac{A(s)}{1 + A(s)} = \frac{\frac{2\zeta\omega_n s + \omega_n^2}{s^2}}{1 + \frac{2\zeta\omega_n s + \omega_n^2}{s^2}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad (6)$$

Equations 5 and 6 use the notation ω_n for the natural frequency and ζ for the damping factor. This type of PLL has become important for generating the phase reference for jitter measurements for cases where SSC (spread spectrum clocking) is employed. The higher order jitter transfer function provides better tracking of the 30 KHz modulation rate of the clock frequency used by the SSC while allowing the 3dB cutoff to remain at a relatively low frequency. The closed loop response curves for the 1st and 2nd order PLL's are shown in figure 2.

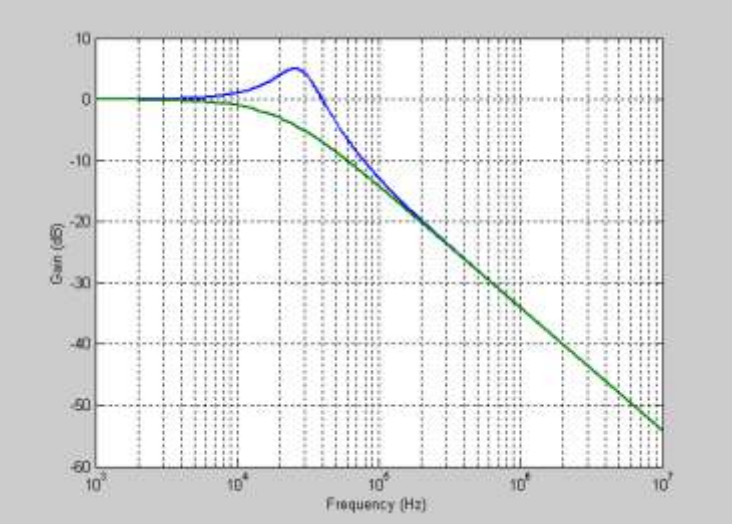

Figure 2: Jitter transfer function for 1st order type 1 and 2nd order type 2 PLL. The damping factor is .707 for the 2nd order PLL and the cutoff and natural frequencies are 100 KHz.

Observed jitter transfer function

The observed jitter transfer function or OJTF is the phase response of a system which uses a PLL to generate its reference clock. In the case of a serial digital receiver, the PLL recovers the clock used to detect the data bits being received. The OJTF is given by 1-JTF:

$$OJTF = 1 - JTF = 1 - \frac{A(s)}{1 + A(s)} = \frac{1}{1 + A(s)} \qquad (7)$$

The OJTF has a high pass frequency response so jitter significantly below the cutoff frequency is not observed and in the case of a jitter measurement device, is not measured. The observed jitter transfer function gives the amount of jitter which is tracked and therefore not observed at the output of the system as a function of the jitter rate applied to the input. The OJTF applies to the system shown in figure 3 where the output is the phase difference between the recovered clock via a PLL and the phase reference at the input.

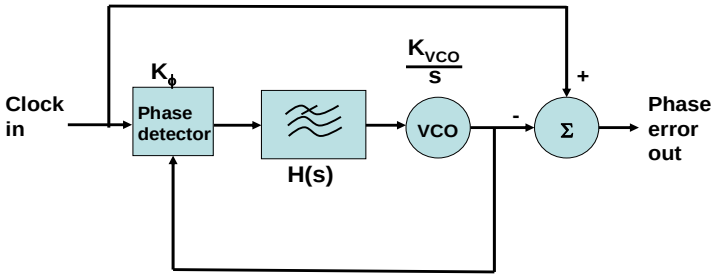

Figure 3: Phase error measurement using a PLL to generate the reference

The OJTF for the two PLL examples above are shown in figure 4. Equations 8 and 9 show the OJTF for the 1st and 2nd order phase locked loops.

$$OJTF_1 = \frac{1}{1+A(s)} = \frac{1}{1+\omega_1/s} = \frac{s}{s+\omega_1} \qquad (8)$$

$$OJTF_2 = \frac{1}{1+A(s)} = \frac{1}{1+\frac{2\zeta\omega_n s+\omega_n^2}{s^2}} = \frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2} \qquad (9)$$

The OJTF for the 2nd order PLL has zeroes at 0 and $2\omega_n\zeta$ and poles at:

$$\omega_n\zeta \pm \omega_n\sqrt{\zeta^2-1} \qquad (10)$$

The damping factor shifts the cutoff frequency depending on its vale. A damping factor of 0.707 gives poles at:

$$\frac{\omega_n}{\sqrt{2}}(1\pm j) \qquad (11)$$

These pole locations give a cutoff frequency at the natural frequency with overshoot in the frequency response. If the damping factor is 0.5, there are 2 poles at the natural frequency and the frequency response has no overshoot.

The combination of the OJTF of a jitter measurement device and the JTF of the clock generator under test gives the measured jitter as a function of frequency. For example, a clock generator with a type 1, 1st order PLL measured with a jitter measurement device employing a golden PLL is:

$$J = JTF_c OJTF_s = \frac{\omega_1}{s+\omega_1}\frac{s}{s+\omega_2} \qquad (11)$$

The jitter measurement has a frequency response with poles at ω_1 and ω_2 which are the corner frequencies of the clock and jitter measurement device respectively. The overall response is a band pass filter because the clock JTF is low pass and the jitter measurement device OJTF is high pass. Accurate measurement of the clock JTF requires that the OJTF cutoff of the jitter measurement be significantly below that of the clock JTF and that the measurement is compensated for the instrument's OJTF. The compensation for the instrument OJTF is performed by measuring the jitter of the reference clock at each jitter rate being tested and comparing the reference jitter with the jitter measured at the output of the DUT.

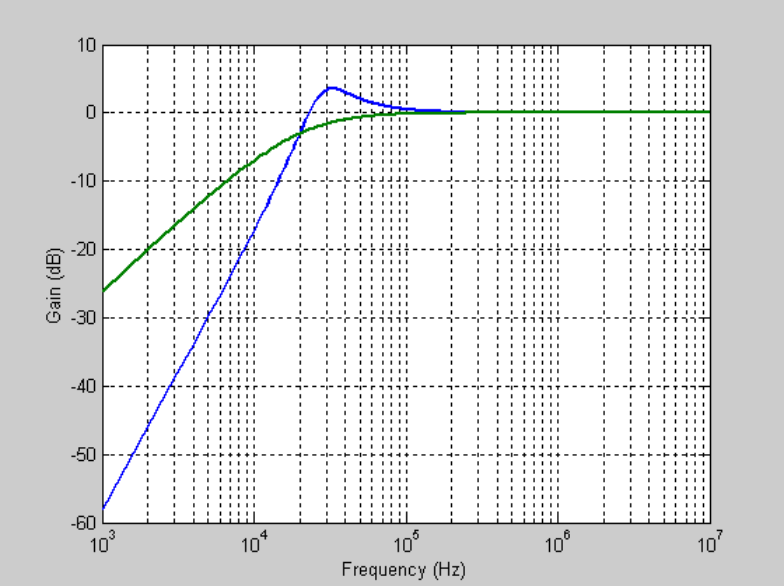

Figure 4: OJTF for 1st and 2nd order PLL

The open loop, closed loop and jitter transfer function are all related. Table 1 shows the relationships among them. Given any one of the three, any other of the transfer functions can be generated.

Table 1: Relationships among open loop transfer function (A), JTF and OJTF.

	JTF(s)	A(s)	OJTF(s)
JTF(s)	-	$\frac{A(s)}{1+A(s)}$	$1-OJTF(s)$
A(s)	$\frac{JTF}{1-JTF}$	-	$\frac{1-OJTF(s)}{OJTF(s)}$
OJTF(s)	$1-JTF(s)$	$\frac{1}{1+A(s)}$	-

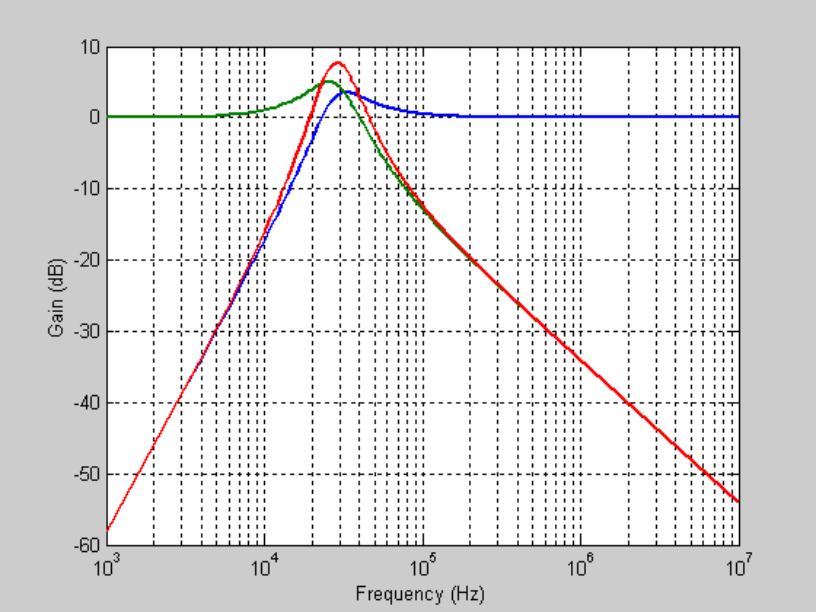

Figure 5: Jitter response (red trace) for a measurement with OJTF (blue trace) on a device with JTF (green trace)

Figure 5 shows the response of a jitter measurement device which uses a 2nd order type 2 PLL to generate its phase reference. The device under test is a clock also with a 2nd order type 2 PLL. The measured response near the cutoff of the DUT has a significant error when the cutoff of the PLL in the measurement is near that from the DUT. Lowering the cutoff of the PLL in the measurement reduces the error at the DUT cutoff as shown in figure 6. The OJTF of the measurement system has a high pass characteristic so the JTF measured below the DUT cutoff will still contain an error.

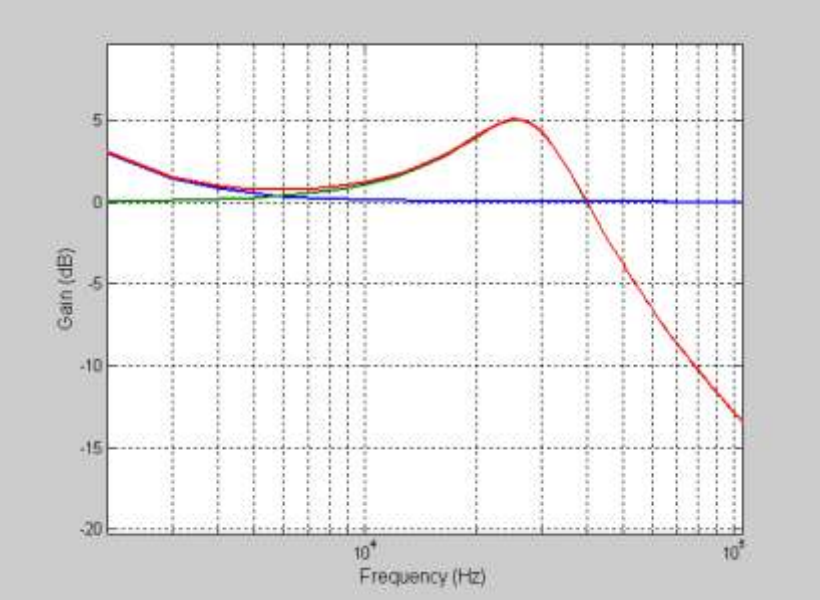

Figure 6: Jitter response (red trace) for a measurement with OJTF (blue trace) with a cutoff at 1/10 that of the DUT with JTF (green trace).

The lower the cutoff frequency of the jitter measurement device the better the accuracy of the measurement will be. The cutoff frequency is limited by several factors including the phase noise of the DUT and measurement time. These factors will be addressed in the next section on measurement considerations.

Measuring the jitter transfer function

Instrument observed jitter transfer function

The jitter transfer function of a clock can be measured by a variety of instruments but the most popular instrument for this type of measurement is the digital sampling oscilloscope or DSO. The DSO acquires the clock signal and measures the phase of each transition by determining the time at which the clock waveform crosses a pre-determined amplitude threshold. A number of consecutive clock transitions are measured and their phases are accumulated in a phase vs. time record.

The raw phase vs. time information can be plotted and measured to directly show the jitter or accumulated in a histogram to view the statistical distribution of the jitter. The jitter track is essentially a sampled waveform representing the phase of each transition and has a sampling rate equal to the clock frequency. The highest frequency component of the jitter measurement is ½ the clock rate according to the Nyquist sampling theorem. The lowest measurable jitter rate in the record is determined by the observation time. In addition to the frequency limitations resulting from the limited observation time, the phase of the clock transitions can exceed one period of the clock over the observation time. The excess phase is controlled by using a software phase locked loop to derive a

reference clock from the measured clock phase and subtracting the reference phase from the measured clock phase. This operation is shown schematically in figure 7.

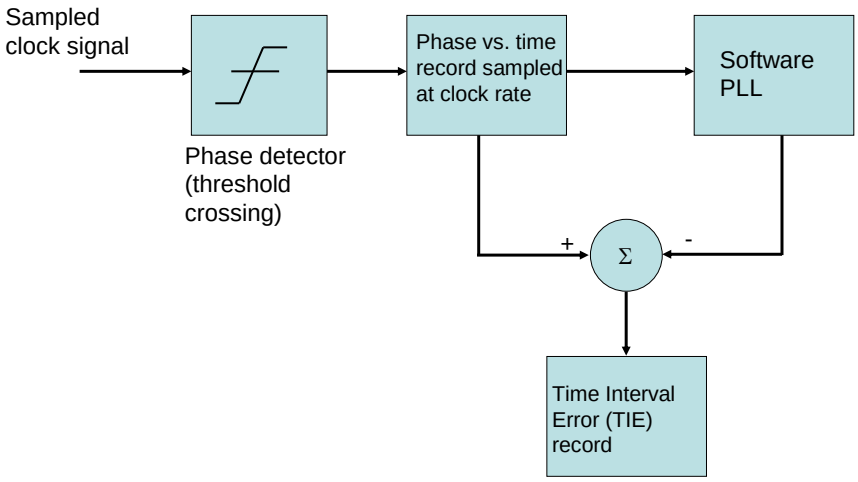

Figure 7: Flow diagram of jitter measurement on a DSO using software PLL

Figure 8 shows the TIE (Time Interval Error) track and histogram measured on a clock signal. The histogram provides valuable information about the long term variations in the timing while the track provides a direct view of how the phase of the clock evolves over time. In many cases, the jitter modulation can be directly viewed and measured in the track. In other cases, it is necessary to transform the track into the frequency domain using an FFT so that the individual frequency components of the jitter can be measured. The processing gain of the FFT allows jitter at specific rates to be measured down to the femto-second range.

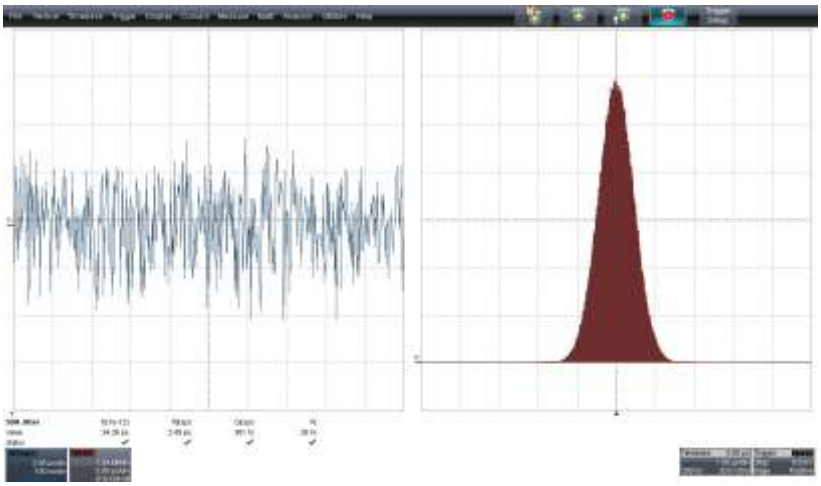

Figure 8: Track (left) and histogram (right) of jitter measurements on a clock signal

A 1st or 2nd order PLL is implemented in software on the phase samples from the clock under test. The recovered clock is discrete, however, and limited in duration as a result of the finite record length. The record length sets the minimum frequency of the JTF that can be measured. Figure 9 is a plot of simulated jitter measurements using a 1st order PLL phase reference and record lengths of 2 micro-seconds and 20 micro-seconds. The PLL loop bandwidth is 533 KHz and the ideal response is plotted in blue. The red trace is the measured response using a 2 us record length which includes one complete cycle of a 500 KHz sine wave. The measured p-p Pj falls below the ideal response as the jitter rate is reduced due to the limited record length. The green trace is for a 20 us record length which allows the capture of a complete cycle of a 50 KHz sine wave. The 20 us record matches the ideal response very well at the cutoff frequency and the error remains small at rates below the cutoff. Maintaining the record length at a minimum of 1/10 of the inverse of the PLL loop bandwidth minimizes the response error.

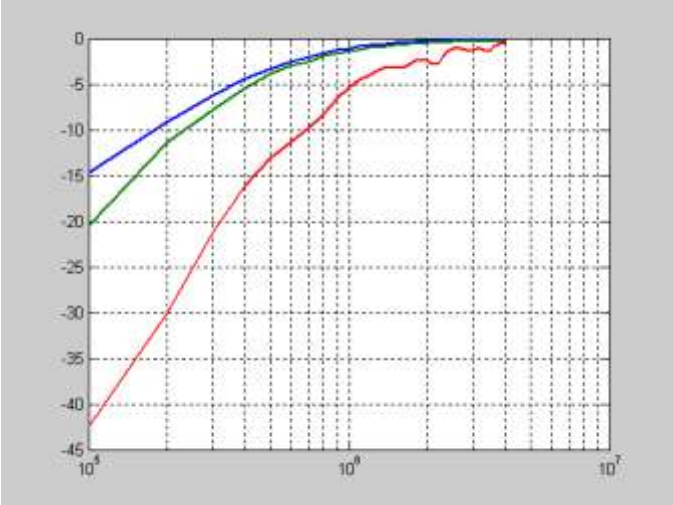

Figure 9: OJTF for 2 us and 20 us record lengths compared to the ideal response for an OJTF with a 533 KHz cutoff.

Injecting jitter with phase modulation

The JTF is measured by adding jitter to the phase reference of the clock and measuring the phase deviation (jitter) on the clock. The jitter transfer is the ratio between the injected jitter and the jitter on the clock signal which is plotted as a function of the rate of the injected jitter. The measurement is a 2-step process; measure the injected jitter on the reference at each rate and measure the clock jitter at each rate. The calibration step is necessary to compensate for the OJTF of the jitter measurement system and the source used to inject jitter on the reference clock.

The most direct way of injecting jitter on the reference clock is by using phase modulation. There are a number of clock sources which feature phase or delay modulation which can be used for this purpose. When injecting jitter, one must keep in mind the expected jitter transfer function. For example, if the JTF is expected to be on the order of -40 dB at a particular frequency the one must inject a sufficient amount of jitter

at that rate in order to have a measurable jitter level on the clock signal. The minimum measurable jitter is determined by the jitter noise floor of the jitter measurement device or JMD. In the above example, if the noise floor of the JMD is 500 fs RMS then the residual jitter from the clock under test should be 5 ps RMS or more. With a -40 dB JTF, it would be necessary to inject at least 500 ps RMS (1.414 ns p-p for sine wave modulation) of jitter in order to have a measurable residual jitter. The modulated clock source must be capable of generating this amount of jitter.

Injecting jitter with frequency modulation

In many cases, phase modulation is not capable of generating the required amount of jitter. An alternate method is to use FM on the reference clock. Frequency is the derivative of phase; f = dϕ/dt. Using sinusoidal jitter modulation simplifies this because the derivative of a sine wave is a cosine wave which preserves the modulation shape.

Equations 12 describe the reference clock frequency and phase when FM is used to inject jitter. The phase has a sinusoidal variation and its p-p value is equal to the FM deviation divided by the jitter frequency multiplied by the period of the reference clock.

$$f_{clk} = 2\pi f + 2\pi f_D \sin(2\pi f_j t) = \frac{d\phi}{dt}$$

$$\phi(\tau) = \int_0^{\tau} 2\pi f + 2\pi f_D \sin(2\pi f_j t)dt = 2\pi f\tau - \frac{2\pi f_D}{2\pi f_j}\cos(2\pi f_j \tau) \qquad (12)$$

$$Pj(p-p) = \frac{T_{clk} f_D}{2\pi f_j}$$

For the special case of sine wave modulation, FM can be used to inject jitter into the reference clock. An additional benefit of FM is that much higher peak phase deviations can be achieved. A typical synthesized sine wave generator has frequency modulation which is suitable for jitter injection.

Example measurements

Narrow loop bandwidth clock cleaner chip

The first measurement example uses a “clock cleaner” chip. This device is designed to improve the jitter of a reference clock applied to its input. The device works by employing a narrow bandwidth PLL which gives it a JTF that rejects all but the lowest frequency jitter present at the reference input. The JTF of this chip is characterized by a low cutoff frequency and high jitter rejection.

Figure 10 shows the measured JTF of this chip for offset frequencies ranging from 100 Hz through 10 KHz. The JTF was measured at 300, 400, 500, 1000, 3000 and 6000 Hz. The measurement setup is shown in figure 11. A synthesizer was used to generate the

reference clock at a frequency of 61.44 MHz and FM was added to the signal to inject the jitter.

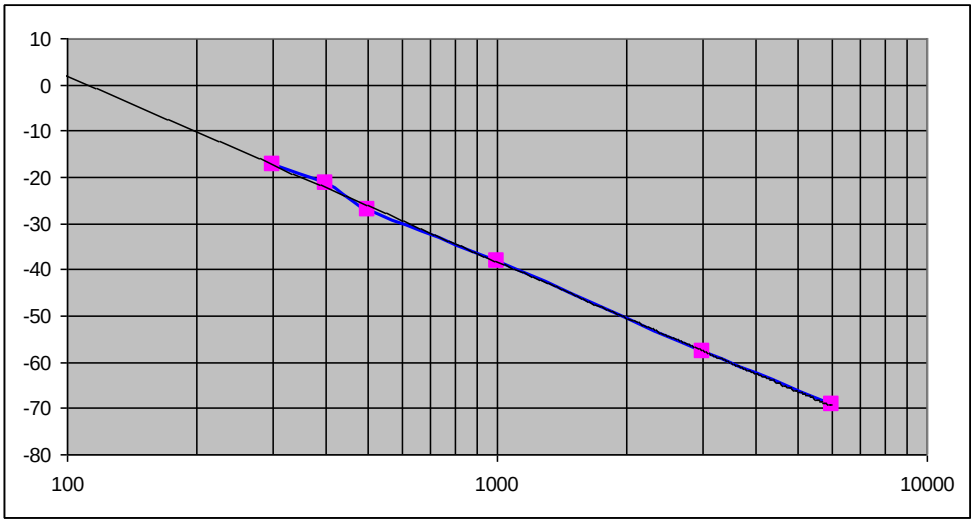

Figure 10: jitter transfer function of clock cleaner chip. The trend line is drawn to indicate the 3 dB point

The FM was adjusted following equations 12 to provide a suitable amount of jitter to measure the JTF. The FM deviations for each rate are shown in table 1 along with the expected peak to peak periodic jitter for each rate. The deviations were chosen to maximize the Pj at the DUT input so that the attenuated jitter at the DUT output would be as high as possible. The maximum Pj was limited to prevent the PLL in the DUT from losing phase lock. The deviation was increased for rates above 500 Hz because the residual jitter on the clock became immeasurable owing to the very high rejection above this offset (greater than 40 dB). Also, because FM is being used, the higher rate requires a larger offset to maintain a high peak jitter. The FM deviation and equivalent peak to peak periodic jitter are summarized for each rate in table 2.

Table 2: FM rate, deviation and equivalent Pj for the injected jitter used to test the clock cleaner chip

FM Rate	FM Deviation	p-p Pj
300	2 KHz	17.3 ns
400	2 KHz	12.96 ns
500	2 KHz	10.37 ns
1000	6 KHz	15.6 ns
3000	6 KHz	5.18 ns
6000	12 KHz	5.18 ns

Table 3 shows the measurement results for the 6 jitter rates tested. The identical settings were used in the jitter measurement device to measure the input and output jitter. Note that the actual p-p jitter at each rate is not exactly equal to the expected value as listed in table 1 but by measuring the input and output at each jitter rate, this error does not impact the JTF measurement.

Table 3: Measured jitter at DUT input and output.

Jitter rate	Measured p-p Pj at DUT input (ps)	Measured p-p Pj at DUT output (ps)	JTF (dB)
300	18100	2469	-17.3031
400	13887	1200	-21.2685
500	11129	491	-27.1075
1000	14600	181	-38.1335
3000	5506	7	-57.9148
6000	5721	2	-69.1288

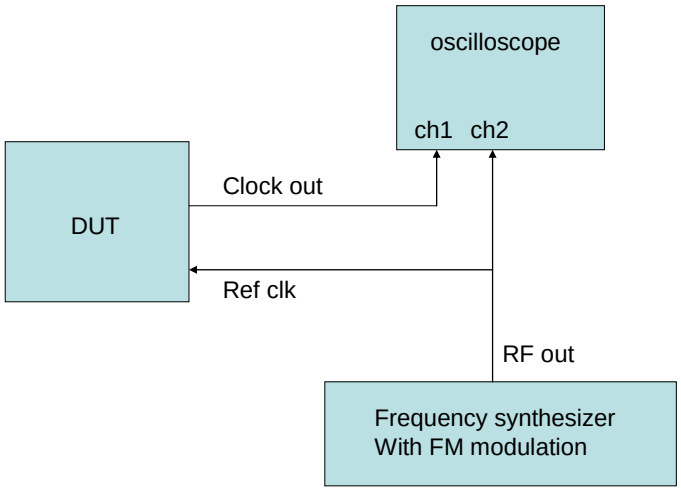

Figure 11: measurement configuration for JTF of clock cleaner chip

The jitter was measured by computing the FFT of the TIE measurements acquired over a single acquisition. This record is sampled at the clock rate (one measurement per period of the clock) so the frequency range of the FFT was 0 Hz to 30.72 MHz. The use of the FFT allows for accurate measurement of the injected jitter by measuring the frequency bin corresponding to the rate of the injected jitter. This technique prevents measuring jitter at frequencies other than that of the injected jitter such as spurious FM in the clock source. It is also possible to measure the p-p value of the jitter track but this method is only effective when the jitter is very high. Figures 12 through 15 show the track and spectrum for the jitter on the reference clock and output clock at a jitter rate of 6 KHz. The very high jitter rejection at this rate makes it impossible to measure the output jitter directly from the jitter track however; the jitter spectrum allows the residual jitter at 6 KHz to be clearly seen.

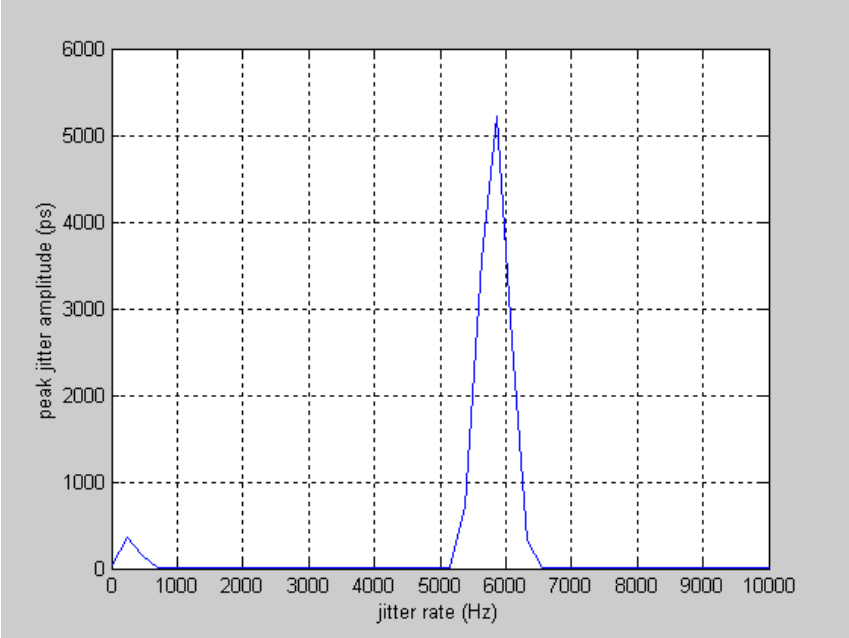

Figure 12: jitter spectrum of the reference clock at the DUT input with 6 KHz injected jitter

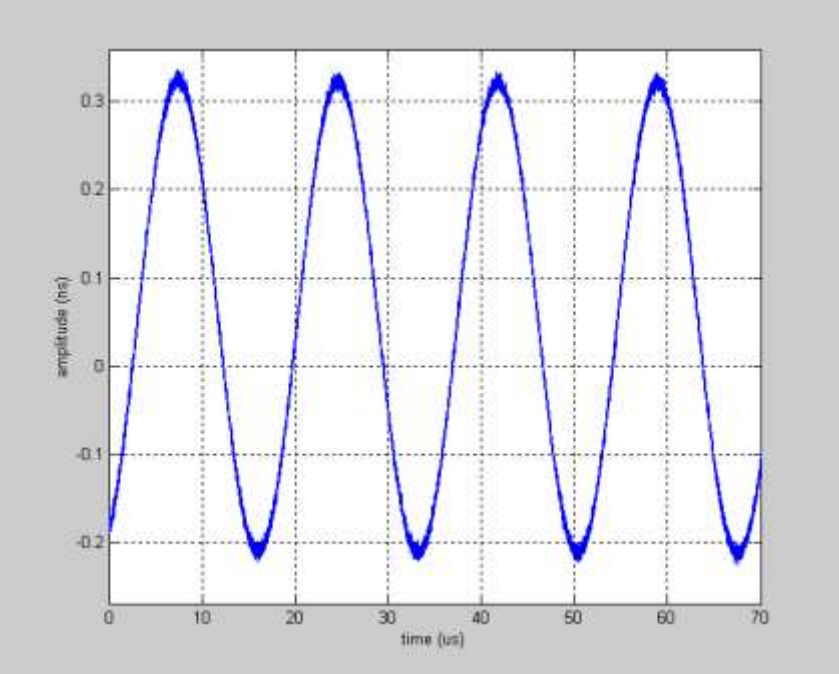

Figure 13: jitter track of reference clock with 6 KHz injected jitter. Note the modulation is clearly evident and easily measurable.

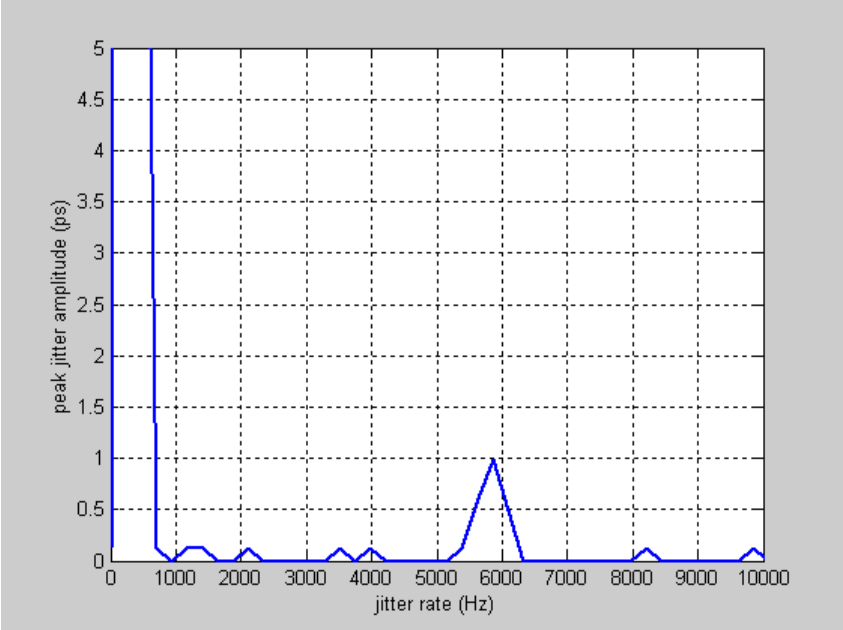

Figure 14: jitter spectrum of the DUT output with 6 KHz injected jitter. The peak at 6 KHz is the residual jitter.

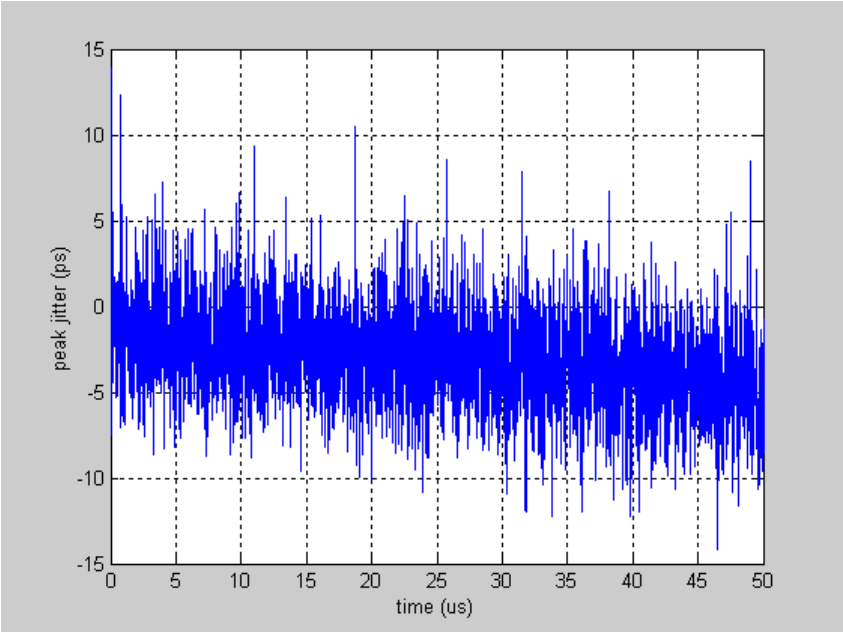

Figure 15: jitter track of the output of the DUT. Note that the injected 6 KHz jitter is below the noise and not visible in the time domain.

The very low jitter rates required to measure the JTF required long acquisitions of data. At 300 Hz, one cycle of the jitter was 3.33 ms and at a sampling rate of 20 GHz, a 100 M sample acquisition was required to see 5 ms which allowed one cycle of the 300 Hz jitter to be captured. While the software PLL is normally used to generate the phase reference for jitter measurements as shown in figure 7, the low rates used for this measurement

prevented its use and an absolute time interval was used as a phase reference for these measurements.

Figure 16 shows the JTF of a type 1 2nd order PLL superimposed on the measured response of the clock cleaner chip. The 2nd order PLL response had a natural frequency of 110 Hz and a damping factor of 0.5. The measured response of the clock cleaner chip matches the ideal 2nd order PLL exactly so we can conclude that the chip contains a 2nd order PLL.

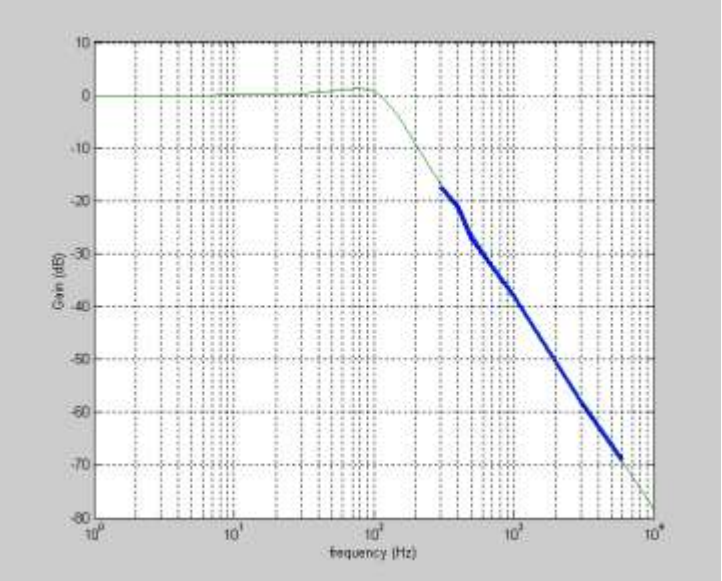

Figure 16: Measure jitter transfer function (bold line) superimposed on an ideal 2nd order PLL JTF.

High Speed Serial Data Transmitter

Serial data transmitters generally use an on-chip clock generator which uses an external reference oscillator. The output of the clock is inaccessible however its jitter can be seen on the data signal at the transmitter output. The PLL in the clock circuit for this application has a much wider bandwidth than the clock chip measured above. The measurement technique is similar, however.

For this device, a differential clock source with phase modulation was used as the reference clock for the on-chip PLL. The jitter on the data signal transmitted from the chip was measured as the clock source was modulated with varying rates of phase jitter. The injected RMS jitter was held at a constant 30 ps for all jitter rates. As was the case for the clock cleaner, the periodic jitter or Pj was measured for both the clock source and the data signal at the rate of the injected jitter.

Unlike the clock signal, the data signal is coded in NRZ format and so it does not have a transition for every bit interval. This presents a problem when computing the FFT because the transform requires a fixed sampling interval. In order to maintain this fixed

interval “virtual” transitions are inserted into the phase vs. time sequence for those bit intervals where the data signal does not have a transition. The location of the virtual transitions is determined by linear interpolation between the phase measurements of the transitions surrounding the missing ones.

The measured jitter values for the transmitter are shown in table 4. The injected jitter rates are much higher than those used for the clock cleaner so the acquisition lengths on the oscilloscope were much shorter.

Table 4: Jitter measurements for serial data transmitter

Jitter rate	peak injected Pj (ps)	peak output Pj (ps)	Jitter transfer (dB)
1.00E+05	30	25.6	-1.37763
2.00E+05	30	25.6	-1.37763
4.00E+05	30	26.8	-0.97973
8.00E+05	30	24.8	-1.65339
1.00E+06	30	26.4	-1.11035
2.00E+06	30	26.4	-1.11035
5.00E+06	30	22	-2.69397
1.00E+07	30	15	-6.0206
1.50E+07	30	10	-9.54243
2.00E+07	30	7.65	-11.8692
2.50E+07	30	6	-13.9794
3.00E+07	30	4.3	-16.8731
3.50E+07	30	3.48	-18.7108
4.00E+07	30	2.88	-20.3546
5.00E+07	30	1.86	-24.1522
6.00E+07	30	1.44	-26.3752

The 3 dB cutoff for the JTF on this device is 5 MHz and the roll-off has a 20 dB/decade slope which is consistent with a first order PLL. The JTF is plotted in figure 17 along with an ideal first order PLL with a cutoff of 6 MHz. The jitter rejection is somewhat higher than a first order PLL would provide at high offset frequencies so this clock is more complex than a simple first order.

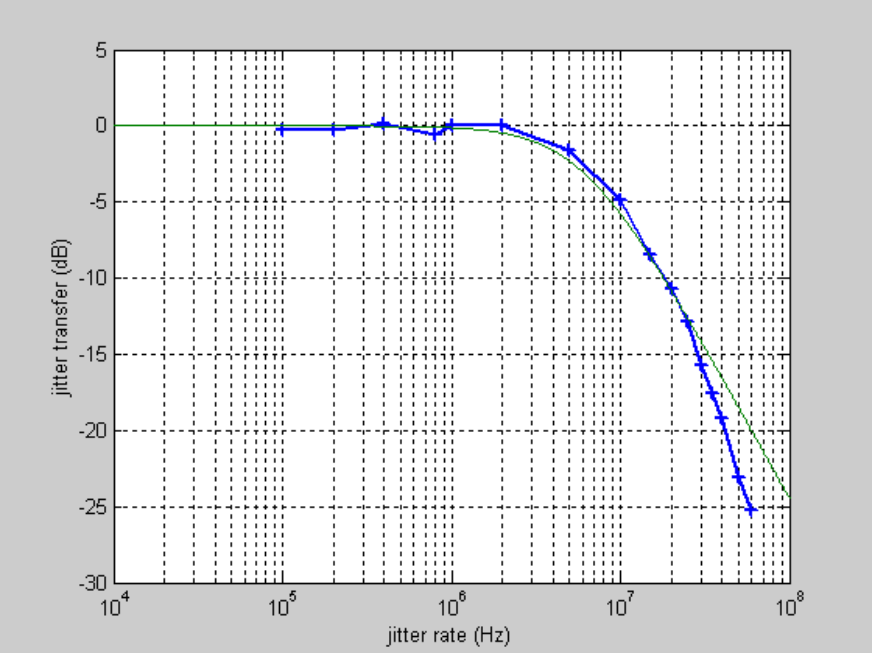

Figure 17: Jitter transfer function of 3 Gb/s serial data transmitter. The thin trace is that of an ideal 1st order PLL with a 6 MHz cutoff

Conclusion

Understanding the jitter transfer function of clock generation circuits is critical to their effective use in many applications. The JTF can be effectively characterized using a digital oscilloscope and a clock source with either phase or frequency modulation. Since the JTF is the ratio of the output jitter to the applied jitter on the reference clock, both signals must be measured as a function of frequency. The oscilloscope settings must be the same for both measurements (the applied and output signals) and one must pay careful attention to the acquisition time of the measurement as the low frequency limit is set by the observation time. A rule of thumb is to acquire 10 times the period of the lowest frequency component when possible. The amount of injected jitter must also be increased to a sufficient level for those areas of the measurement where the JTF is very small. Enough jitter must be injected to allow sufficient residual jitter at the DUT output to measure the ratio. The use of an FFT of the TIE measurement sequence improves the accuracy of JTF measurements in two ways. First, the processing gain of the FFT improves the jitter noise floor of the measurement allowing very small residual jitter values to be measured and, second, the specific frequency of the injected jitter can be measured at the input and output thereby avoiding any inaccuracies caused by imperfect jitter injection equipment.

References

Jim Stimple, *Clock Synthesis, Phase Locked Loops, and Clock Recovery*, Digital Communications Test and Measurement (chapter 9), Prentice Hall, 2008