irfu

cea

saclay

DAC 10 Bits « MultiLSB »

Ecole de Microélectronique

La Londe les Maures

12 – 16 Octobre 2009

fabrice.guilloux@cea.fr on behalf IRFU's group

Constrains of the Design

irfu cea saclay

❖ The KM3NET design study

- ⊙ Underwater neutrino telescope (potential sites on fig 1)
- ⊙ Cherenkov light detection from photo-multiplicator tubes (PMTs on a tower - fig 2)
- ⊙ Choice of detection unit not done yet : 31x3'' PMTs vs 1x8'' PMT (fig 3a & fig3b)

➔ **Need of a flexible electronics**

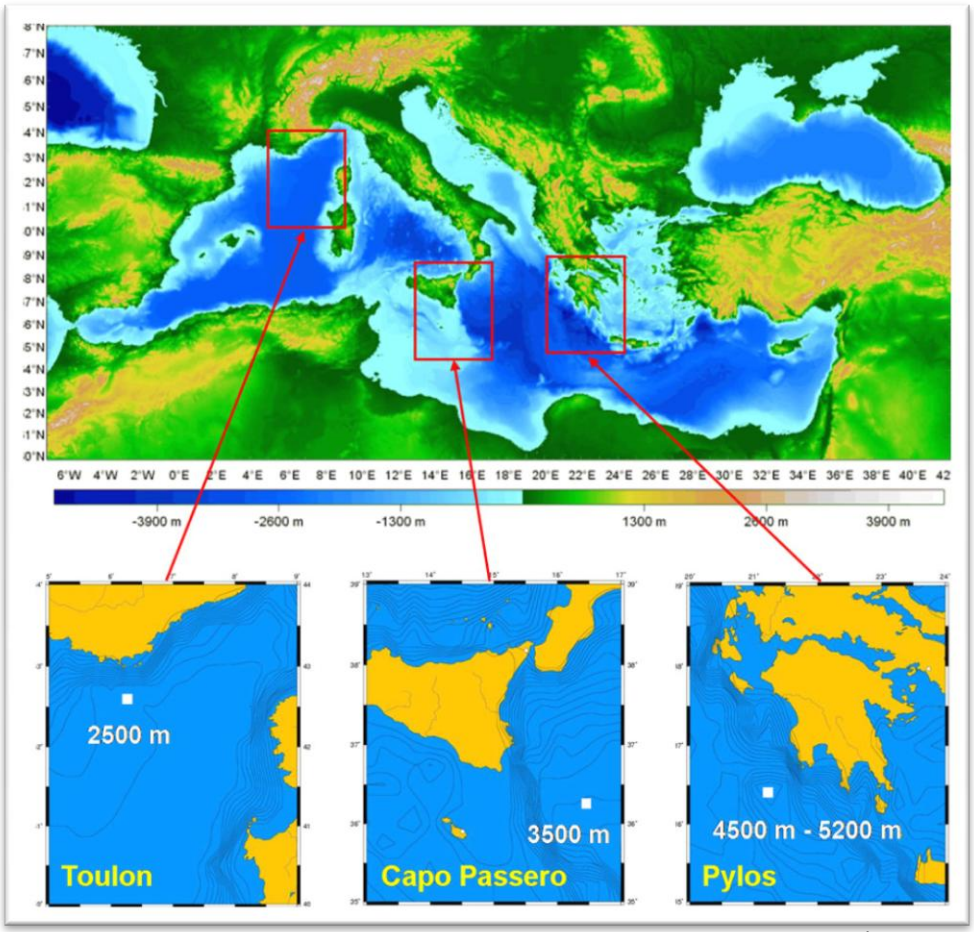


Fig 1

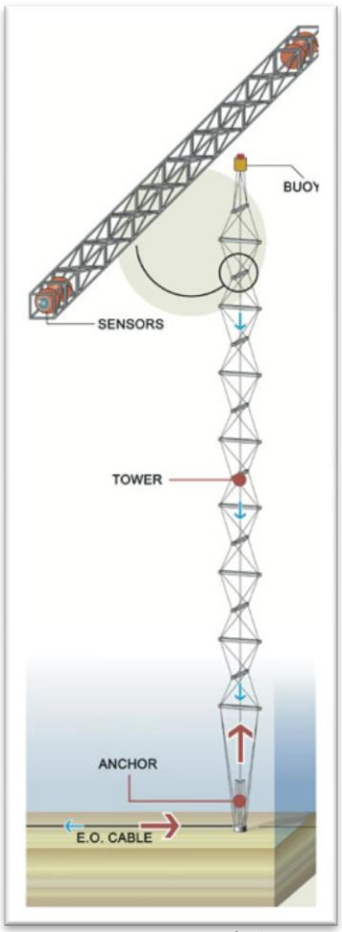


Fig 2

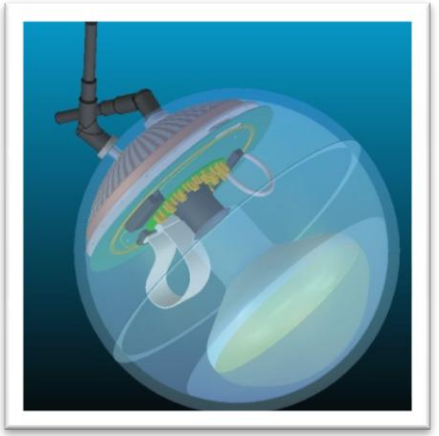


Fig 3a

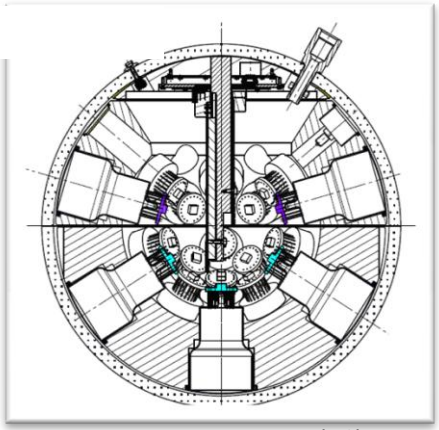
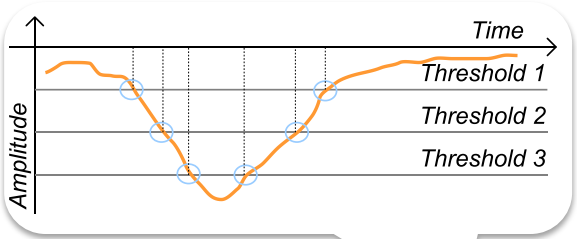


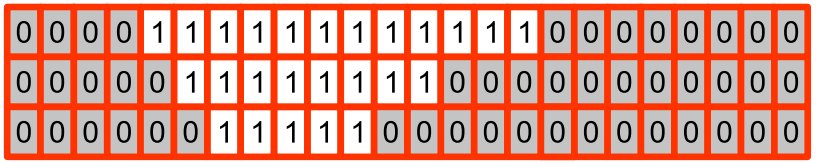
Fig 3b

Constrains of the Design

DAC 10b

irfu cea saclay

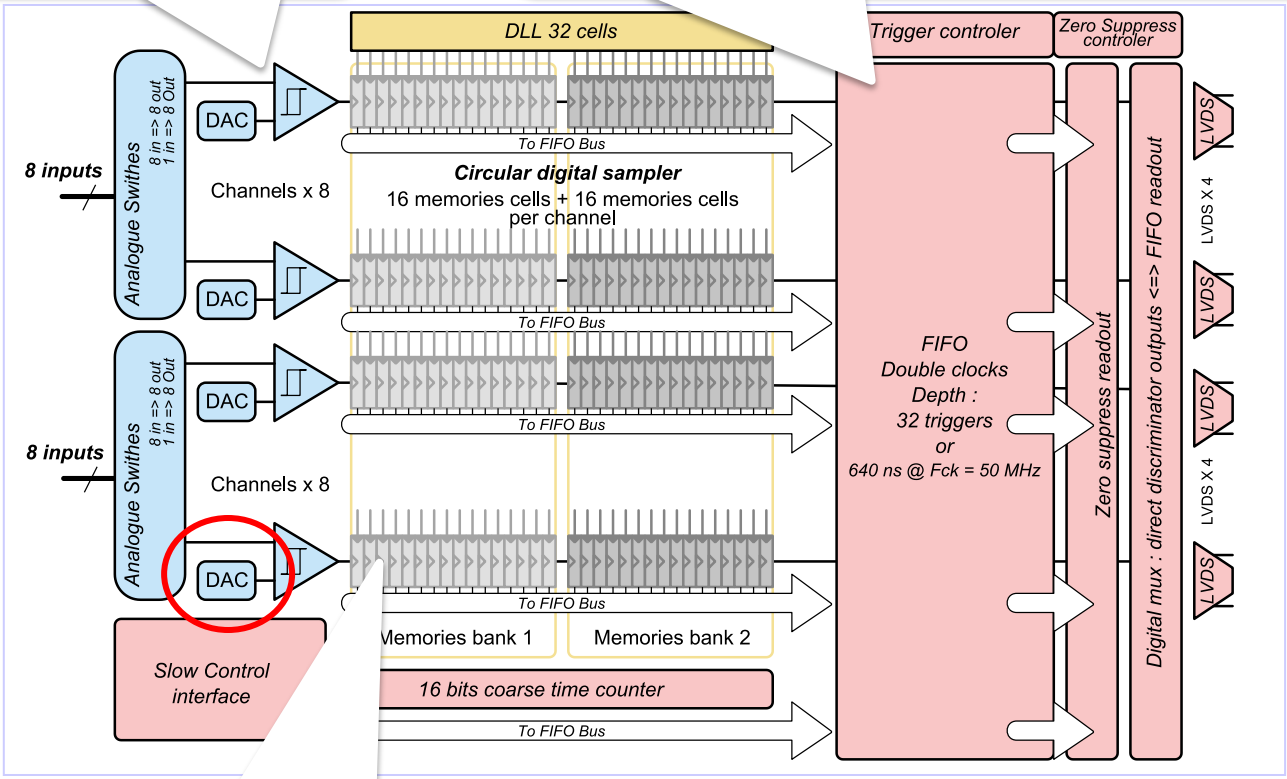


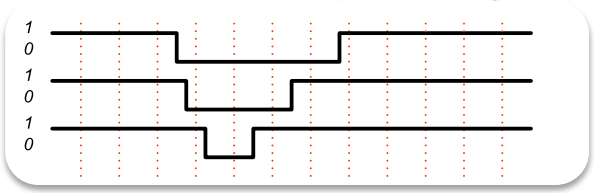


❖ DAC

- ⊙ 10 bits (~1.5mV)
- ⊙ Static
- ⊙ Linear
- ⊙ Fit in channel width
- ⊙ Min-Max (V) = [0.9:2.4]
- ⊙ 1 calibration for the 16 DACs

Choice : resistors ladder



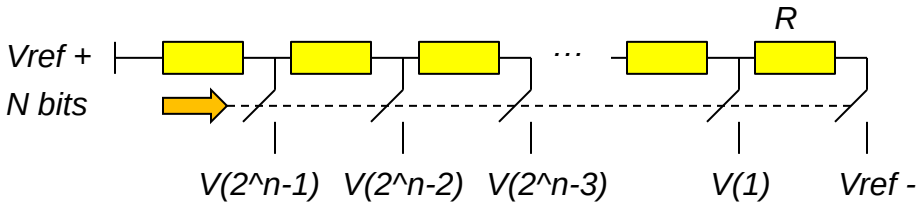


❖ Scott (AMS S35D4)

- ⊙ Scott 0 (11/08) ➔ Validated &Tested - No FIFO
- ⊙ Scott 1 (09/09) ➔ To be tested

irfu cea saclay

❖ Conventional DAC resistors ladder



⊙ 10 bits ➔ 1024 resistors ➔ need to be reduced

⊙ $$DNL(\%) \approx \sigma\left(\frac{\Delta R}{R}\right) = \frac{A\_R}{\sqrt{W \cdot L}}$$

W : resistor width
L : resistor length
A_R : technology dependant

Gaussian variation of R

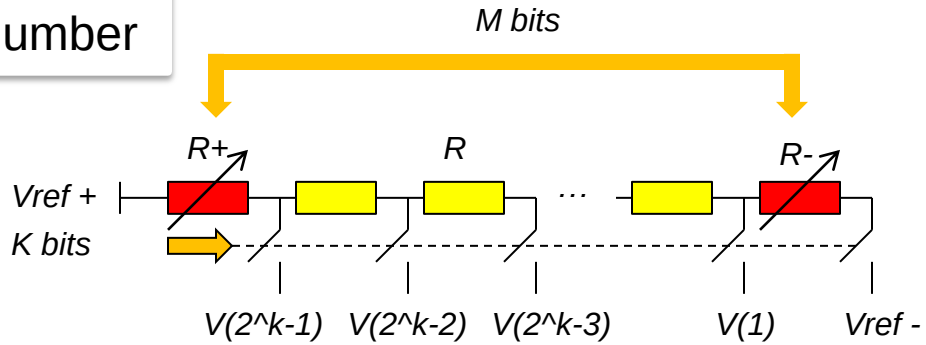
⊙ $$INL_{\max}(mV) = \frac{1}{2} \cdot \frac{Vref_{+} - Vref_{-}}{\sqrt{Nb}} \cdot \sigma\left(\frac{\Delta R}{R}\right)$$

Nb : Number of resistors [1]

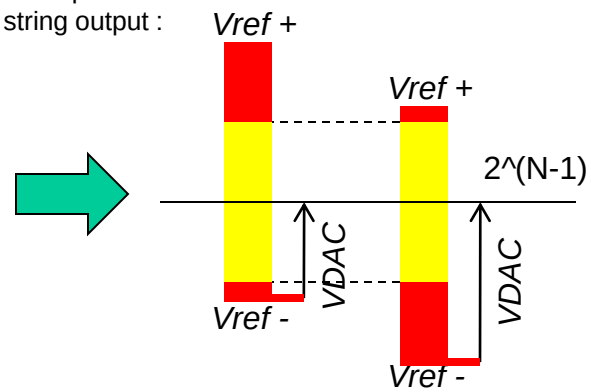
❖ Multi LSB resistor string DAC

K+M = N bits
*(R+) + (R-) = R ➔ Rtot = 2^k*R*

① Reduction of resistors number



Example of LSB shift for a constant coarse resistor string output :



[1] "A 10-bit Folded Multi-LSB Decided Resistor String Digital to Analog Converter, Chun-Chieh Chen & Al, ISPACS 2006"

Optimization vs Size

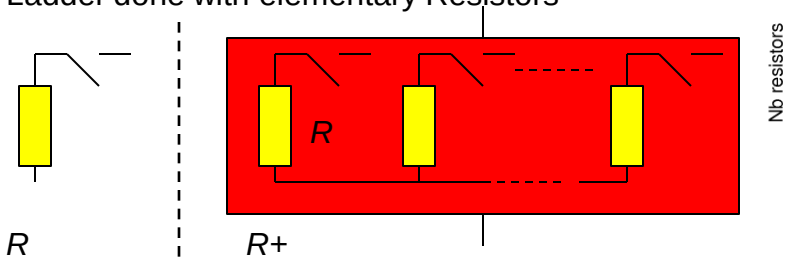
DAC 10b

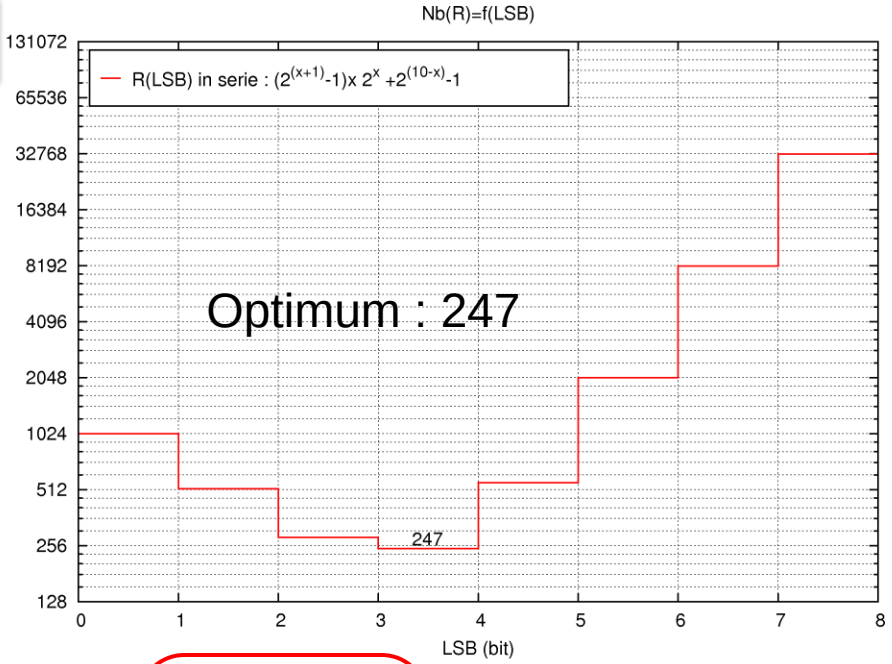
irfu cea saclay

① Reduction of resistors number Q

$$Q = (2^K - 1) + (2^{M+1} - 1) \cdot 2^M$$

Ladder done with elementary Resistors





② DNL

Resistor	R poly 2	R poly H	R poly B	(mc file)
σ (%)	9.5	6.5	3	8.6
Ω /□	50	1.2k	240	

Specificity AMS S35

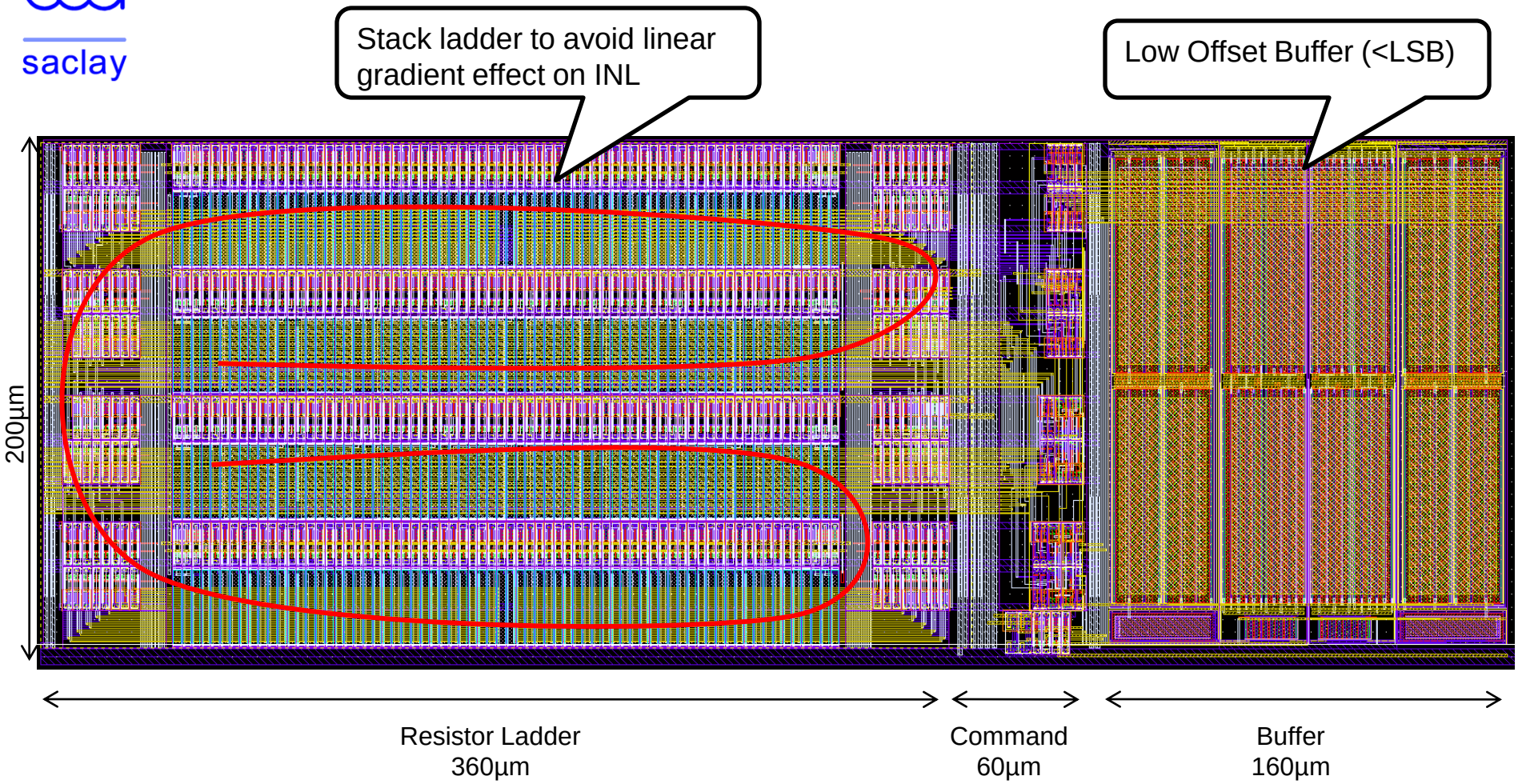
② INL

⊙ Decrease of the number of serried resistors ➔ INLmax < 0.5 LSB ➔ σ(ΔR/R)< 0.3%
➔ W*L > 90

Parameters & Layout

DAC 10b

- Unit resistor size : 30x3µm² ➔ 2400 Ω
- Total resistor 30kΩ ➔ 110µA @ 3.3V dynamic range, 50µA @ 1.5V
- Area : 200x420µm²



Without slow control registers

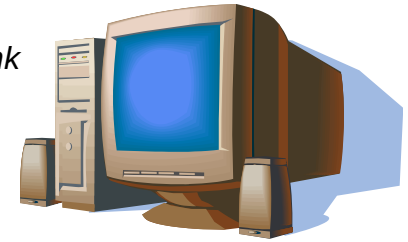
Test Bench

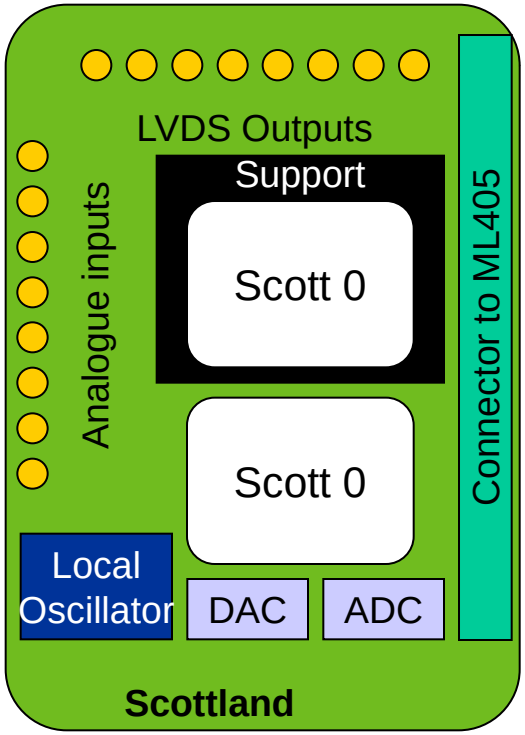
DAC 10b

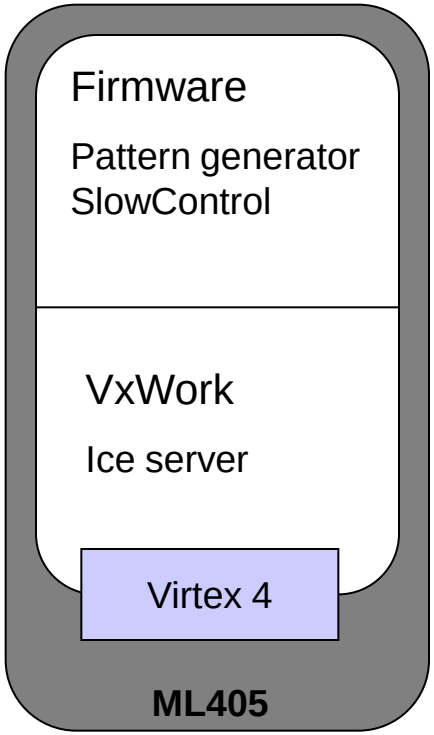
irfu cea saclay

Direct connection

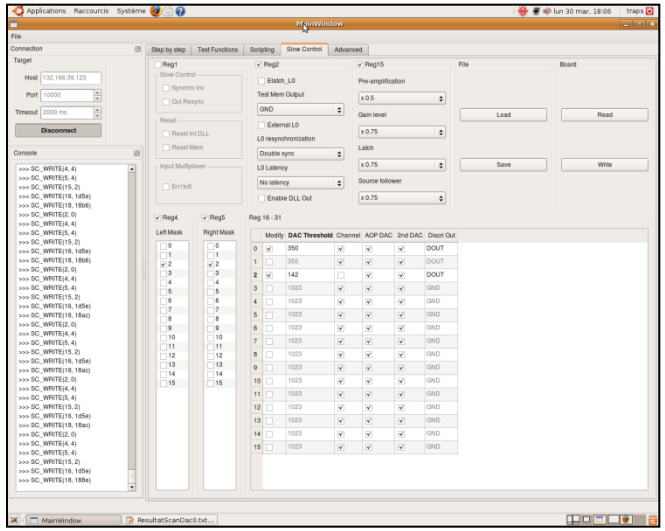
Pattern generator → Scott 0 ⇔ Virtex 4 ⇔ *Ethernet link*







GUI & Ice Client

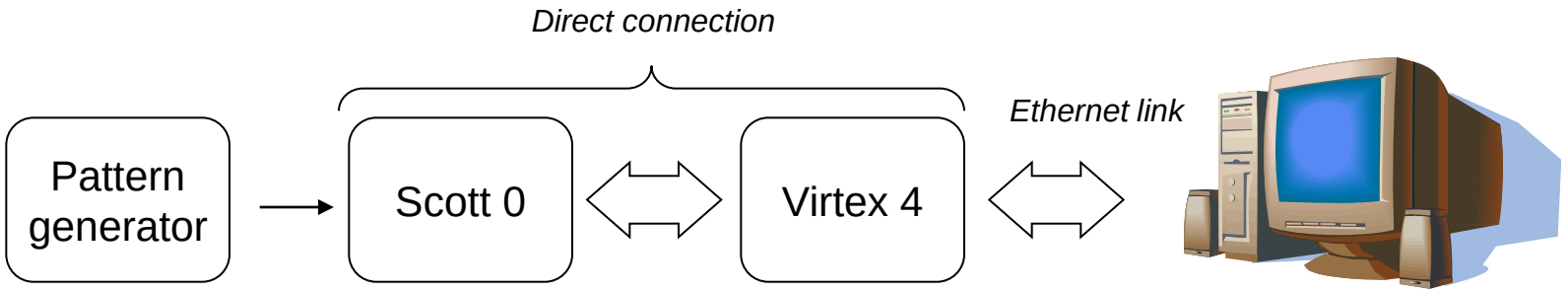


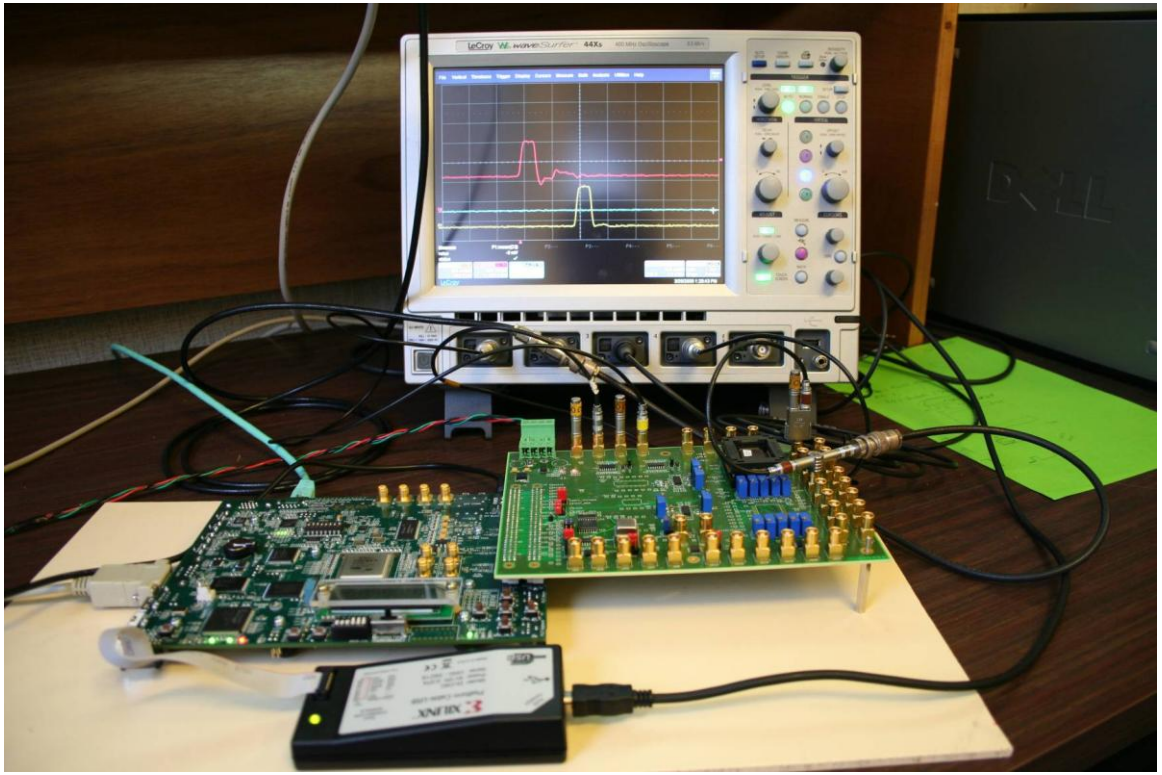
PC

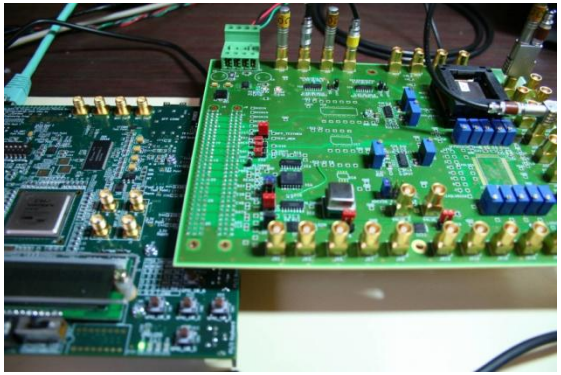
Test Bench

DAC 10b

irfu cea saclay

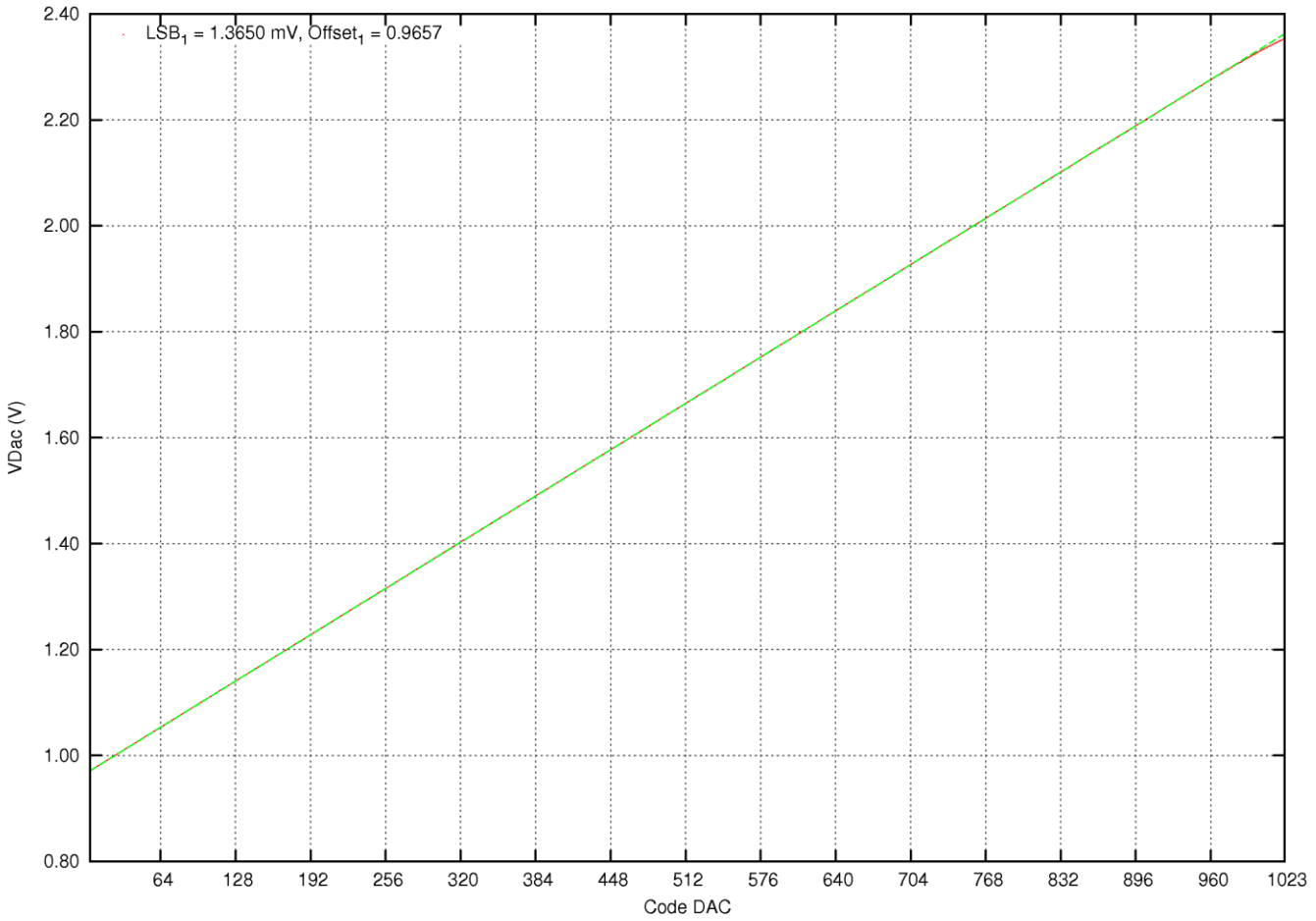






irfu cea saclay

❖ Single DAC Linearity ASIC 3

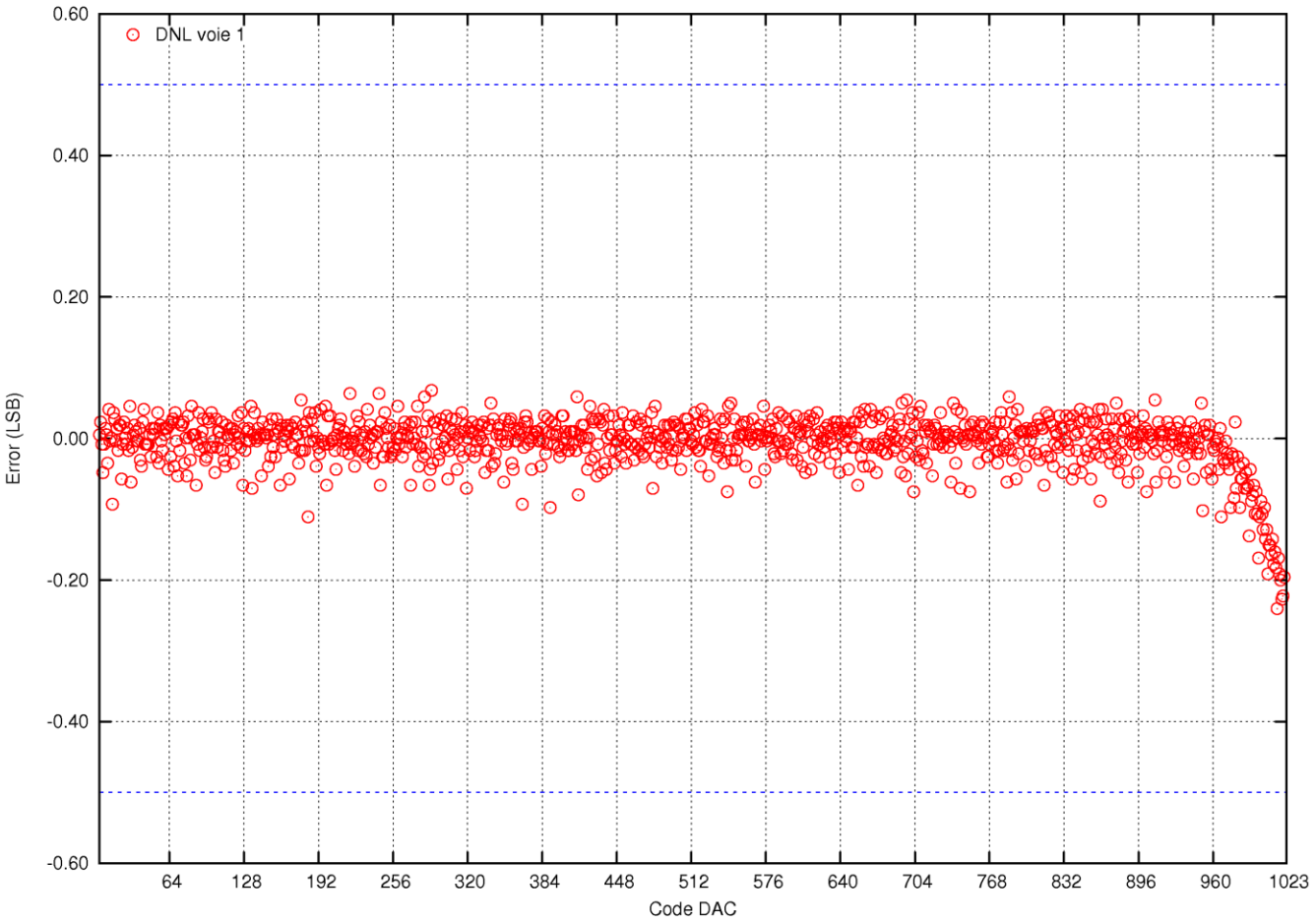


⊙ Dynamic Range : [Vref+:Vref-] ± 500µV (voltage drop in access resistors)

irfu cea saclay

❖ Single DAC DNL

ASIC 3

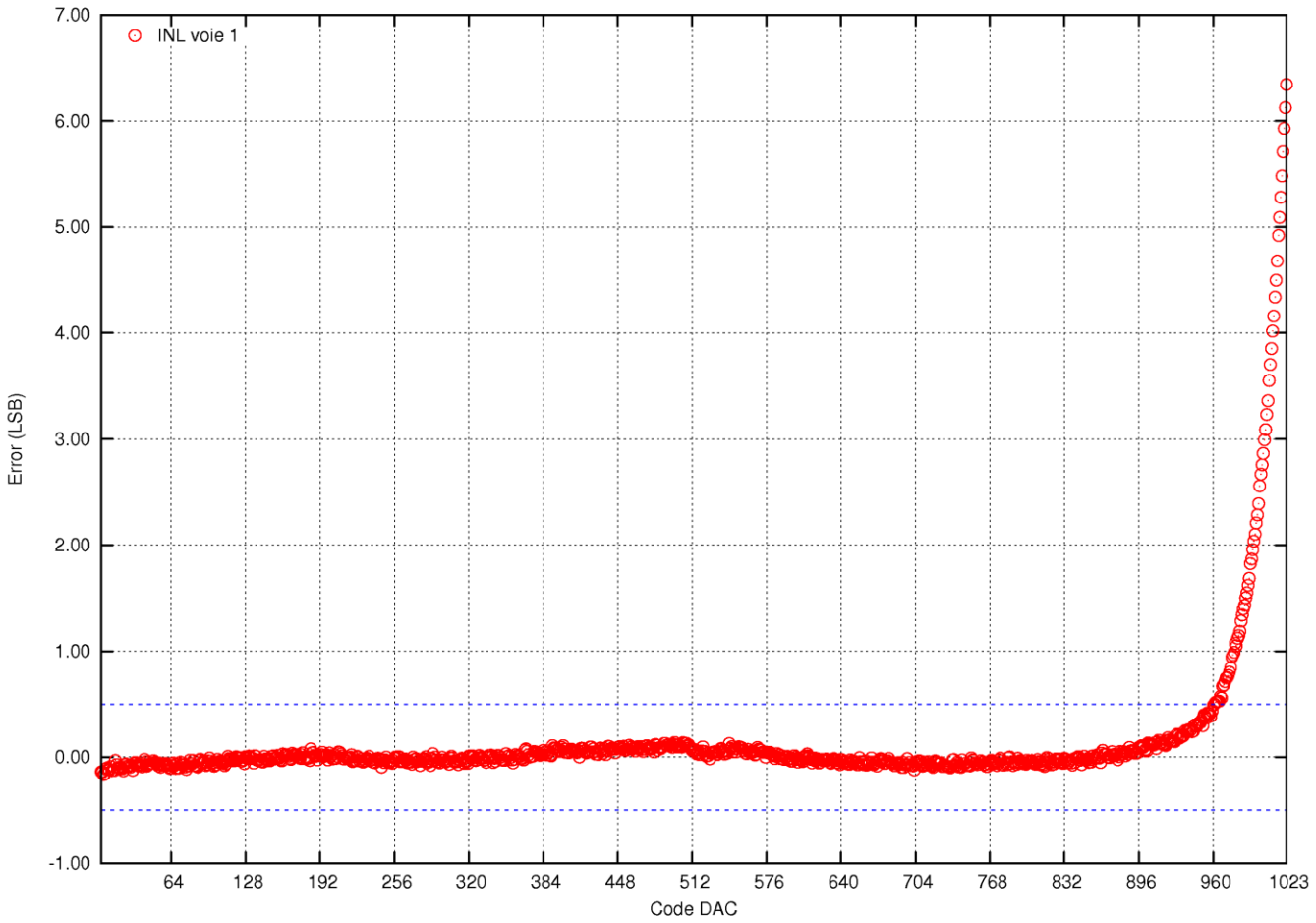


- | DNL | << 0.5 LSB
- σ(ΔR/R) ~ 2.6% (≠ 0.3% expected BUT 2.6% ~ 35µV ➔ limit of acquisition board)

irfu cea saclay

❖ Single DAC INL

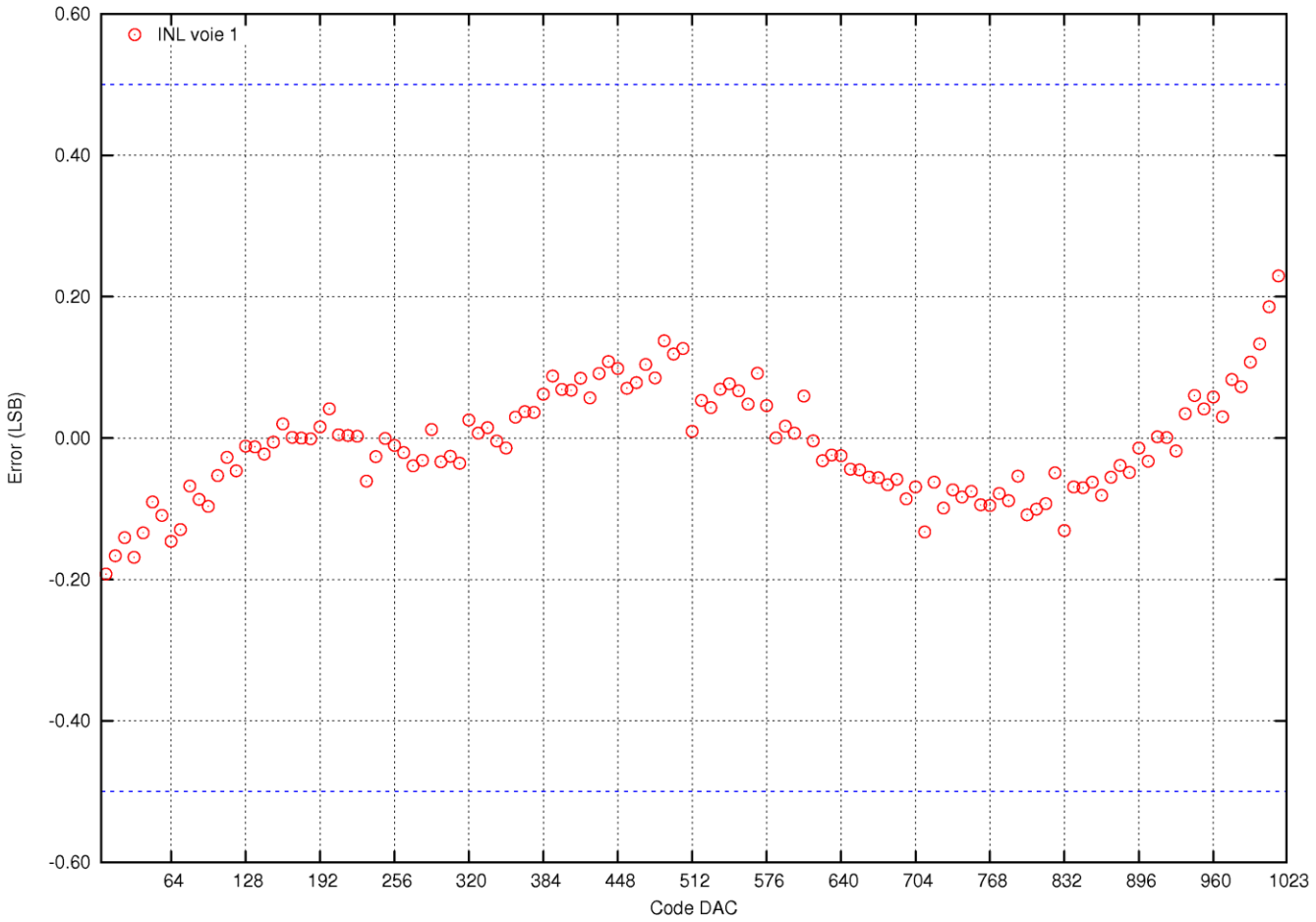
ASIC 3



- From 0 to 960 : | INL | < 0.5 LSB
- After 960 : monotonic shift from the straight line

irfu cea saclay

❖ **Single DAC INL** **Gain 0.5** **ASIC 3**



⊙ | INL | << 0.5 LSB with lower output buffer gain

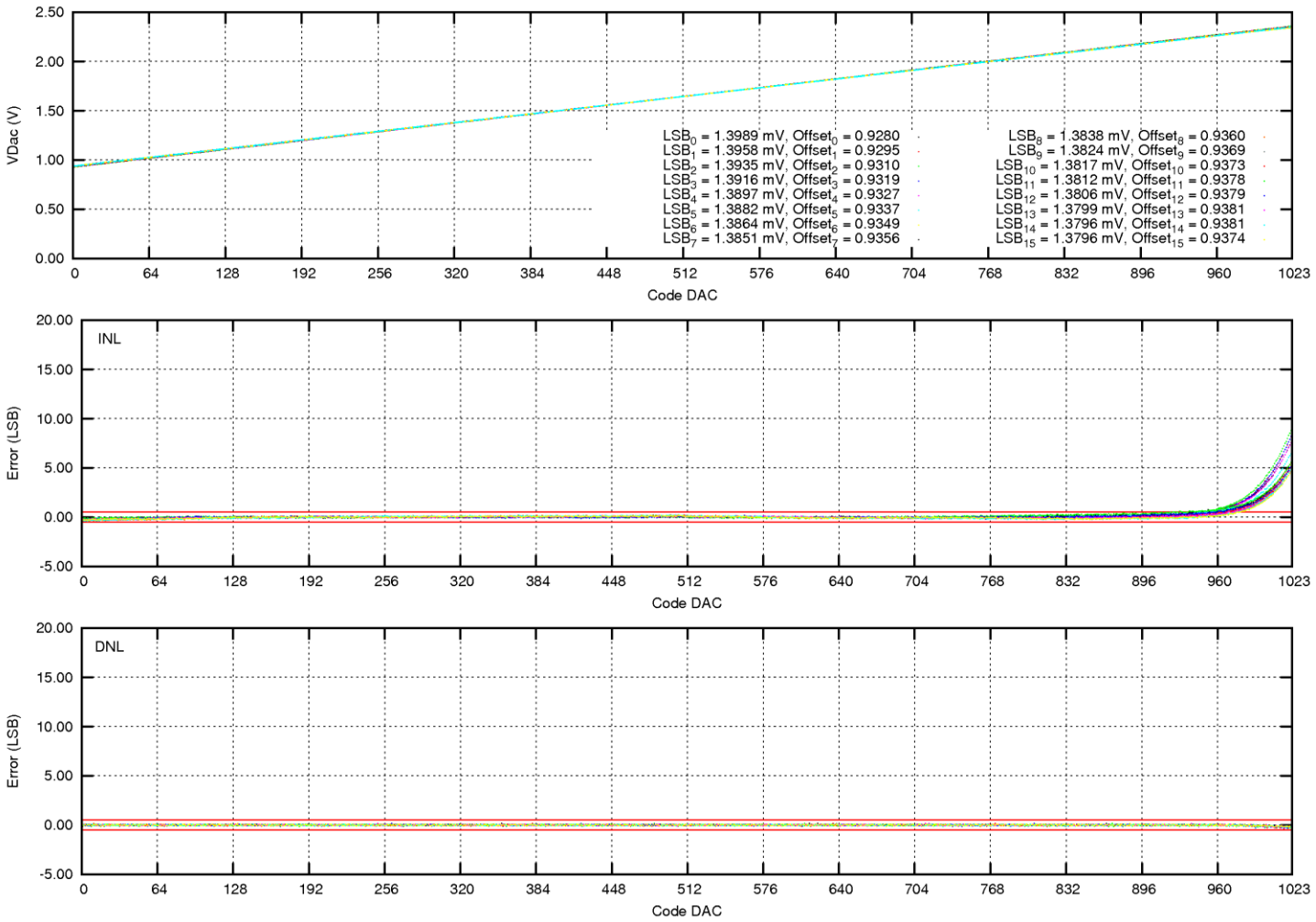
⊙ Mean(INLmax) = 163µV ➔ σ(ΔR/R) ~ 0.4% ➔ A_R = 3% ! 1 point for the datasheet

Results

DAC 10b

irfu saclay

❖ **16 DACs : 1 fit / DAC** **ASIC 4**



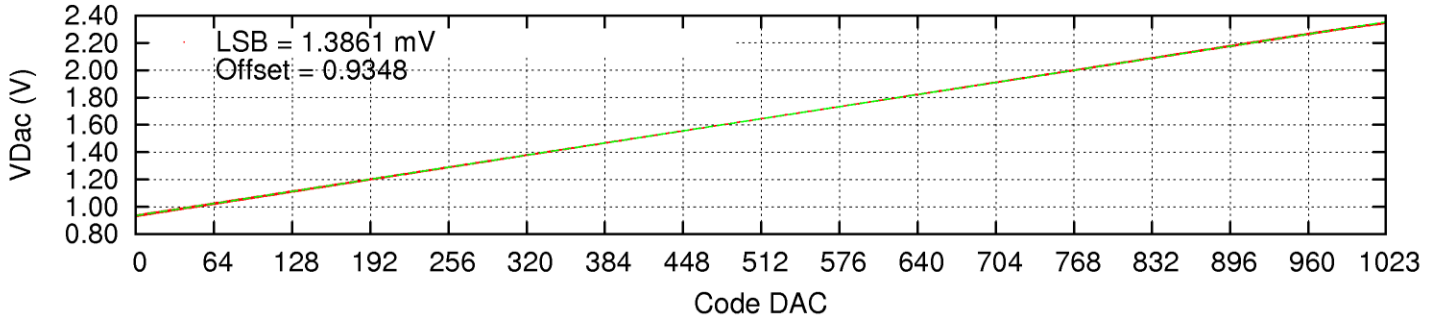
⊙ 10 bits for 16 DACs

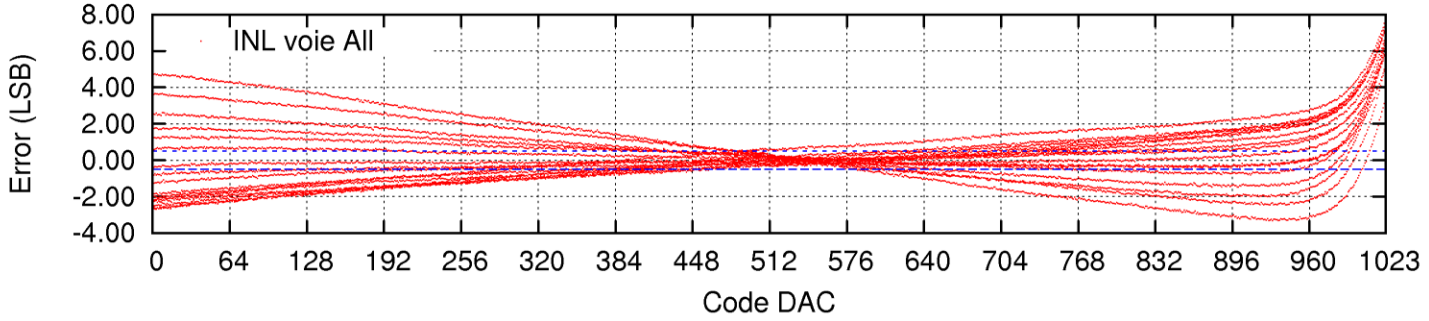
Results

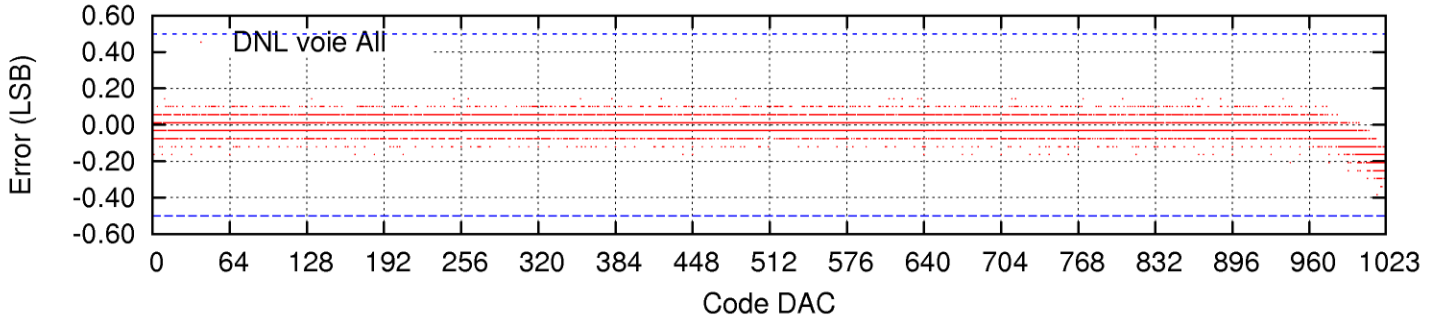
DAC 10b

irfu cea saclay

❖ **16 DACs : 1 fit for 16 DACs** **ASIC 4**





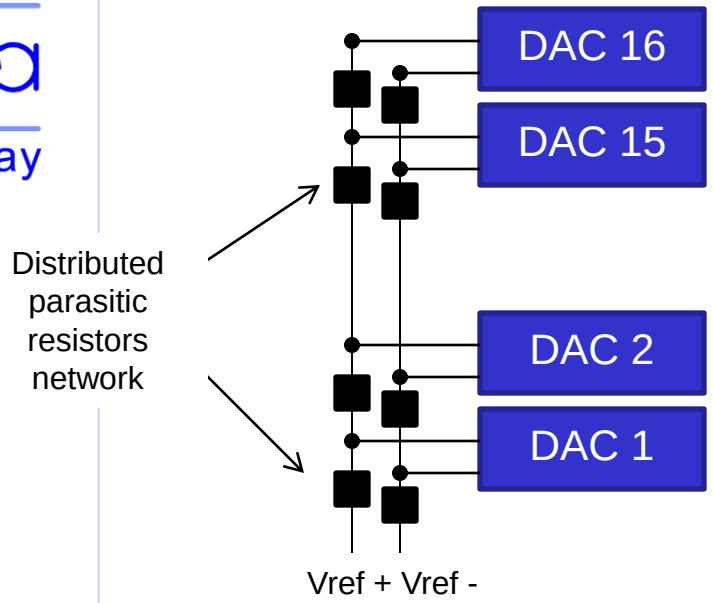


⊙ Rotation center of INL curves ➔ Code 512

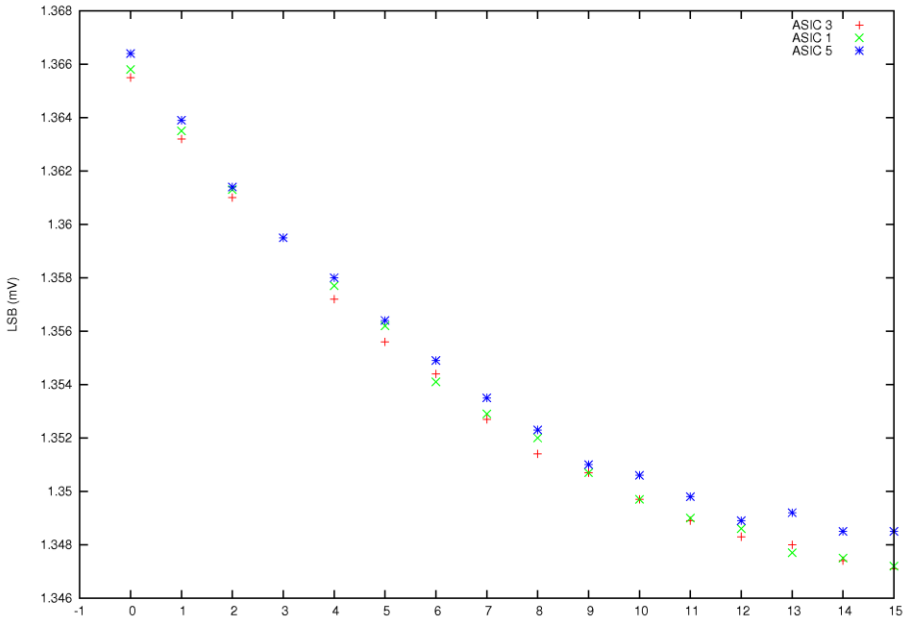
Results

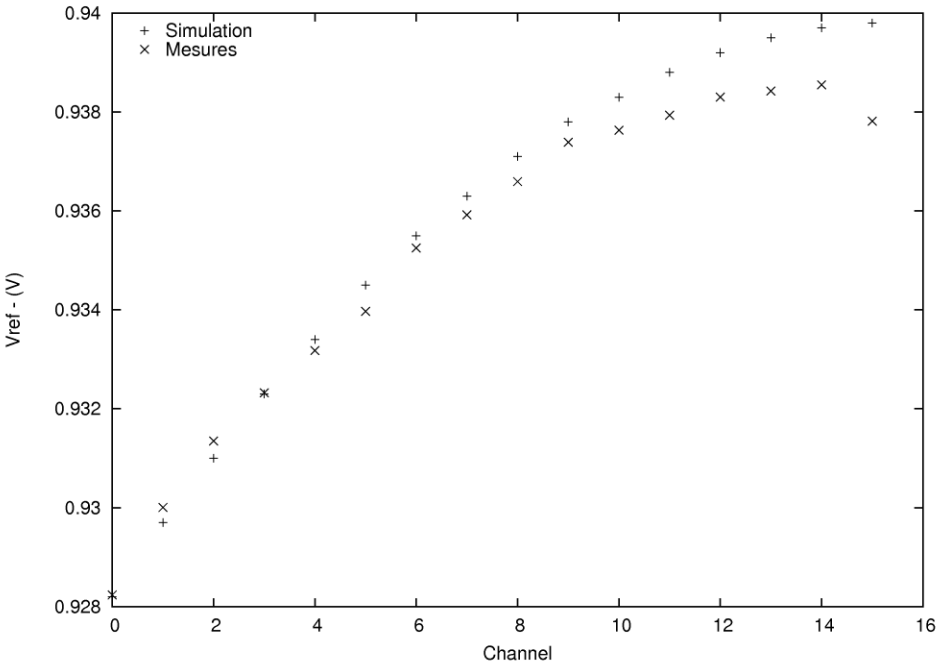
DAC 10b

- **16 DACs**



- Parasitic resistors network on references
- Behavior constant on different ships
- Easily checked in simulation





Conclusions

irfu
cea
saclay

- **Actual DAC**
  - 100% DAC tested are 10 bits !
    - | DNL | < 0.5 LSB
    - | INL | < 0.5 LSB if output buffer current supply is set to 0.5
  - No common calibration (even if the 'error' seems repeatable for 3 ASIC)
    - Error understood and corrected in Scott 1

- **Possible upgrade**
  - Optimize the size of the layout :
    - Change the digital vs analog command circuit ratio
  - Change to a differential mode
    - Solve the constrains supply by the INL

Thank You

irfu cea saclay

❖ Scott ASIC

Analogue Signal → Front End Asic → Digital data → System on Chip → Ethernet TCP/IP data link → Shore

16 channels

Circular memory

Sampling memory 1
16 digital cells (~ 20ns)

Sampling memory 2
16 digital cells (~ 20ns)

Input k

DAC k

Discriminator k digital output

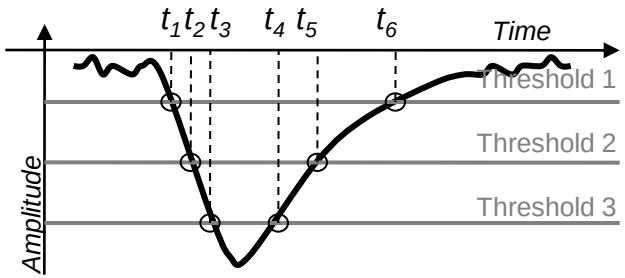
0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0 → 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Writing

Reading

Zero supress
No dead time

Digital Fifo + Zeros suppress



❖ DAC main constrains

- ⊙ 10 bits
- ⊙ Static + linear
- ⊙ Less calibration as possible

Choice of DAC : resistor string