

Outils de CAO

Ecole de microélectronique IN2P3

12 -15 octobre 2009, La Londe Les Maures

Mission: Doter les électroniciens de l'IN2P3 des outils de conception permettant de mener la Recherche, Développement et Fabrication nécessaire aux expériences

↩ **Développements cohérents**

- Pas de rupture entre les étapes de conception
 - ↳ Un Système Intégré
 - ↳ Des bibliothèques communes (PCB), IP

↩ **Environnement standard**

- Synergie entre laboratoires, IN2P3, Internationaux

↩ **Maintenir le potentiel des électroniciens**

- Technicité

↩ **Négocier les marchés**

- Visibilité de l'Institut
- Interlocuteur unique vis-à-vis des fournisseurs

Organisation de la Mission

- **Centre mainteneur (LAL)**
 - ↳ **Gestion licences CC-IN2P3**
 - ↳ **Serveur Web**
 - <http://www.in2p3.fr/actions/electronique/organisation.htm>

- **Top to bottom**
 - ↳ **Chefs de Service**
 - ↳ **Correspondants CAO**
 - ↳ **Correspondants Formation**

- **Bottom Up**
 - ↳ **Sites experts → Contact avec hot line fournisseurs**
 - ↳ **ASIC: IPHC + LAL**
 - **Virtuoso → Isabelle, Grégory, Frédéric, Nicolas, Claude + Gisèle**
 - **SOC → Abdelakder, Guy + Frédéric**

- **Broadcast → Liste de diffusion: Il faut s'inscrire!**
 - ↳ Liste CADENCE IAO-L (simulations, synthèses numériques)
 - ↳ Liste CADENCE MGR-L (installations, management logiciels)
 - ↳ Liste CADENCE MGR_IN2P3-L (licences)
 - ↳ Liste CADENCE PCB-L (flot "SPB" Concept-Allegro)
 - ↳ Liste CADENCE VLSI-L (flots CIC et outils associés)
 - ↳ Liste CADENCE FORUM-L

■ Marché signé en 2008

- ↪ **ARTICLE 1 - OBJET DU MARCHÉ**
.....L'IN2P3 a vocation de recherche fondamentale en physique nucléaire et en physique des particules.

Les prestations qui font partie de ce marché sont réservées à ce contexte de recherche fondamentale à l'exclusion de tout autre, en particulier à l'exclusion de prestations de service et de contrats industriels lucratifs.

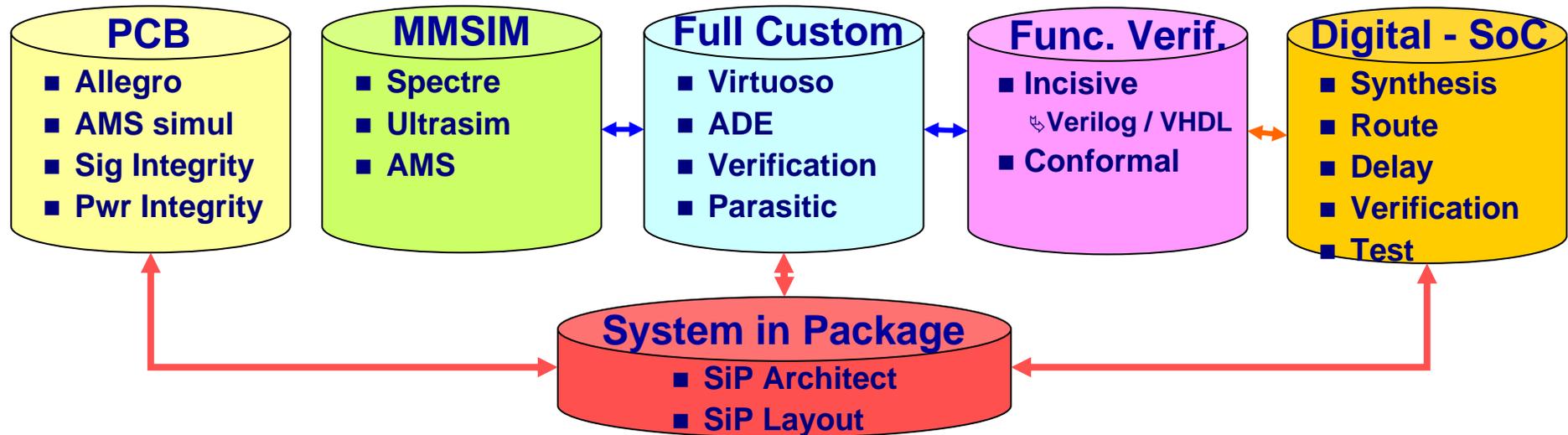
- ↪ **Sensibilisez vos services de valo → MIND**

■ Remarque sur accès Europractice (conf Flot IBM)

- ↪ Justifier d'actions académiques (cours, stagiaires, doctorants)
- ↪ Les fournisseurs sont attentifs



■ Portefeuille du marché



■ Des licences centralisées au CCIN2P3

- ↳ Mutualisées → accès aux versions haut de gamme
- ↳ Pour les nouveaux flots (Virtuoso 6.0, Soc, MMSIM)
- ↳ Compatibles avec les utilisations courantes (V5.xx, Ambient)

■ 2009 a vu le démarrage de Virtuoso 6.x à l'IN2P3

- ↳ Stage spécifique 4 jours à Clermont, 11 IN2P3 + 2 CEA



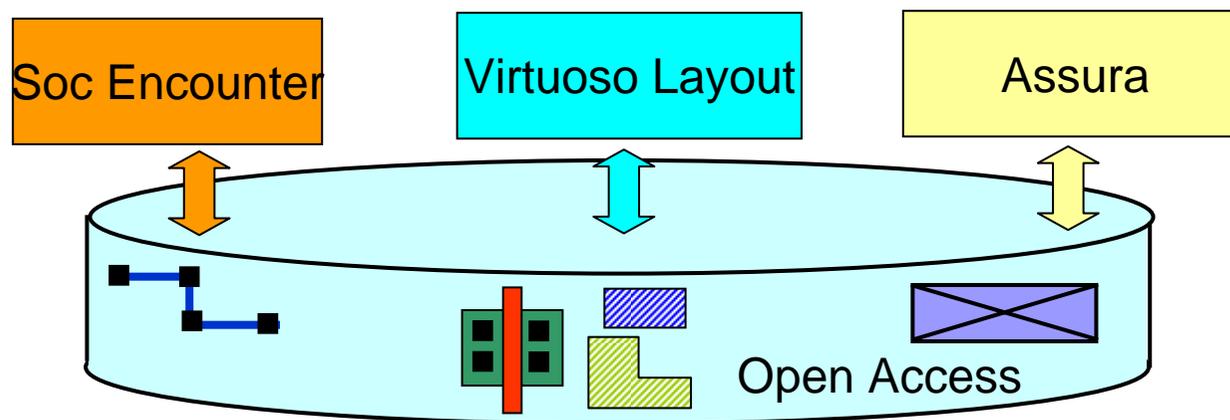
Cadence DFII 6.1xx

■ Utilisation d'openAccess (oa)

↪ Interopérabilité des outils

➢ Layout et vérification principalement

Migration pour
archivage des
designs "Gold" ?



■ Peu de changements apparents au niveau du file system

↪ Library → Cell → Cell Views → sch/layout.oa (.cdb)

↪ Properties Prop.xx → data.dm

↪ Master.tag ✓

↪ Lib.defs, cds.lib ✓ → Warning → Library Path Editor

■ L'interopérabilité implique

↩ Une techfile commune pour Virtuoso et SoC

↩ Redéfinition et création d'objets layouts

➤ Wires → Multilayer + Wire editor

➤ Path segment → Single layer

➤ Boundaries

☞ prBoundary → délimite la surface d'un bloc/circuit

☞ clusterBoundary → identifie un groupe de cellules

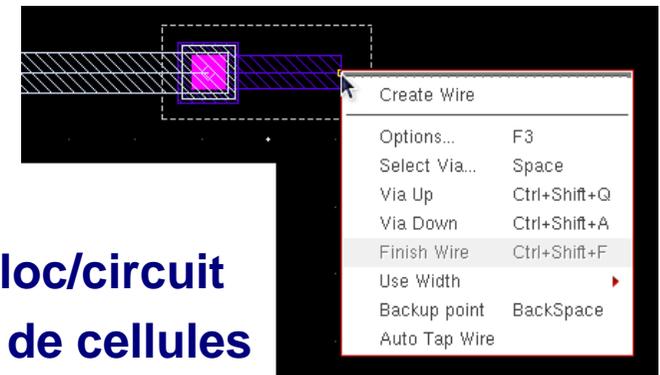
☞ areaBoundary → assigne des éléments à une zone spécifique (High Voltage)

➤ Blockages, interdictions au

☞ Placement

☞ Routage

☞ Pins ...



OpenAccess

■ L'interopérabilité implique

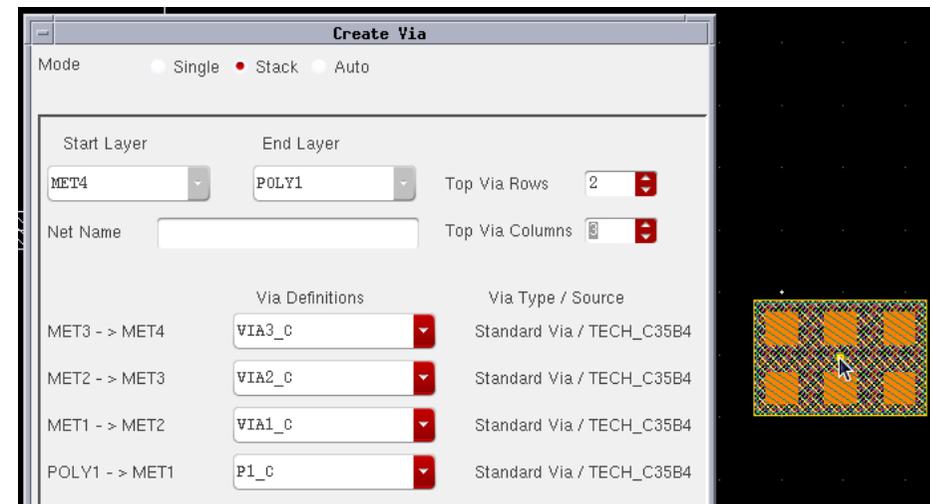
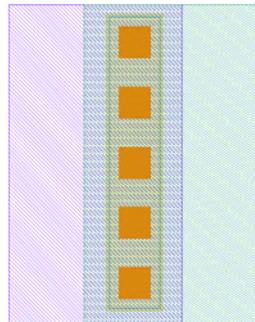
↩ Redéfinition et création d'objets layouts

➤ Marker

- ☞ Représentation unifiée
- ☞ Sauvé dans la base de données
- ☞ Gradué selon la sévérité → Fatal, Warning

➤ Via

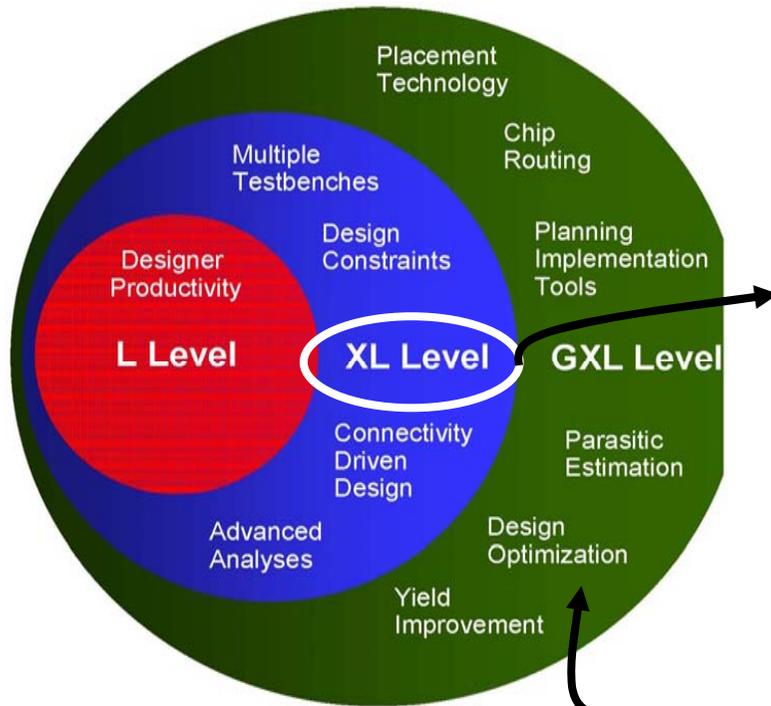
- ☞ Plus de symbolic Via
- ☞ Stacked Vias
- ☞ Auto Vias



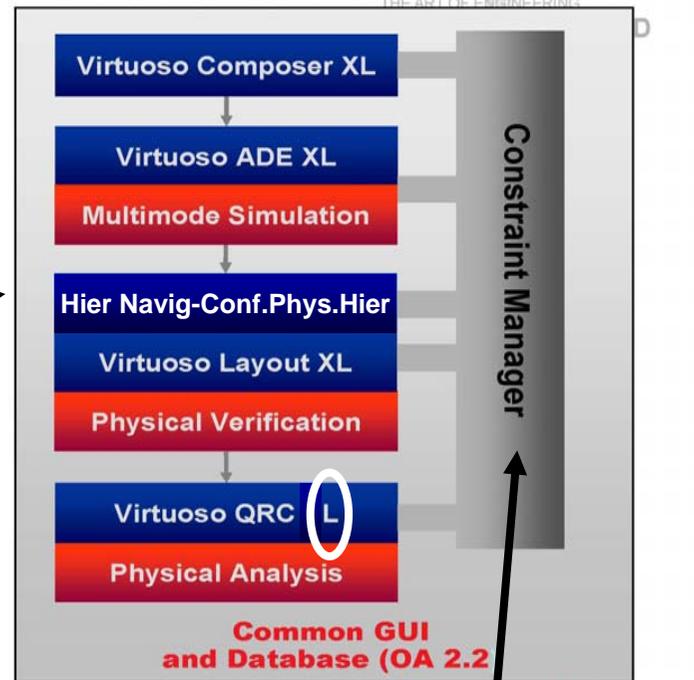
Environnement de travail IN2P3

Offre Cadence

XL: config. 6.x de base des labos Config. 5.1



5 licences GXL



Propagations des contraintes



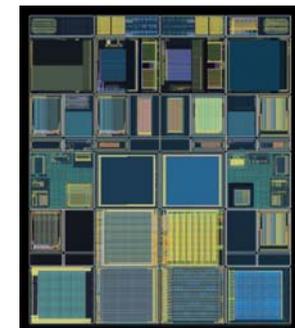
■ Gros designs, réticule MPW

↪ mode 64bits

- Layout, Layoutplus(32), Assura, Calibre (M-G)
- Certaines fonctionnalités n'existent qu'en 32 bits → SpectreVerilog

■ Accélération simulation, vérification

↪ Mode multi-processeur (WS Linux biprocessor / quad cores)



3DIC Reticule 8 GB

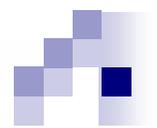
Schematic XL

- Un ensemble d'assistants – Des workspaces configurés
- Onglet/schéma

The screenshot shows the Cadence Schematic XL editor interface. The main workspace displays a complex circuit schematic with components like resistors, capacitors, and transistors. Several panels and toolbars are highlighted with blue arrows and labels:

- Navigator:** Located on the left side, showing a hierarchical tree of components.
- Property Editor:** Located below the Navigator, displaying properties for the selected component.
- Viewer:** Located at the bottom left, showing a world view of the schematic.
- Assistants:** A menu at the top center, with several items circled in red, including Navigator, Property Editor, World View, Search, Constraint Manager, Circuit Prospector, and Annotation Browser.
- Show/Hide assistants:** A button at the top right, also circled in red.
- Search:** A search bar on the right side of the interface.
- Constraint Manager:** A panel on the right side, used for managing design constraints.

At the bottom left, the text "claude.colle" is visible. At the bottom center, the text "mouse L: schSingleSelectP1()" and "M: schZoomFit(1.0 0.9)" are visible. At the bottom right, the text "R: schHIMousePopUp()" and "Cmd: Set: 1" are visible.



Constraints Assistant

- Propage et impose clairement les intentions du concepteur
 - ↪ A l'équipe de design (FE / BE)
 - ↪ A travers le flot

Annotation txt formalisée en contrainte

Constraint Manager

Type (2) Parameters

preamplifier1... constraint

- Alignment ... top
 - M5 top
 - M6 top
- Current (2) 2m
 - M1:S
 - M0:D

Constraint (2) Constraint Pa

Name	(various)
Owner	CLD.preampli...
Axis	horizontal (de...
Enabled	true
Status	none
Notes	
PreserveOr...	false
pitch	(not set)
DC Value	0.002

R: schHiMousePopUp()
Cmd: Sel: 0

Constraints Assistant

■ Propagation vers le layout (XL)

The screenshot displays the Virtuoso Layout Suite XL Editing interface for a layout named 'CLD preamplifier1_optin_v2 layout'. The main workspace shows a schematic diagram with several components highlighted in yellow and green, indicating active constraints. The Navigator panel on the left lists various components, including nets (M7, M8, M9), vias (V_M1, V_M6, V_M11, V_M613), and metal layers (MET1, MET2, MET3, MET4). The Property Editor shows details for a selected instance (IM3).

Two Constraint Manager windows are shown. The top window displays a list of constraints:

Type (2 of 2)	Parameters
Alignment	top
IM5	top
IM6	top
Current (2)	2m

The bottom window shows a detailed view of a constraint:

Name	Value
Name	(various)
Owner	CLD.prea...
Axis	horizonta...
Enabled	true
Status	none
Notes	
Side	top
PreserveOr...	false
pitch	(not set)
use	boundary
layerName	TRENCH



■ Un ensemble de contraintes

↪ Sur les transistors, les pins, les nets

↪ De divers types

➤ Transistors

- ☞ Symétrie
- ☞ Matching de paires
- ☞ Ratio
- ☞ Alignement

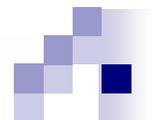
➤ Net

- ☞ Blindage
- ☞ Espacement

■ Fonction “Prospector”

↪ Recherche dans la hiérarchie du schéma l'existence de structures prédéfinies qui devraient se voir assigner des contraintes

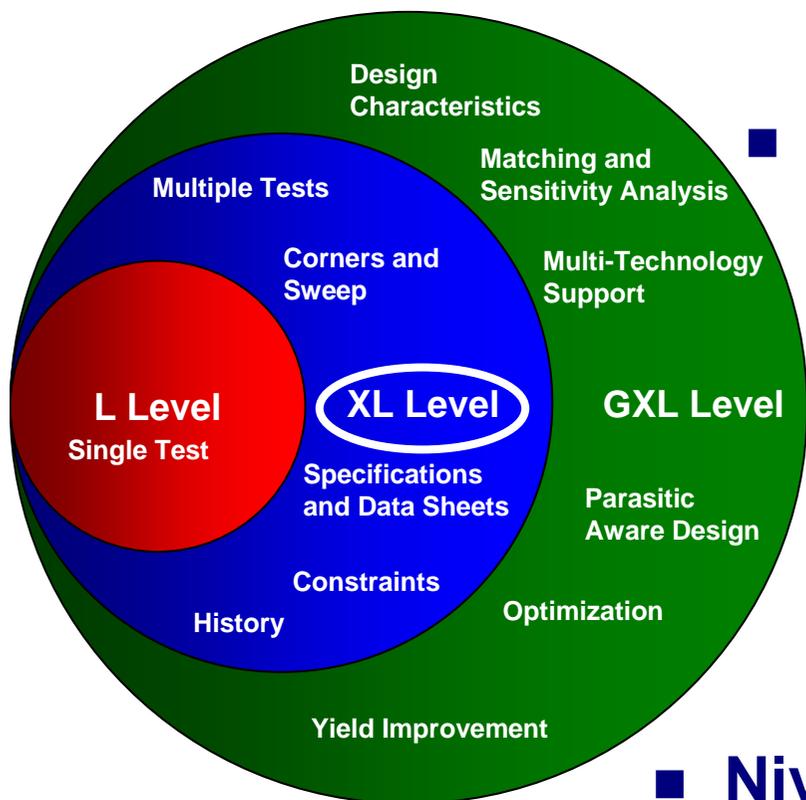
- Tous les miroirs de courant → Ratio
- Toutes les paires diff → Matching



ADE L / XL GXL

■ Niveau L Environnement classique

- DC, Transient, AC, Sweep, Corners, Monte Carlo



■ Niveau XL

↳ Nouvel environnement de simulation

➤ Cockpit sophistiqué pour

- ☞ une vision synthétique
- ☞ Une sauvegarde documentée des simulations
- ☞ Cellview spécifique *adexl*

↳ Sweep, Corners, Monte Carlo

■ Niveau GXL

- Rappel, les jetons GXL sont décomposables en session XL

GXL Feature	Token
Cockpit	2
Characterzation / modelling	1
Matching & Sensitivity Analysis	1
Parasitic Aware design	1
Multi-Technology Support	2
Otpimization (ex NeoCircuit)	6
Yield Improvement	10

ADE XL - Nouvelles interfaces et vue adexl

Create Tools Options Run Parasitics

Create Tools Options

- Test... → **Select Simulator**
- Corner... → **Single Test**
 - DC, Trans, AC
- Document... → **Document XML**
- Setup State...
- Datasheet...
- Spec Summary...

Tests Multiples

Corner Setup

Corner Name: C0

Variable / Parameters	Nominal	C0	C1	C2
Temperature		23	27	50
Design Variables				
vdd	2.3	2.4	2.5	
Parameters				
Model Files				
spectreLib4.scs				
Model Group				
Tests				
myFirstTest				
mySecondTest				
Number of Corners				

Tools Options Run P

- Calculator...
- Results Browser...
- Job Monitor...
- DCM

Run Parasitics Window Help

- Single Run, Sweeps and Corners
- Monte Carlo Sampling...
- Global Optimization...
- Local Optimization...
- Improve Yield...
- Sensitivity Analysis
- Edit Reference Point
- Stop Simulation
- Stop All Jobs

Option GXL

- A explorer

Design Characterization & Modeling (GXL)

- Top-Down / Bottom-Up behavioral models
- Verilog-A[MS], VHDL-AMS, Verilog-D, Liberty

Data View Assistant

Tests

- AC_Test
- Simulator spectre
- Analyses
- dc t 1 10G 20 Logarithmic Po...
- ac
- Design Variables
- eiddq 4-0
- vdd 2-5
- vin_ac 1.25
- Trans_test
- Simulator spectre
- Analyses
- dc t 0 12u
- tran
- Design Variables
- eiddq 4-0
- vdd 2-5
- vin_ac 1.0
- Global Variables
- siddq 0
- vdd 2.5
- vin_ac 1.0
- Parameters
- Corners
- Documents
- Setup States

Run Summary

2 Tests

- 1 Point Sweep
- 0 Corner
- Nominal Corner

History Item	Status
Interactive.1	finished
Interactive.0	finished

Outputs Setup Results Diagnostics

adexl adc_cascode_opamp_sim adc_cascode_opamp_sim

Onglets

Test	Name	Type	Expression/Signal/File	Plot	Save	Spec	Weight
AC_Test		signal	/OUT_AC_3BIT				
Trans_t...		signal	/Vout2				
AC_Test	AC_Ga...	expr	value(mag(VF("/OUT...				
AC_Test	AC_B...	expr	bandwidth(mag(VF("...				
Trans_t...	AvgOut	expr	average(VT("/Vout2"))				

Results

Test	Output	Nominal	Spec	Weight	Pass/Fail
AC_Test	/OUT_AC_3BIT				
AC_Test	AC_Gain_1k	121.7			
AC_Test	AC_BW_3db	36.94M			
Trans_test	/Vout2				
Trans_test	AvgOut	1.575			

Diagnostics

Run: Interactive.1

Run Summary

Design Points	Points/Hour	Elapsed Time	Total Errors
1	450	0:00:08	0

Job Summary Test Summary

Test	Avg(s)	Current	Errors
AC_Test	0.52		0
Trans_test	0.46		0

Virtuoso layout

■ Fonctionnalités en forte augmentation

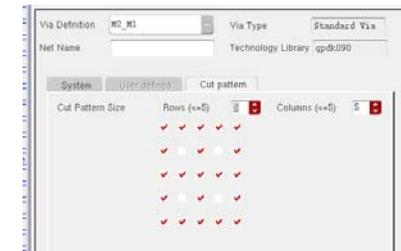
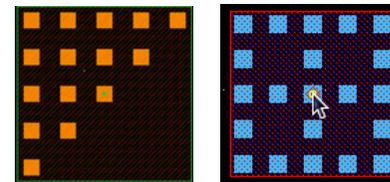
↪ Wires

- Changement de largeur sur segment
- Stretch avec environnement attaché



↪ Contacts / Vias

- Stacked
- Cut Arrays



↪ Toolbox

- A condition d'être supporté par le kit



↪ Dynamic Selection Assistant

- Aide à la navigation dans la hiérarchie



Virtuoso XL

■ Routage Assisté

- ↪ Netlist → Vérification en ligne allégée + On Demand
- ↪ Design rules → Vérification DRC en ligne
- ↪ Contraintes → Constraints manager, blocages

■ Configuration hiérarchique

- ↪ Hierarchy Browser équivalent
- ↪ Génère différentes implémentations physiques
 - Sans toucher au schéma
- ↪ Soft Blocks Mode
 - Pour floorplanning (GXL)

The screenshot shows the 'Configure Physical Hierarchy Editing' dialog box for the cell 'trans_id_bias_mux'. The dialog is divided into 'Logical' and 'Physical' sections. The 'Logical' section shows the library 'ether', cell 'trans_id_bias_mux', and view 'schematic'. The 'Physical' section shows the library 'ether', cell 'trans_id_bias_mux', and view 'layout'. Below these sections is a table of physical cells and their associated libraries and views. A blue box highlights the 'and2_1x_hv' cell in the table, and another blue box highlights the 'and2_1x_hv' cell in the table.

Name	Inherited View List	View To Use	Physical Librar...	Physical Cell	Physical View	Inherited Stop Lit
trans_id_bias_mux	physConfig schematic cm...					layout_test lay...
I11 (ether and2_1x_hv schematic)	physConfig schematic cm...		ether	and2_1x_hv	layout_test	layout_test lay...
I10	physConfig schematic cm...		ether	inv_4x_hv	layout	layout_test lay...
I9	physConfig schematic cm...		ether	nor2_1x_hv	layout	layout_test lay...
I8	physConfig schematic cm...		ether	nand2_1x_hv	layout	layout_test lay...
I7	physConfig schematic cm...		ether	and2_1x_hv	layout_test	layout_test lay...
I6	physConfig schematic cm...		ether	and2_1x_hv	layout	layout_test lay...
I5	physConfig schematic cm...		ether	inv_4x_hv	layout	layout_test lay...
I4	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I3	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I2	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I1	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I0	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I8	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I7	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I6	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I5	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I4	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I3	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I2	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I1	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
I0	physConfig schematic cm...		gpdK090	nmos2v	layout	layout_test lay...
C0	physConfig schematic cm...		gpdK090	nmoscap2v	layout	layout_test lay...

Attributes:

Generation	Parameters	Terminals
Ignore for generation	false	
Ignore for check	false	
Split infactored devices	true	
Remove device		

Floorplanning

- & Soft Blocks → Anticipation
 - ↩ Congestions, Contraintes (alim),
 - ↩ Contraintes sur pins poussées dans les blocks (Numériques)

Attributes

Boundary I/O Pins Obstructions

Rectangle

Width: 5.0000 Height: 10.0000

Area Calculation

Mk: Manual Avg. Area Per Gate: 10.0000 Use Estimator

Avg. Area Per Gate: 10.0000 Gate Count: 100

Net Name	Term Name	Term Type	Layer	Width	Height	Number	Criticality	Sig Type
1 A<0>	A<0>	input	Bondpad	1.0000	1.0000	1	0	signal
2 A<1>	A<1>	input	Bondpad	1.0000	1.0000	1	0	signal
3 A<2>	A<2>	input	Bondpad	1.0000	1.0000	1	0	signal
4 A<3>	A<3>	input	Bondpad	1.0000	1.0000	1	0	signal
5 Ctrl	Ctrl	input	Bondpad	1.0000	1.0000	1	0	signal
6 Y<0>	Y<0>	output	Bondpad	1.0000	1.0000	1	0	signal
7 Y<1>	Y<1>	output	Bondpad	1.0000	1.0000	1	0	signal

Save Soft Block

Virtuoso Schematic Editor XL Editing: ether CidTop schematic Cor

Launch File Edit View Create Check Options Migrate Window Help

Navigator

Show: Default

Name

(CidLvl1_1) Lvl1

(CidLvl2_1) (CidLvl2_1) Ctrl

Property Editor

mouse L: schSing

32(42) >

Virtuoso Layout Suite GXL Editing: ether CidTop layout

Launch File Edit View Create Verify Connectivity Options Tools Window Assura Place Help

cadence

Workspace: Basic

32 Select:1 Sel(N):0 Sel(I):2 Sel(O):0 X:28.2150 Y:31.0550 dX:-10.0450

Navigator

Show: Default

Name

(CidLvl1_2) [...]

(CidLvl2_1) [...]

(CidLvl2_1) [...]

(CidLvl2_1) [...]

(CidLvl1_1) [...]

Back0<0>

Back0<1>

Back0<2>

Back0<3>

Back0<4>

Back0<5>

Back0<6>

Back0<7>

Property Editor

1 objects selected. Show

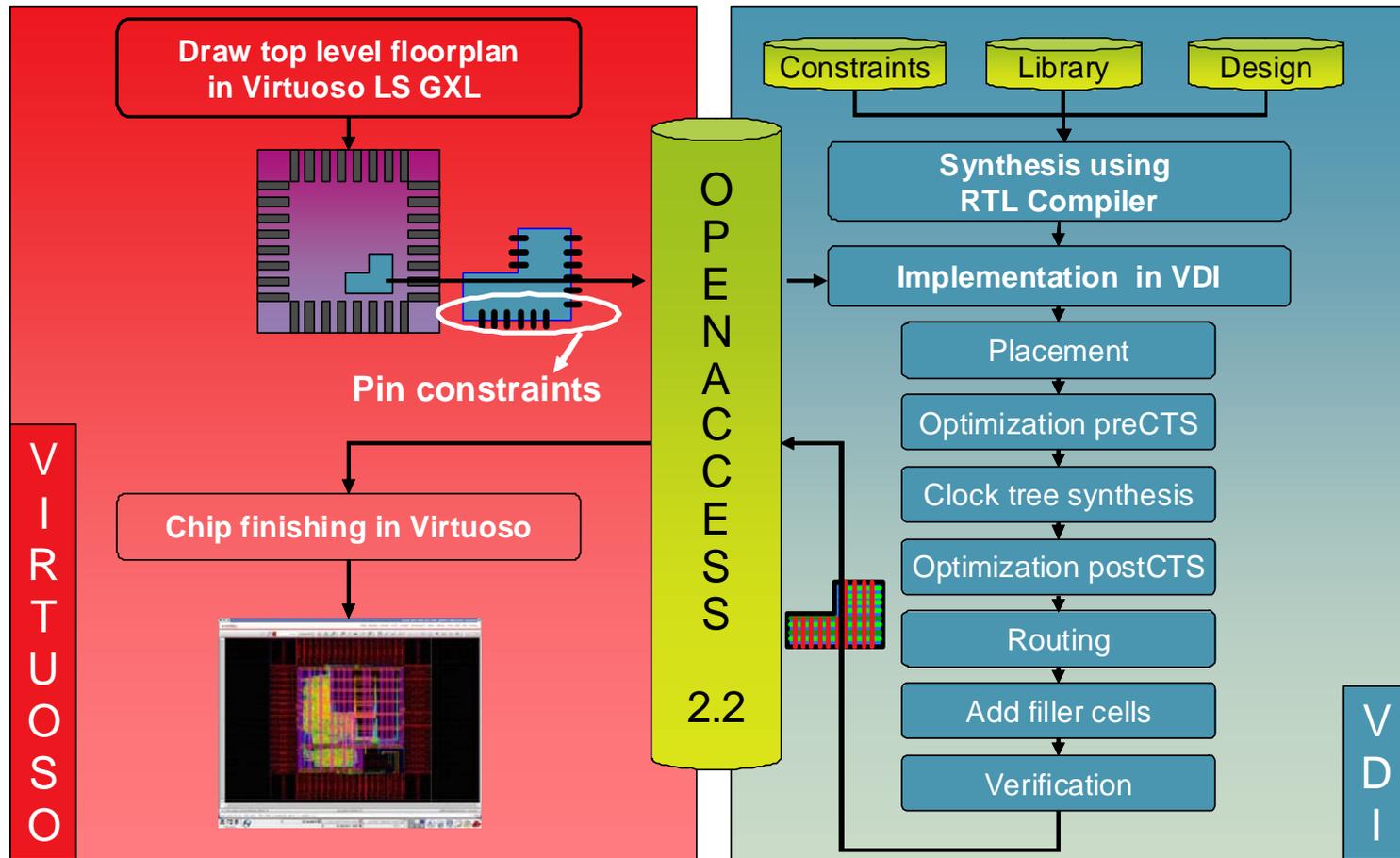
mouse L: Enter Point M: Rotate 90 R: Pop-up Menu

34(44) | Point at the | X: 28.215 Y: 31.055 (FS)Select: 1 Sel(N): 0 DRD: E CAE: OFF dX: -10.045 dY: 45.075 Dist: 46.1807 Cmd: Move

Scénario Mixed Design



Virtuoso digital implementation option *Perfect for “analog-on-top” design flows*



★ VDI uses Encounter and Nanoroute technology

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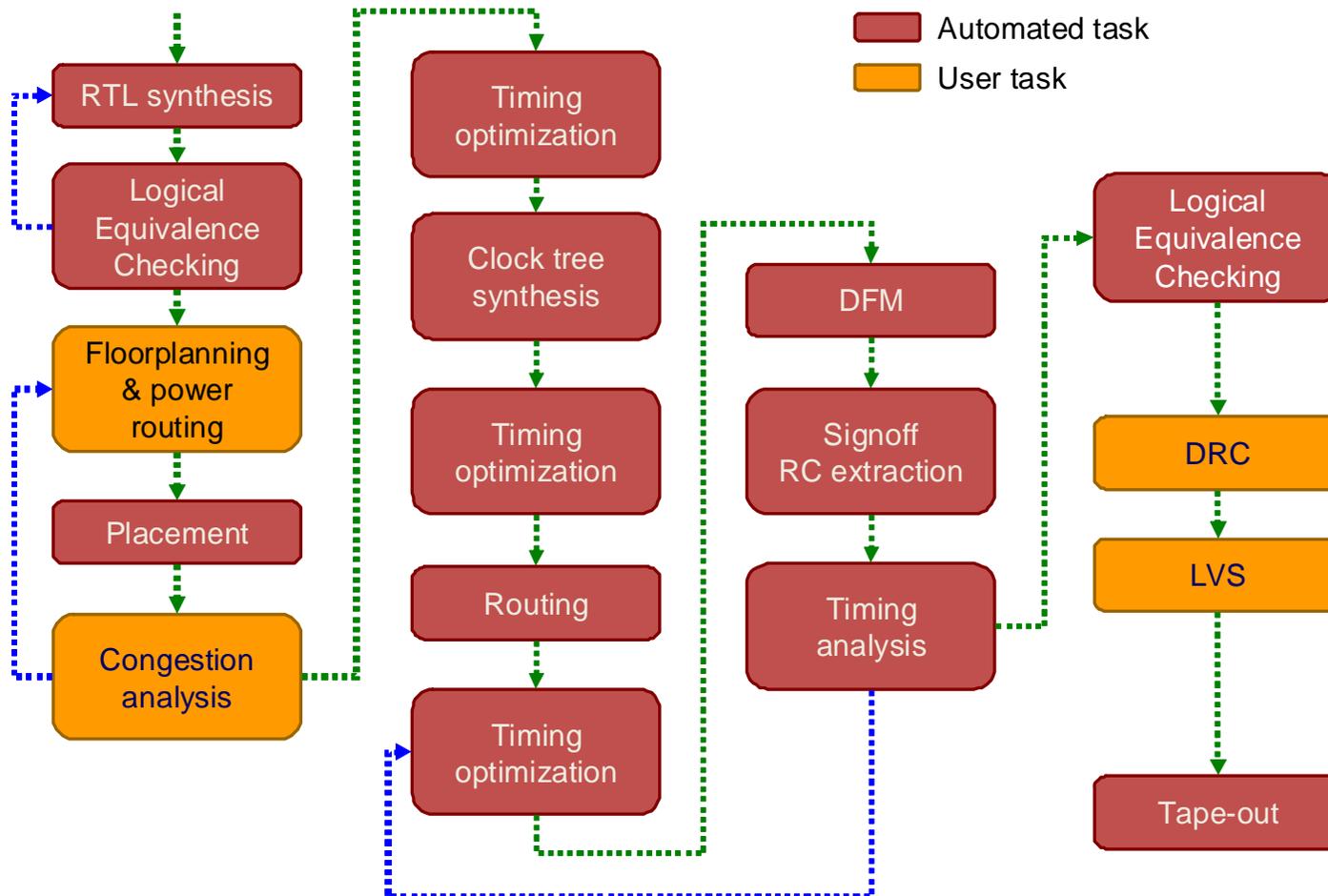
Configuration kit IBM 0.13 μ m “CERN By VCAD ”

Tools

Virtuoso 6.1.3 , SOC Encounter 7.1, Conformal 7.2, EXT 7.1.2 (QRC), Assura 3.2, Calibre 2008.3



Digital design flow



Digital ASIC @ IN2P3 – SoC + VDIO

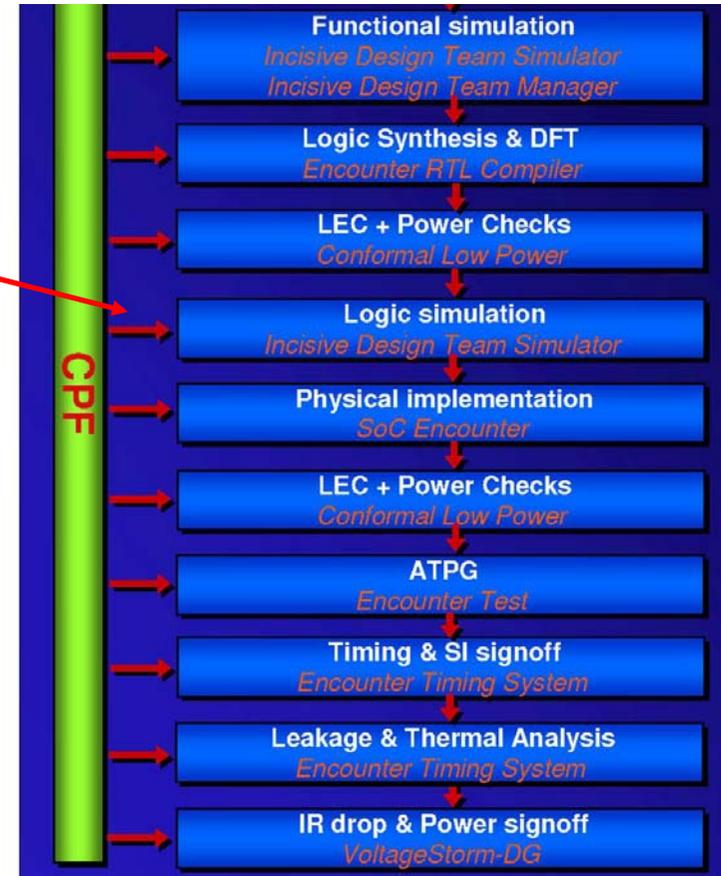
IC numérique Encounter			
FE200	ICD	SOC Encounter	SOC Encounter L, compatible SE
FE200GPS	ICD	SOC Encounter -XL (aka SOC Encounter - GPS)	SOC Encounter XL
RCV200	ICD	Encounter RTL Compiler w/formal vérification (Replace RC200)	Compatible BuildGates BGX5.15-s064 et RC200 Compatibilité RC 5.1
3002	CD	Virtuoso Digital Implementation Option	Version légère de SOC Encounter et RT Compiler, 50kGates
CFM100	ICD	Encounter Conformal L (a.k.a Conformal ASIC)	Vérification formelle
FE725	ICD	Encounter Timing System XL (contient Celtic pour VDIO)	Timing test (Celtic) pour VDIO
CFM400	ICD	Encounter Conformal Constraint Designer - L	Version légère de SOC Encounter et RT Compiler, 50kGates
TDE001	CD	Encounter Test Architect - L	Insertion structures de test
TDE002	ICD	Encounter True Time Test -L	Génération vecteurs de test
VSDG	ICD	Dynamic Gate Option to VoltageStorm PE (Gate and	IR Drop & Power signoff
VSPE	ICD	Voltage Storm PE	IR Drop & Power signoff

Synthesis Product Packaging

VDIO (with 50K* instances max)	
Capacity Limit	G-200K/M-50K
Global synthesis engine	✓
ChipWare	✓
Power exploration and estimation	✓
Power optimization (MVT, clock gating)	✓
DFT analysis & fixing	✓
Scan insertion	✓
PLE wire modeling	✓
Retiming	
Superthreading master	
Top-down multi-supply voltage (MSV)	
Multi-mode	
Yield Optimization	
Power Shutoff (w/ CPF)	
DVFS	
Predict QoS	

Encounter Back-end Packaging

VDIO (with 50K* instances max)	
Capacity limit (instances)	50K*
Partitioning & Timing Budgeting	
Power Planning & Routing	✓
Placement (std. cell and Block)	✓
Timing Optimization (optDesign)	✓
Timing (CTE and SignalStorm)	✓
Clock Tree Synthesis	✓
Routing (Wroute & NanoRoute)	✓
Multi-Supp Multi-Voltage	✓
Multi-Vth	✓
FE RC Extraction	✓
Signal Wire / Manual Editing	✓
ECO	✓
FE Verify	✓
Celtic SI Analysis	
Clock Mesh support	
Yield Analysis	
MS (DoT) features (routing, AMS int.)	
OA Support	✓
GDSII Out	✓



Outils pour les principaux kits en usage

	AMS 0.35	IBM 130	Chartered 130	XFAB 0.35	IBM 90	UMC 0.13	ST 0.25
Core & IO Libs	Foundry	<u>Foundry</u> ARM	<u>ARM</u> Synopsys	Foundry	? ARM	<u>FARADAY</u> ARM	Foundry
Virtuoso	6.1	6.1	5.1	6.1	6.1	5.1 / ?	5.1
SoC / VDIO	X	X	X	X	X	X	X
Assura DRC-LVS	X	X		X	X	X	
RCX	X			X		X	
QRC		X			X		
Calibre DRC-LVS	Signoff	X	<u>Signoff</u>	Signoff	X		Signoff
xRC							
Hercules DRC-LVS		X	X		X		
STAR-Rcx			<u>X</u>				X
Magma LVS 3D?			X (Tezzaron)				



■ Flot de conception CMS → Cadence-Mentor-Synopsys

- ↳ Accès à tous les outils
 - Europractice à travers les pôles
- ↳ Mise en Oeuvre / Maintenance
- ↳ Formation sur outils autres que Cadence

■ Cores & IO cell libraries

- ↳ Si externe (ex ARM)
 - Accès au programme universitaire
 - Pas de maintenance
 - Reconstitution des librairies
 - GDS2 + DEF + Modèles +Tech files
 - Cohérence du flot
 - Négociation d'un support

↳ Black box / macro

- Bibliothèque industrielle AMS dans les pôles

↳ Radtol / SEL & SEU free

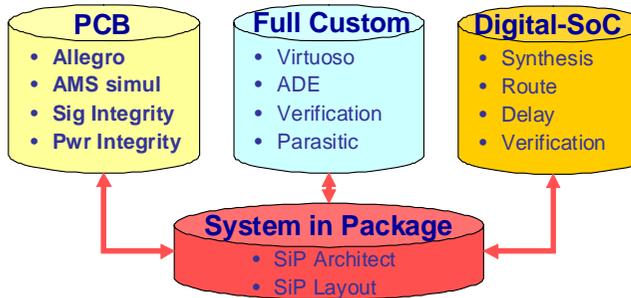
↳ RAM blocks / Memory compiler / IP

■ OK pour IBM 130

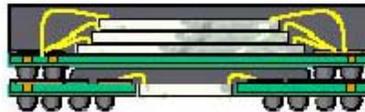
■ Chartered ou autres ?

ALLEGRO – SiP → System In Package

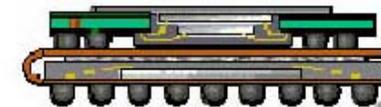
- Single package that combines all of the electronic components needed to provide a system or sub-system
 - digital ICs, analog ICs, RF ICs, passive components or other elements)



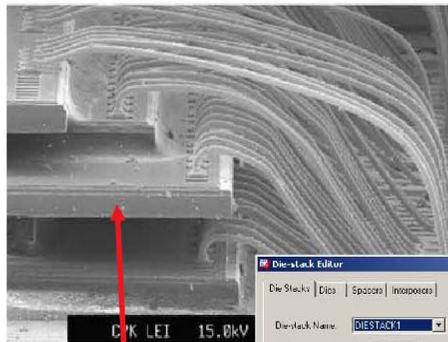
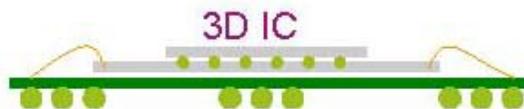
Die stacking



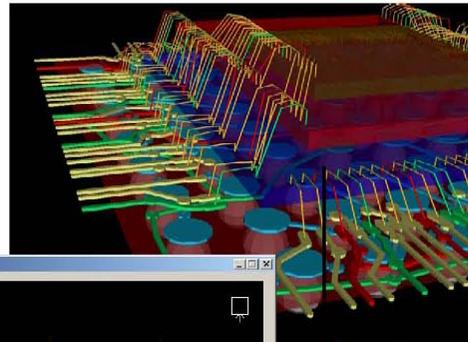
Package-on-package



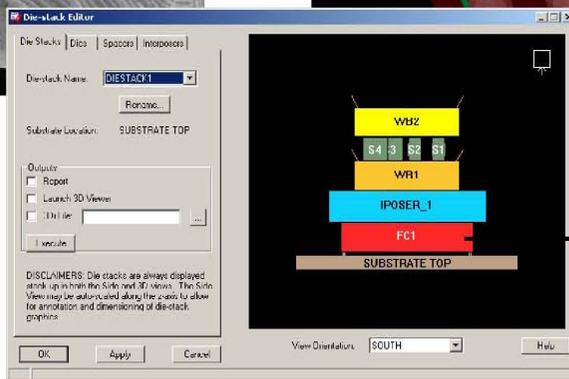
Complex die stack design



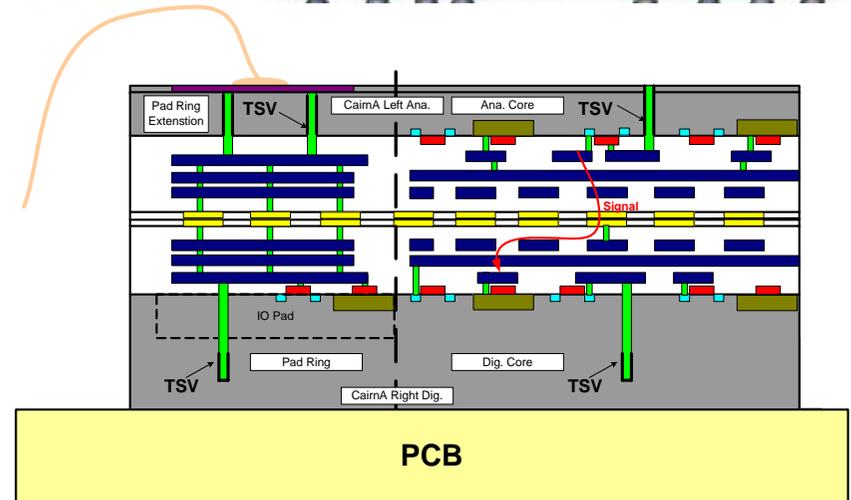
Actual Stack Design



3D Stack Viewer



3D Stack Design



CAIRN A

Gds2 Tier1 & 2 + PCB database

Conclusion: Utiliser Virtuoso 6 comme vecteur d'évolution

■ Solidifier les flots des kits (conf "IBM-CERN by VCAD")

- ↪ Méthodologie du flot
 - Mixed layout platform
 - Vérification formelle

■ Augmenter la méthodologie de travail → Equipes / Pôles

- ↪ Aide à la documentation intégrée
- ↪ Constraint manager, Mixed floorplanning, Chip estimate
- ↪ Outils de haut niveaux GXL
 - Qui routent en maîtrisant les >1000 règles de design
 - Caractérisation, Virtuoso Custom Router

■ Travailler en amont, plus grande interaction avec

- ↪ Les électroniciens du PCB, Intégration des ASIC au détecteur → Construction d'échelles
 - Modèles des ASICs (IBIS, BSDL)
 - System in Package
- ↪ Les numériciens → Toujours plus de fonctionnalités intégrées dans les ASIC
→ Pilotage / RO des ASIC par FPGA
 - Modèles communs avant partitionnement et ciblage
 - INCISIVE, + FPGA suites: Synplify, ISE, Quartus
- ↪ Les testeurs → Cahier des charges de testabilité avant design
 - Scan Insertion
 - Test Pattern Generator
- ↪ Les mécaniciens
 - Visualisation 3D
 - Simulation thermique

■ → De nombreux outils sur lesquels se former

- ↪ Formations dédiées



Difficulté à maîtriser
toutes les
fonctionnalités quand
on va du FE au BE