12 bit – 25 MHz – Pipeline Analog to Digital Converter

Ecole de Microélectronique IN2P3
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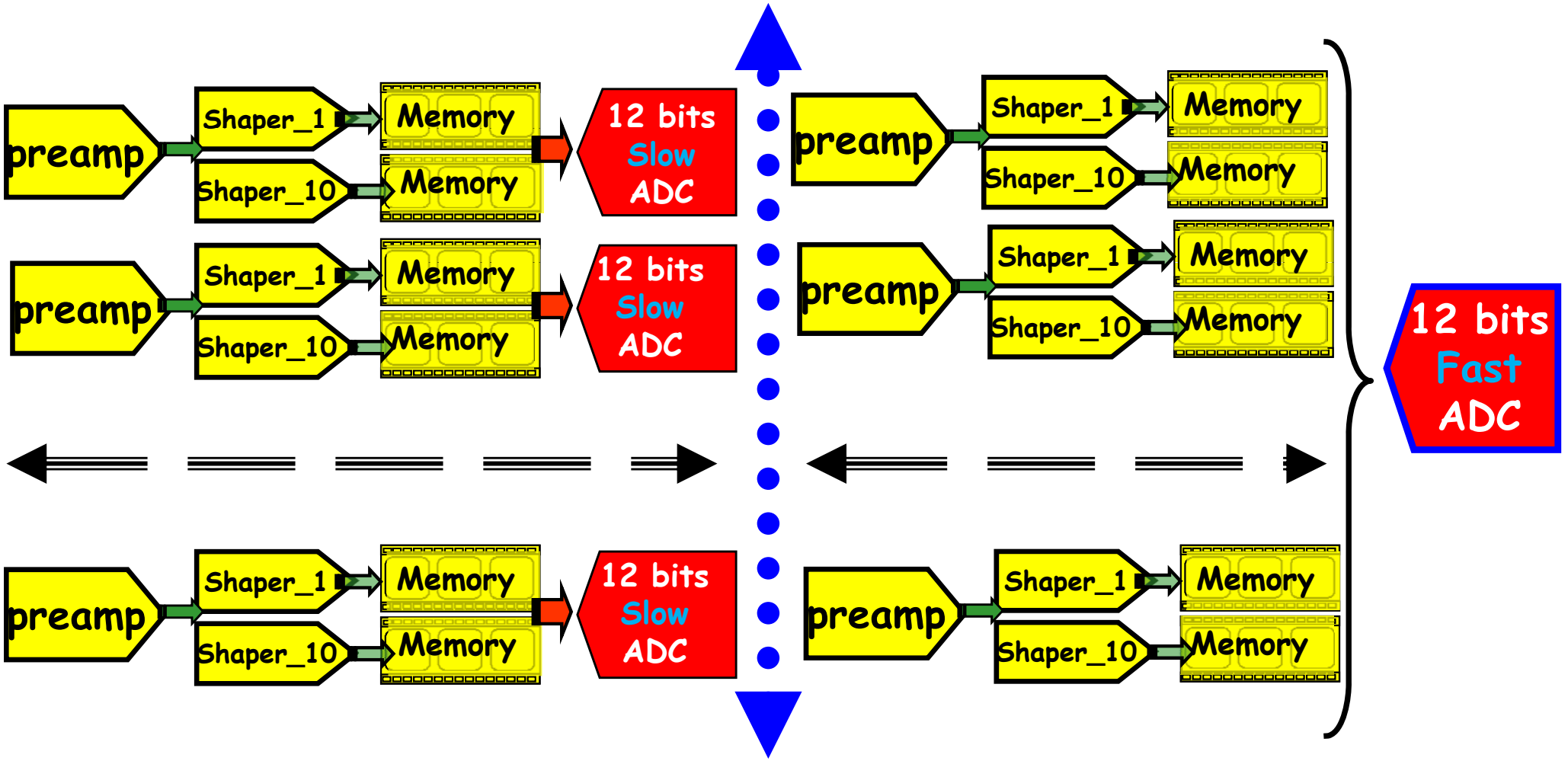
Outline

- Architecture project
  - ADC: 1.5 bits
  - ADC: 2,5 bits
- ADC test
  - ADC parameters
    - Static parameters
    - Dynamic parameters
  - Test method
- Conclusions

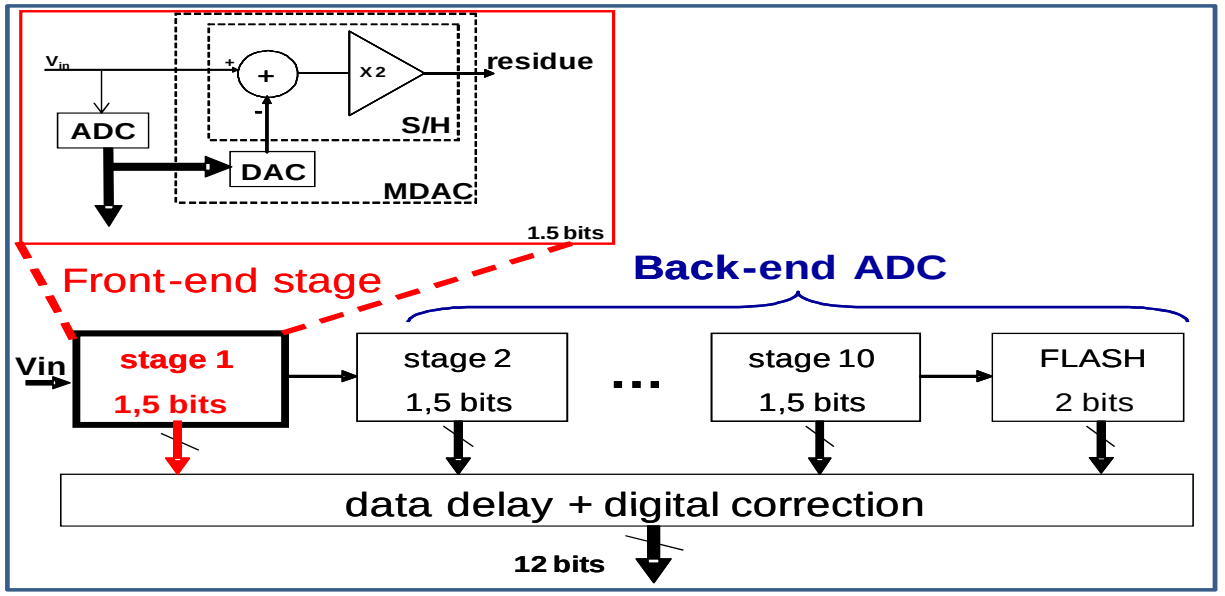
Slow vs High speed ADC configuration
ILC – ECAL configuration



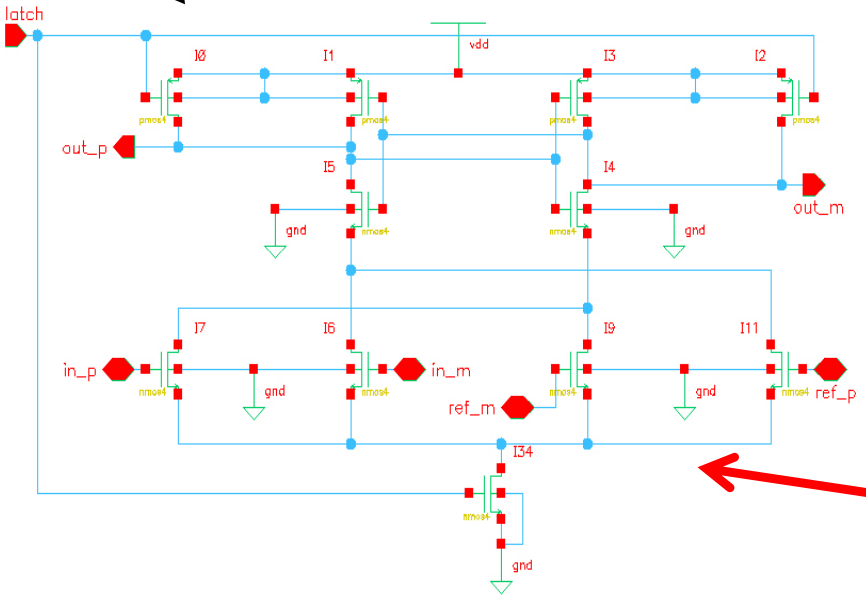
High speed ADC industrial purpose

- **MEMS**
  - Gyroscope
  - Accelerometer
- **Imaging applications**
  - Infrared Bolometer
  - Cryogenic Bolometer
  - Nanowire sensor (LOAG Lab)

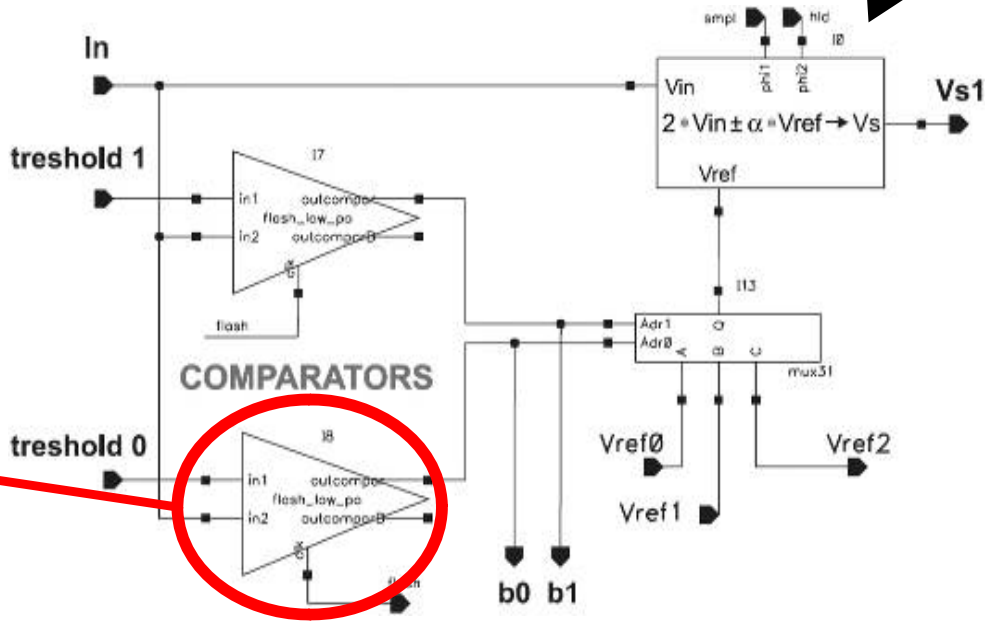
Pipeline ADC architecture (1)



Dynamic Comparator



1.5 bit MDAC



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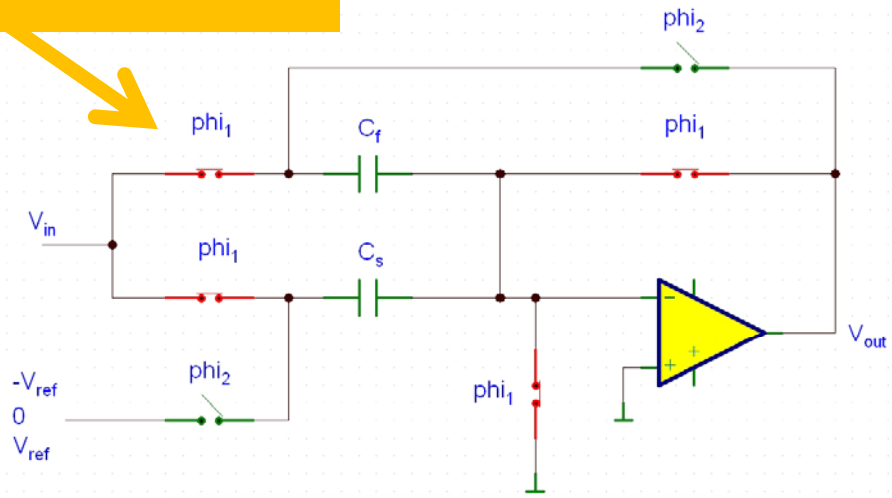
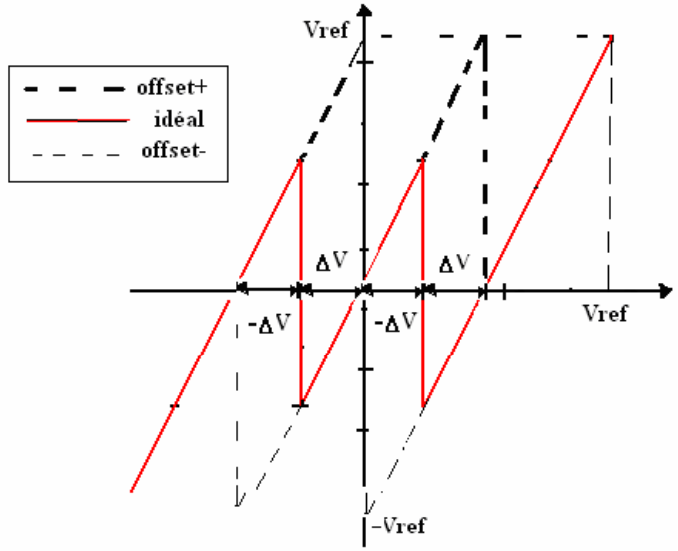
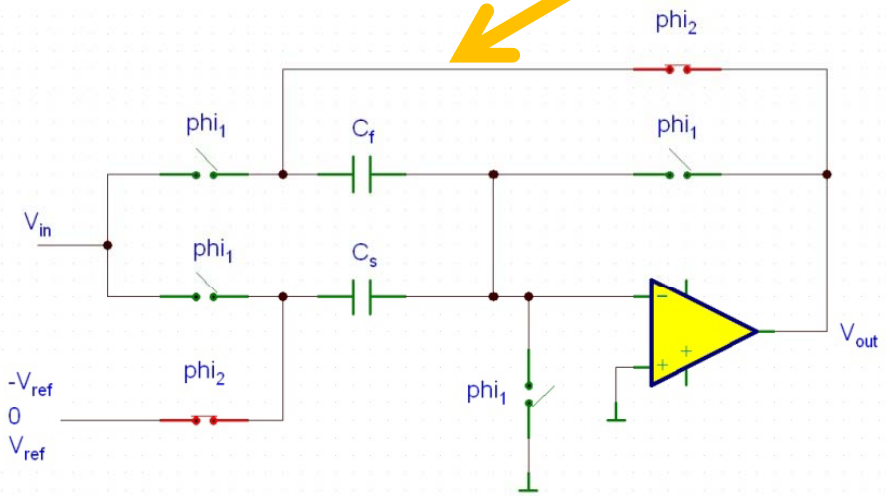
Pipeline ADC architecture (2)

Sampling phase



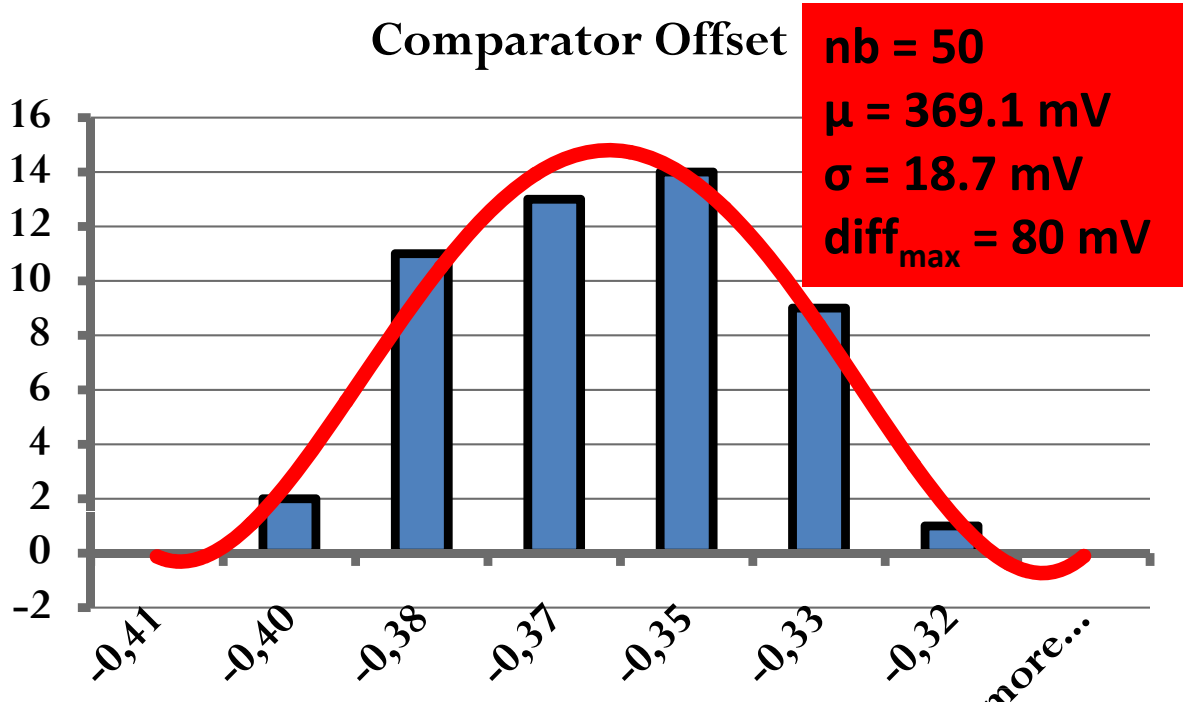


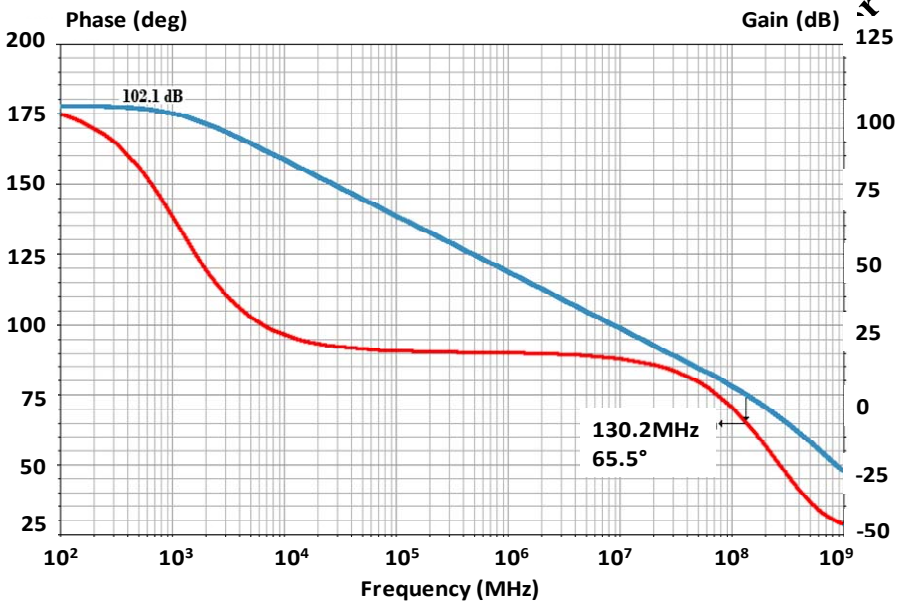
Hold phase



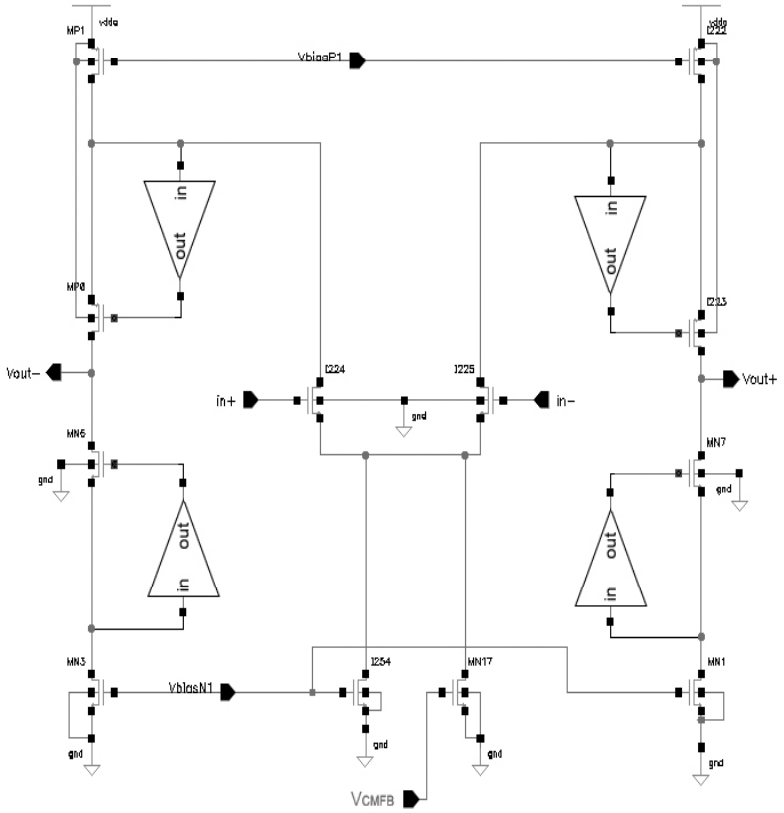
$$V_{out} = 2.V_{in} - d_i.V_{ref}$$
$$d_i = \{-1, 0, +1\}$$

Pipeline ADC architecture (3)

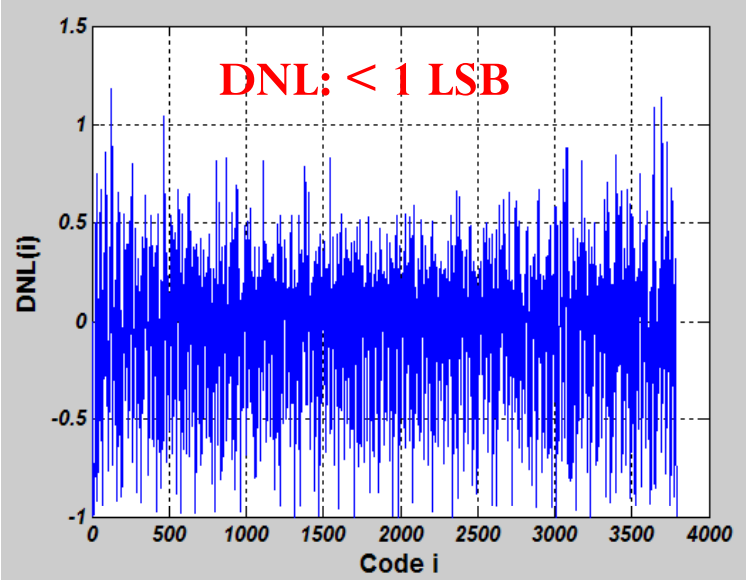


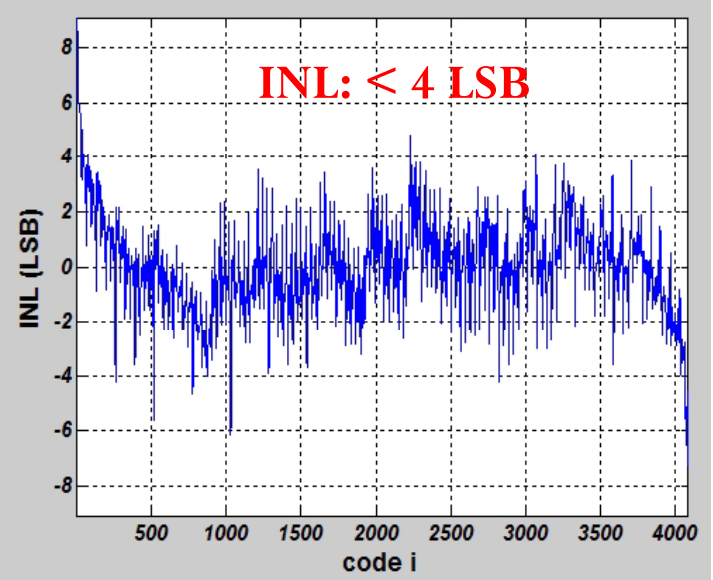


- ADC block:
  - 2 dynamic comparators
  - Offset allowed: $V_{ref}/4$

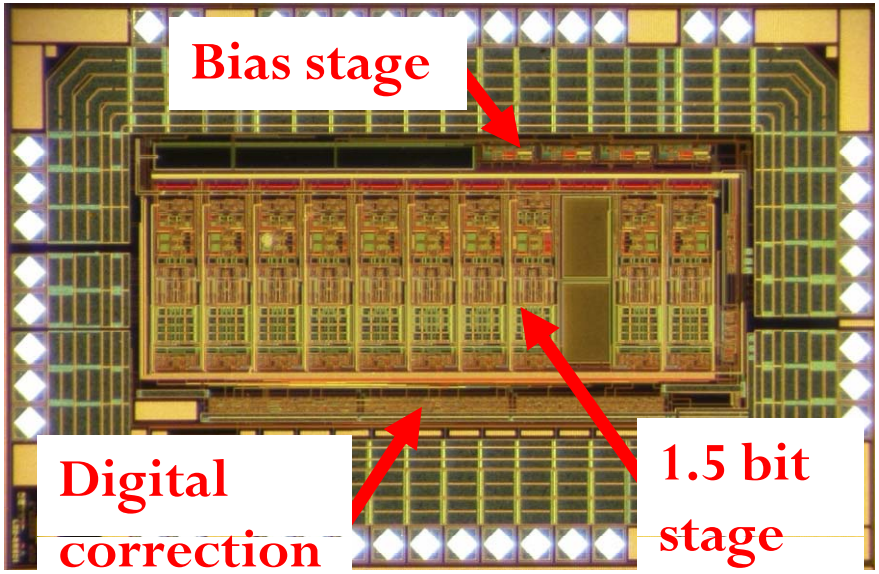


Full 1.5 bit Pipeline ADC

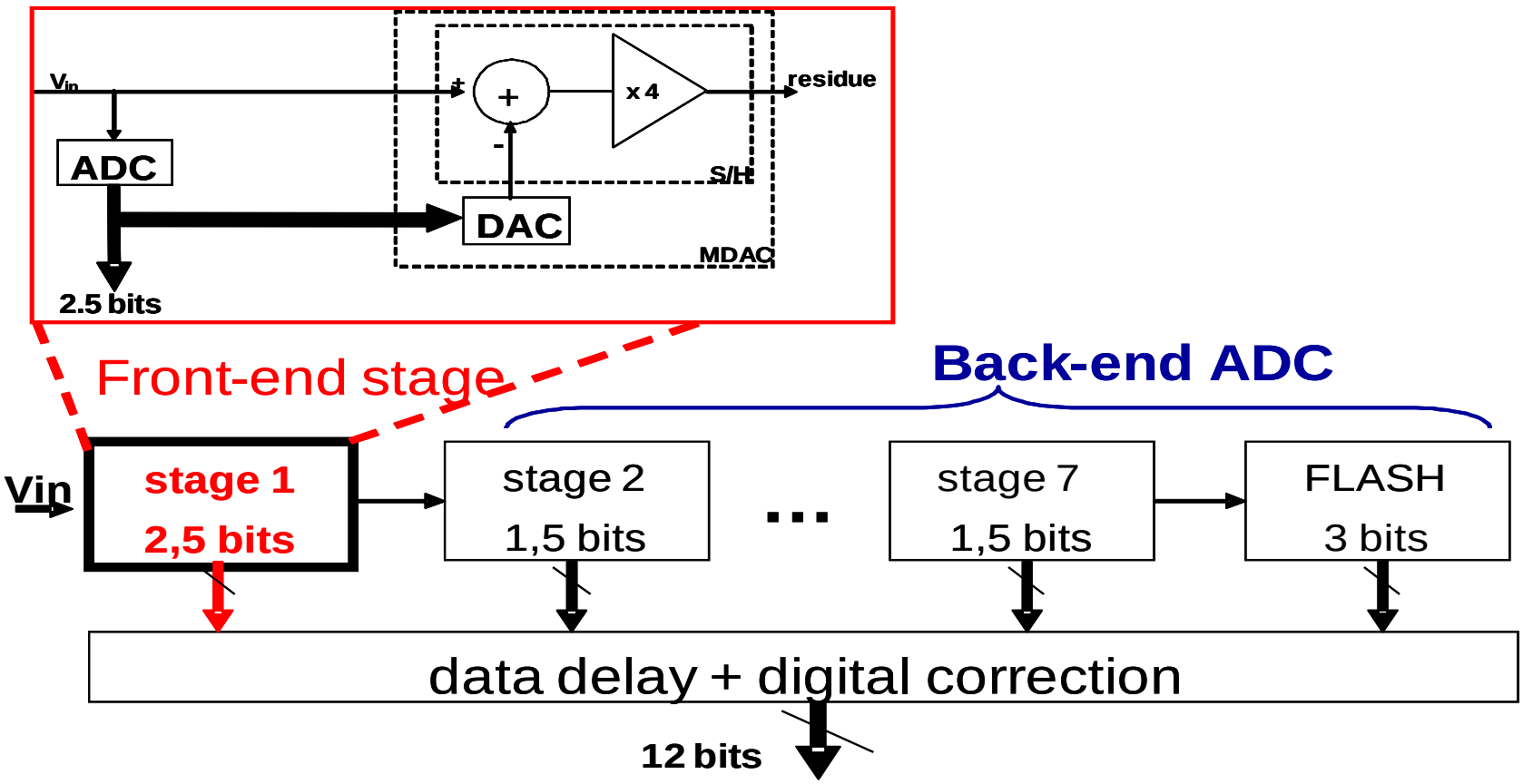




- Process matching is limiting to 10 bits
  - Increase resolution in 1st stage
    - Difficult to design OTA block
    - Comparator offset
    - **Capacitor Matching**
  - Digital gain correction
    - Dynamic Element Matching
    - Still under study



Pipeline ADC with Multi-bit first stage (1)

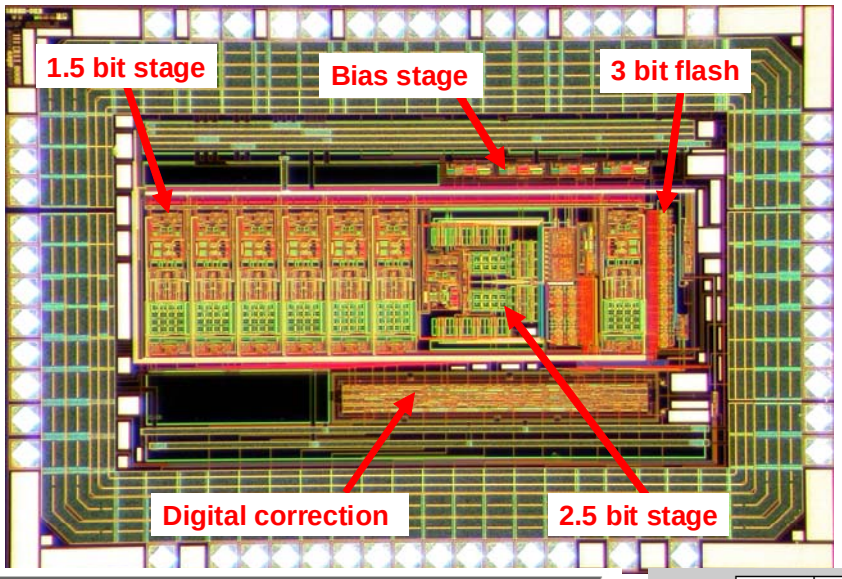


- Multi-bit 1st stage: 2.5 bit
  - MDAC with a gain of 4
- Back-end composed by 6*1.5 bit stage and a 3 bit flash ADC

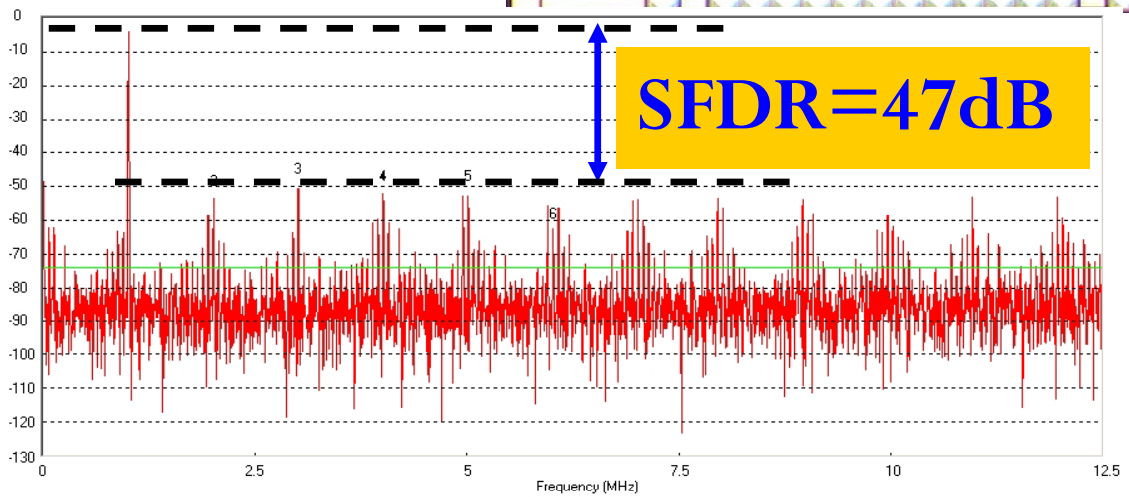
Pipeline ADC with Multi-bit first stage (2)

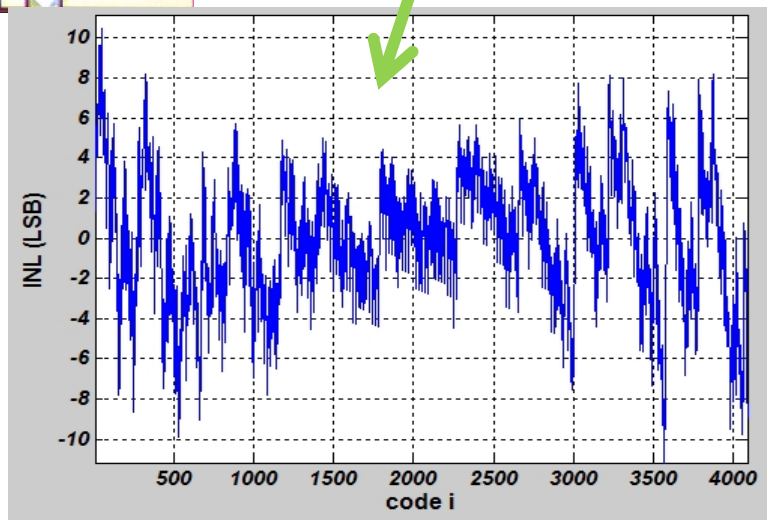
- Multi-bit 1st stage: 2.5 bit => 1st prototype

Capacitor Matching more critical on 2.5 bit stage

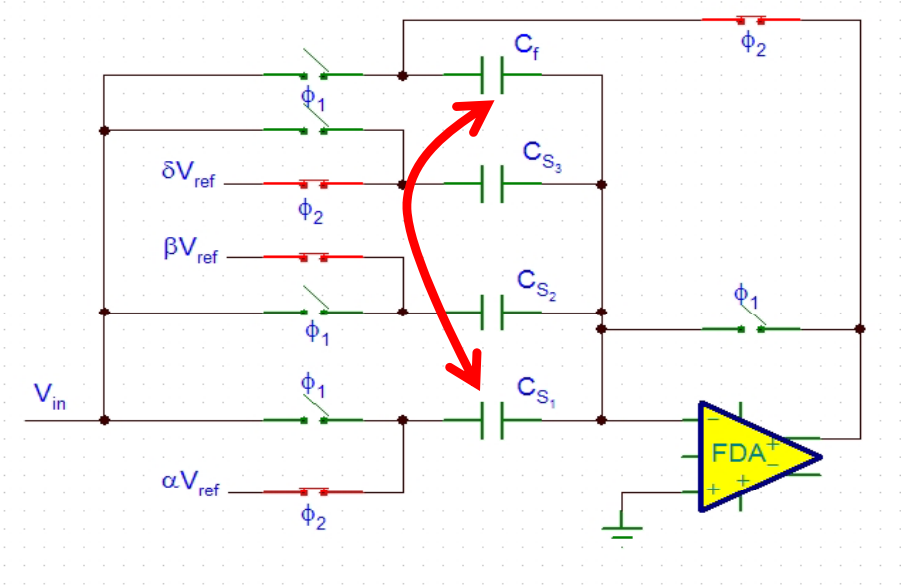


Linearity about ±8 LSB





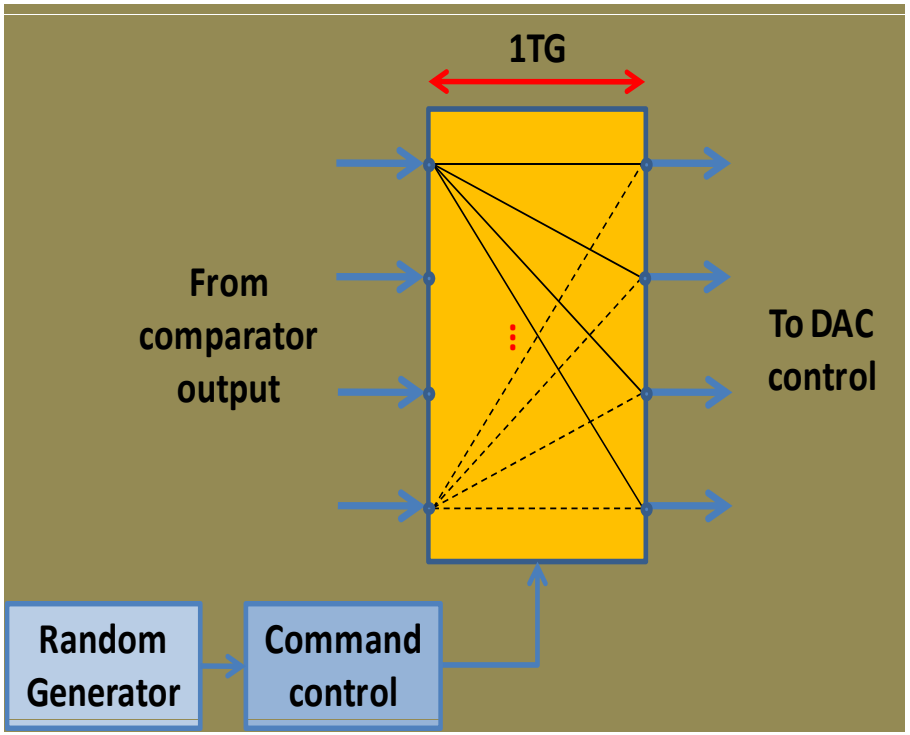
Pipeline ADC with Multi-bit first stage (3)



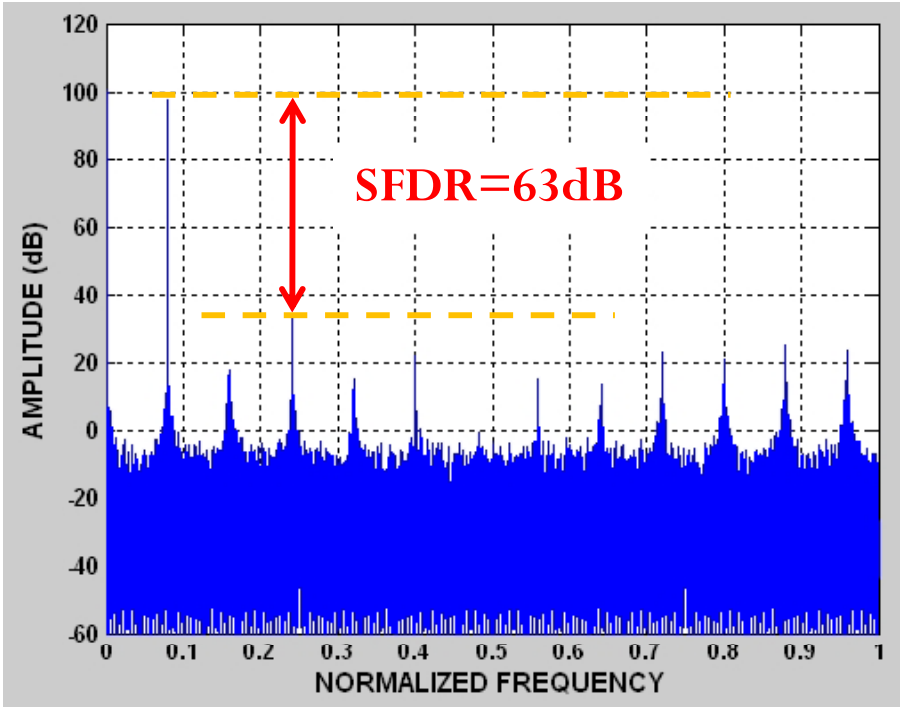
$$V_{out} = \left(\frac{\sum_{i=1}^{3} C_{s_i} + C_f}{C_i} \right) \times V_{in} \pm \alpha \times \left(\frac{\sum C_j}{C_i} \right) \times V_{ref}$$

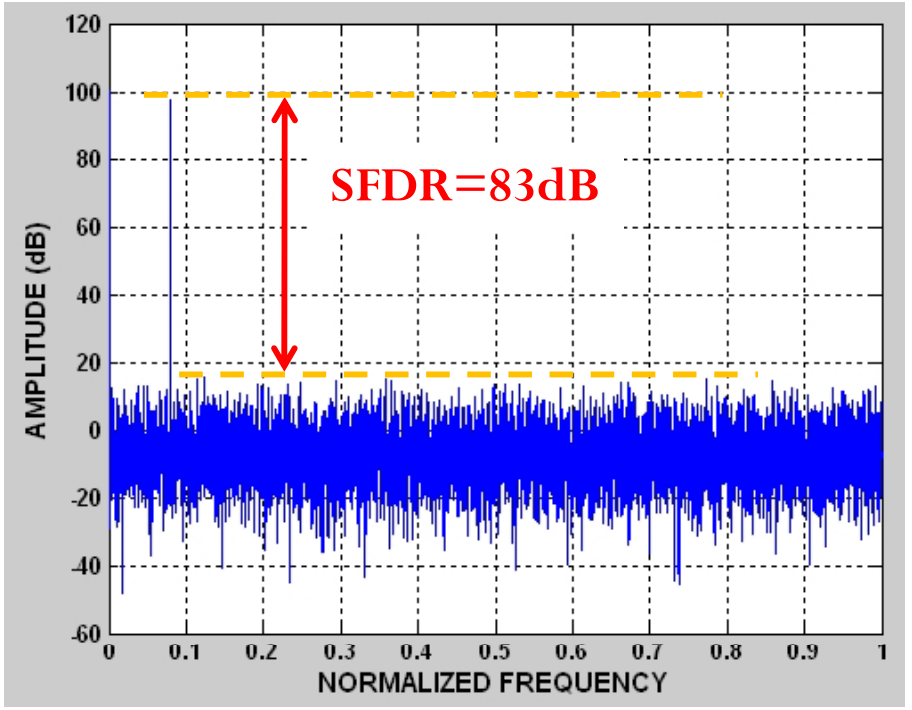
$$i = \{1,2,3,f\}, i \oplus j = 0$$

- Dynamic element
  - Random selection of the feedback capacitor
    - Closed loop Gain modulation
  - 1 Transmission gate from comparator output to DAC control
  - Distortion => Noise

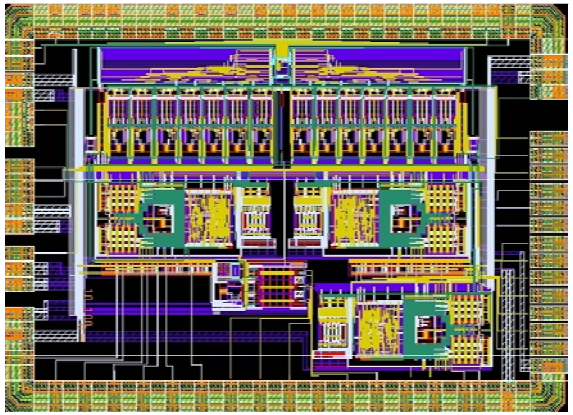


Pipeline ADC with Multi-bit first stage (4)





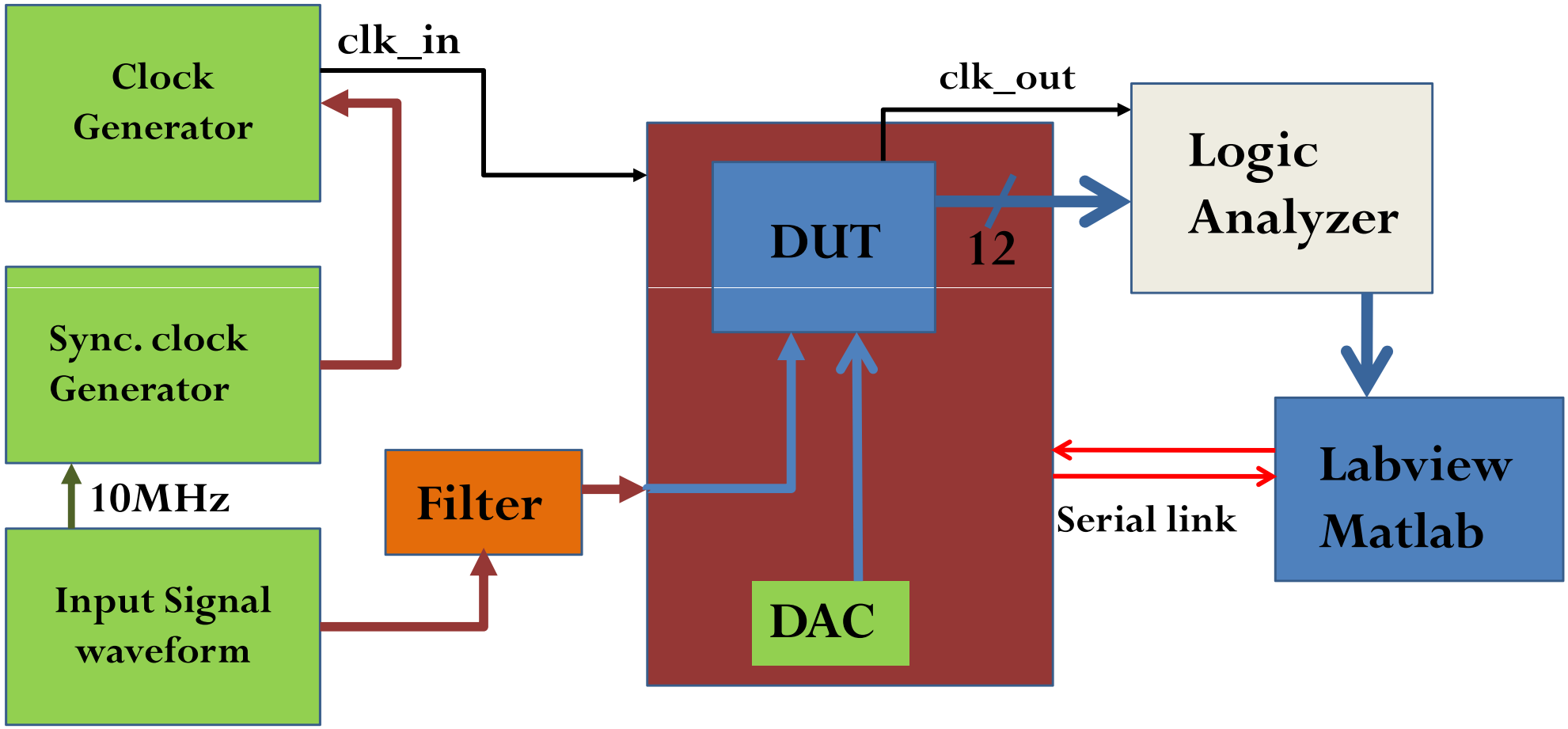
- Dynamic Element Matching: MATLAB simulation
  - Distortion => Noise
  - SFDR is increased
    - Improve linearity



Submitted on September 09

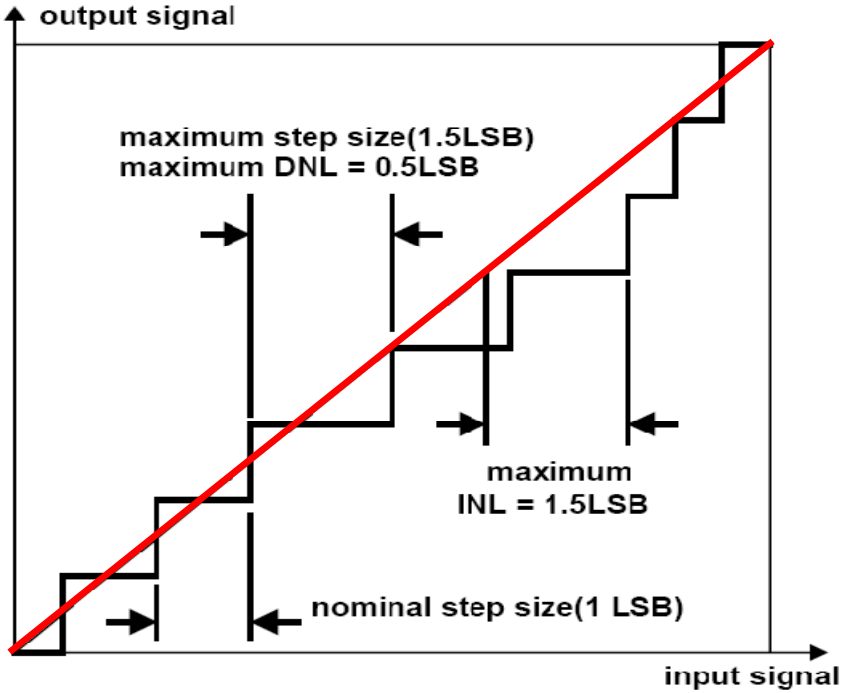
ADC test: Configuration

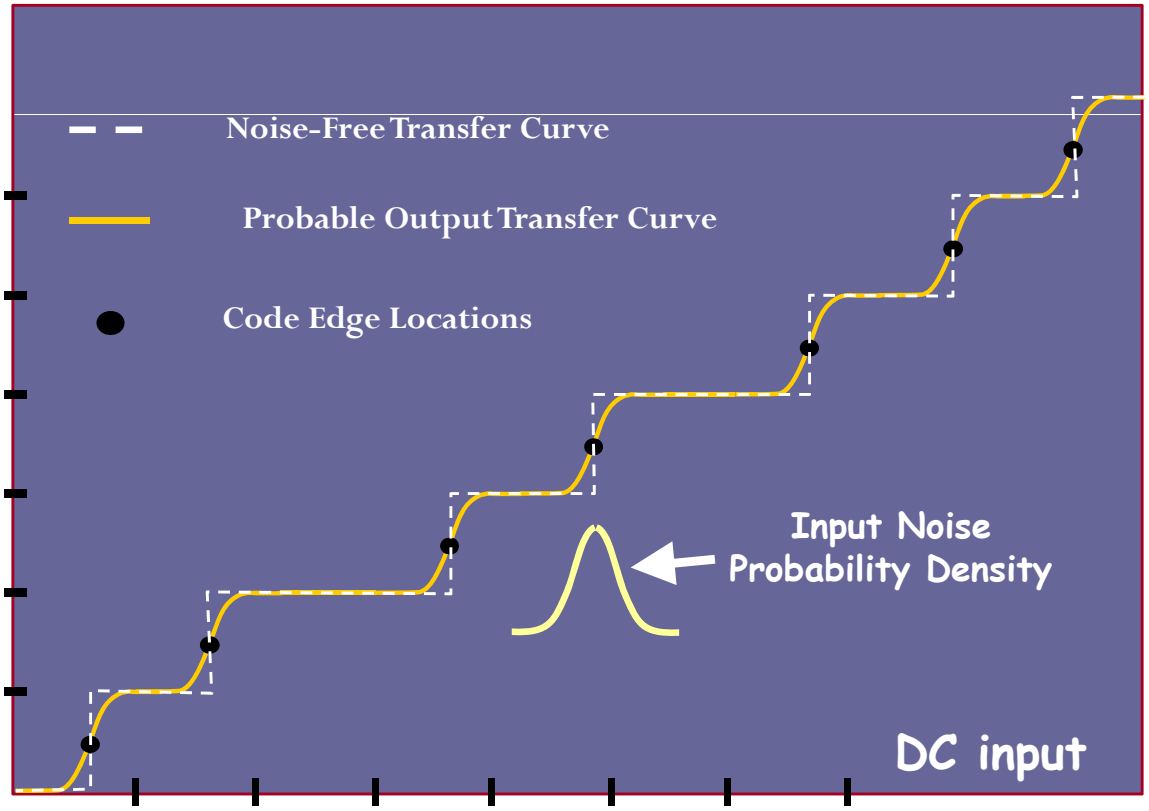
- Test configuration



ADC test: parameters (1)

- Static parameters
  - Differential Non Linearity (DNL)
  - Integral Non Linearity (INL)
  - Noise



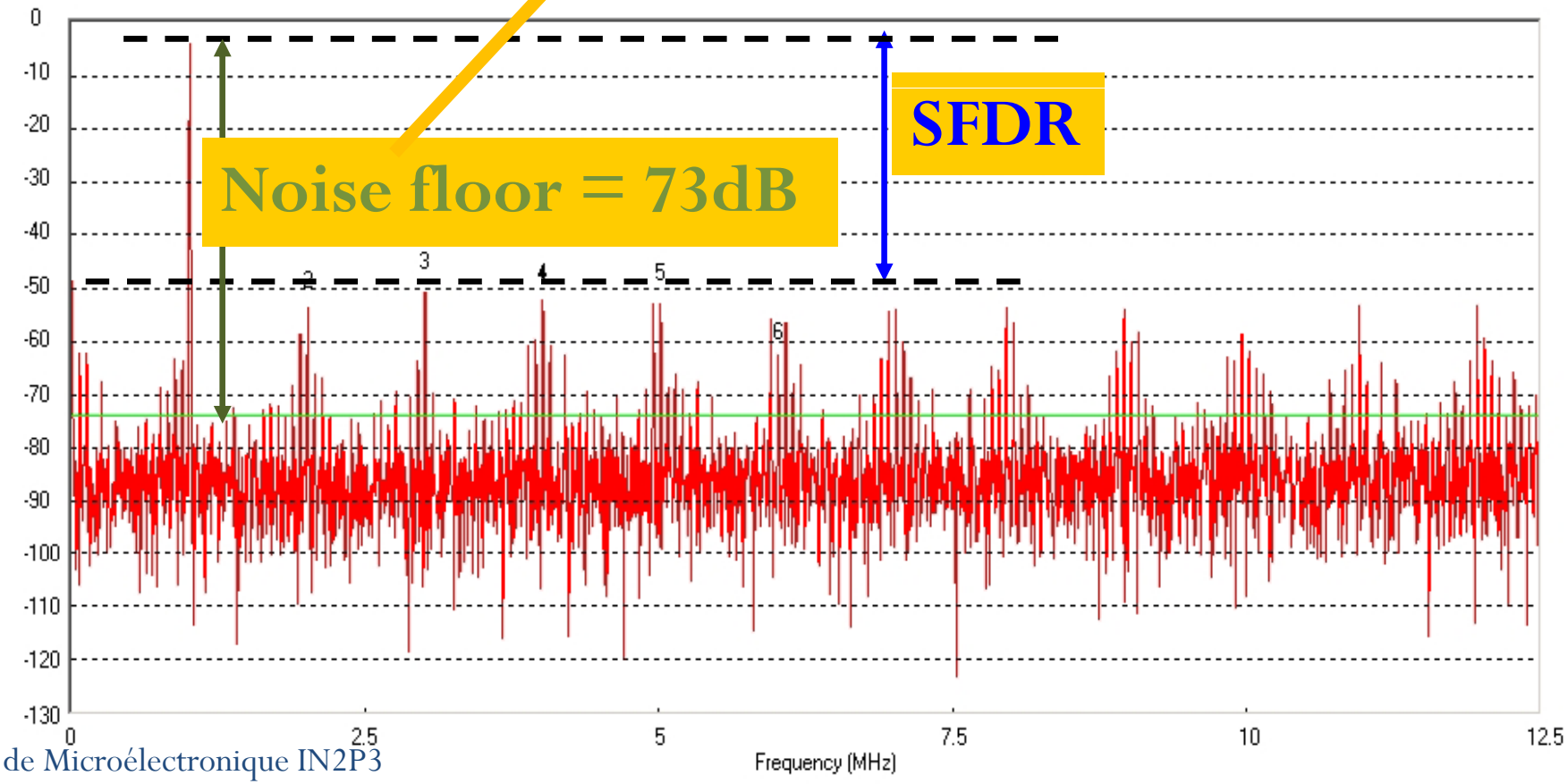


ADC test: parameters (2)

- Dynamic parameters
  - Noise floor => SNR
  - SINAD => ENOB
  - SFDR => Linearity
  - …

$$\frac{SINAD - 1.76}{6.02}$$

$$SNR + 10 * \log_{10}\left(\frac{M}{2}\right)$$

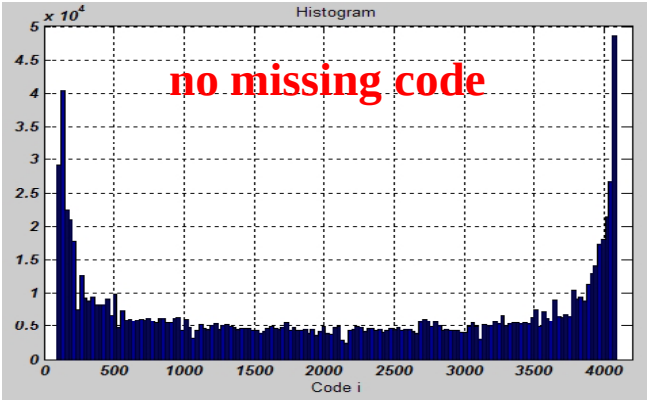


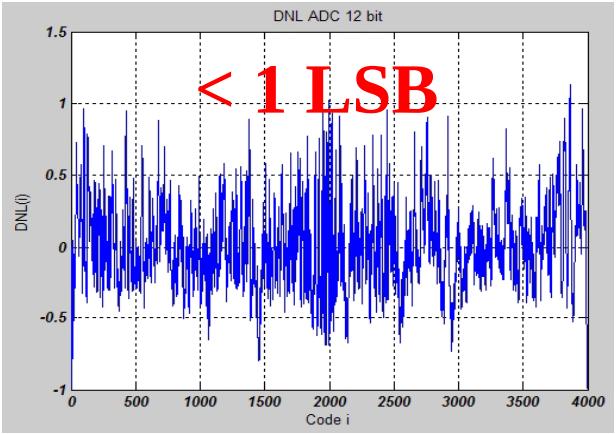
Test Method (1): Full 1.5 bit stage ADC

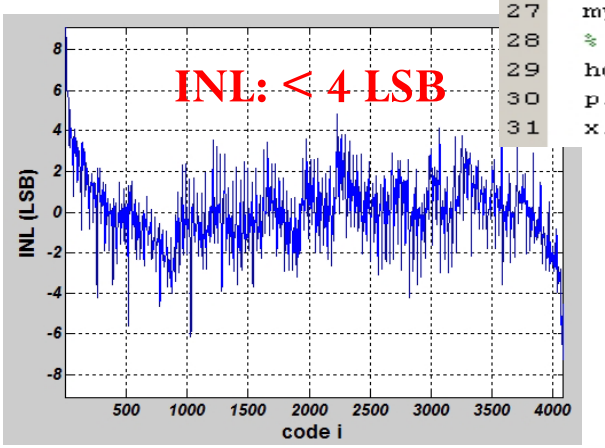
- Tools: Labview + MATLAB
- Ramp input signal
  - DC parameter extraction (Labview)
    - Step size = LSB
    - > 100 points by step
    - INL: fit of the output transfer function
- Sine wave input signal
  - Static parameters => Histogram (statistical results) (MATLAB script)
  - Coherent sampling (excel script: MAXIM IC)
  - Dynamic parameters => FFT

Test Method (2) : Full 1.5 bit stage ADC

- Tools: MATLAB
- Sine wave input signal
  - Static parameters => Histogram (statistical results) (MATLAB script)








```
% DNL and INL extraction from histogram plot
my_minbin=min(my_data);
my_maxbin=max(my_data);
% Histogram plot
figure(1);
hist(dat,my_minbin:my_maxbin);
xlabel('Code i'); title('histogamme'); grid
my_h=hist(dat,my_minbin:my_maxbin);
% Cumulative histogram
my_ch=cumsum(my_h);
% Edge level
my_T=-cos(pi*my_ch/sum(my_h));
%linearise
my_hlin=my_T(2:end) - my_T(1:end-1);
% Cut min and max
trunc=2;
hlin_trunc = my_hlin(1+trunc:end-trunc);
% calculate DNL
my_dnl= [0 hlin_trunc/my_lsb-1];
misscodes = length(find(my_dnl<-0.9));
% DNL Plot
hold off; figure (2);
plot(my_dnl);
xlabel('Code i'); ylabel('DNL(i)');grid

% Calculate INL
my_inl= cumsum(my_dnl);
% INL Plot
hold off; figure (3);
plot(my_inl);
xlabel('Code i');ylabel('INL(i)');grid
```

Test Method (3) : Full 1.5 bit stage ADC

- Tools: MATLAB
- Sine wave input signal
  - Coherent sampling (excel script: MAXIM IC)

$$\frac{f_s}{f_{in}} = \frac{N_{tot}}{N_{wind}}$$

N_{wind} → prime number

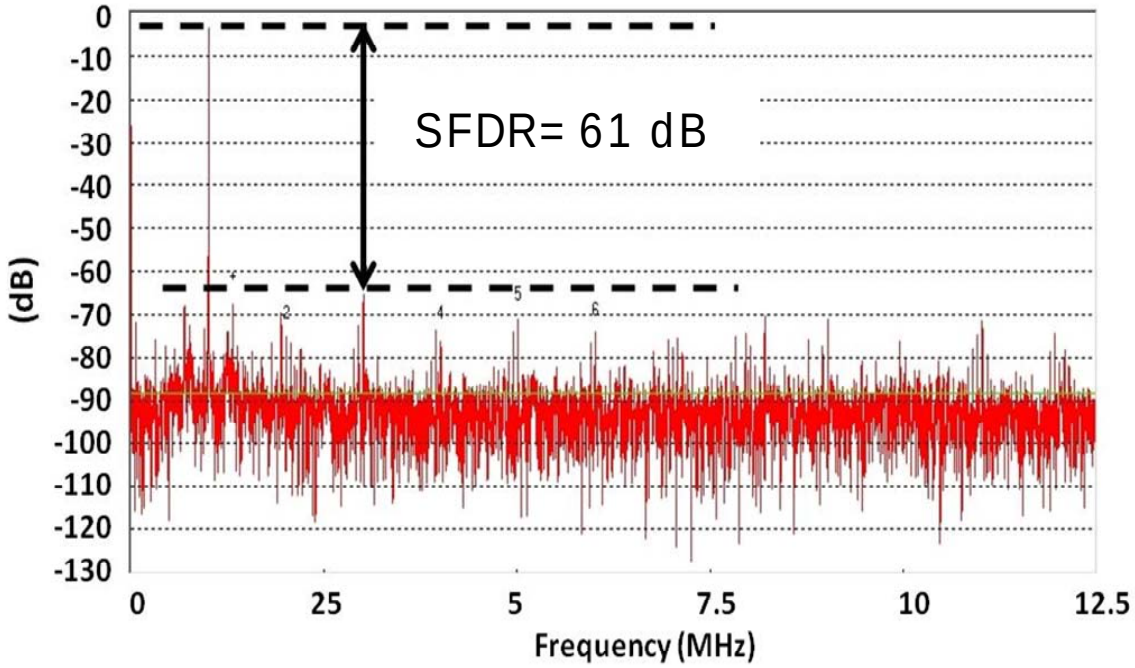
Example:

$f_s = 25\,MHz \quad f_{in} = 1\,MHz$

$N_{tot} = 2^{14}$

$N_{wind} = 657$

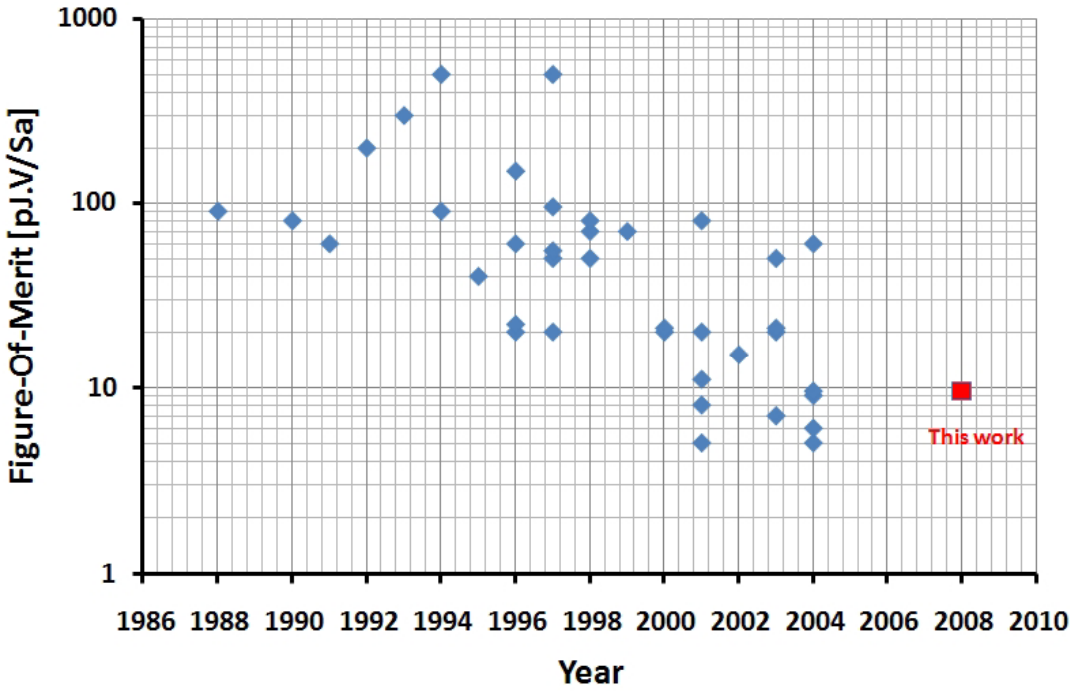
$f_{in} = 1.0025024414\ 06250\ MHz$



Conclusions (1)

- Pipeline ADC 25MHz - < 40mW
  - 2 versions: 1.5 bit stages, multi-bit first stage
- Figure of Merit (FoM) → ADC with full 1.5 bit stage

$$FoM = \frac{Power}{2^{ENOB} \cdot f_s} \bullet V_{dd}$$



Conclusions (2)

- ADC Test
  - Parameters
  - Methods

Testing results reliability

Depend very often

on SETUP & METHOD used

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Thanks for your attention