IN2P3 CSNSM LAL LURE IPN Orsay

Omega

OMEGAPIX

The first 3D IC prototype for the ATLAS upgrade SLHC pixel project designed at LAL

École IN2P3 de microélectronique
La Londe les Maures
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Orsay MicroElectronic Group Associated

Outline

- Chartered/Tezzaron 3D technology for the ATLAS upgrade SLHC pixel project

- Analog cell design: analog tier
  - Preamplifier
  - Shaper + Threshold DAC
  - Discriminator

- Digital cell design: digital tier
  - 24 DFF shift register

- Dedicated test chip

- Conclusion

SLHC upgrade: Aggressive requirements

SLHC : 10x increased luminosity => new RO electronics have to be designed

We are studying an alternative approach to:

- ✓ Minimize pixel pitch: study smaller pixels (50x50 µm² instead of 50x250 µm²)
- ✓ Target 3 µW/ch: 2 µW/ch for the analogue tier, 1 µW/ch for the digital one
- ✓ Design analogue tier with low noise low power preamp including shaping + threshold DAC
- ✓ Low threshold (1000 e-), low noise (100 e-)
- ✓ Discriminator in digital tier + dynamic memory

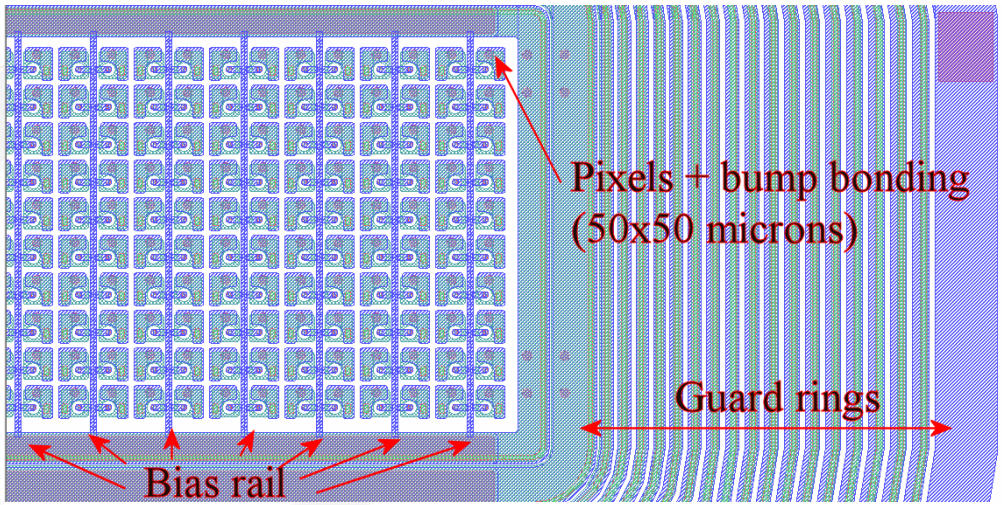
Goals:

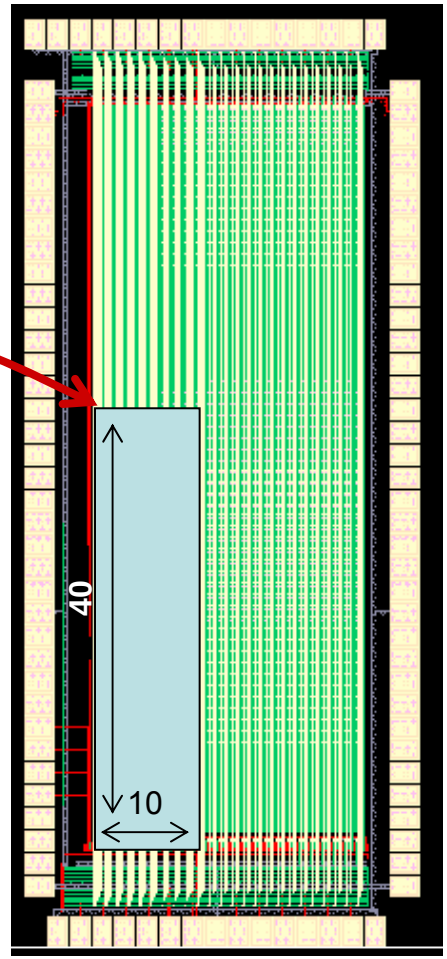
- ✓ Explore the Chartered 130nm CMOS techno and 3D features from Tezzaron
- ✓ Study variants of blocks for FEI4 (preamp, discri, DAC, local storage…)
- ✓ Study digital coupling to analog tier with discri in digital tier (not still implemented)

Pixel Matrix

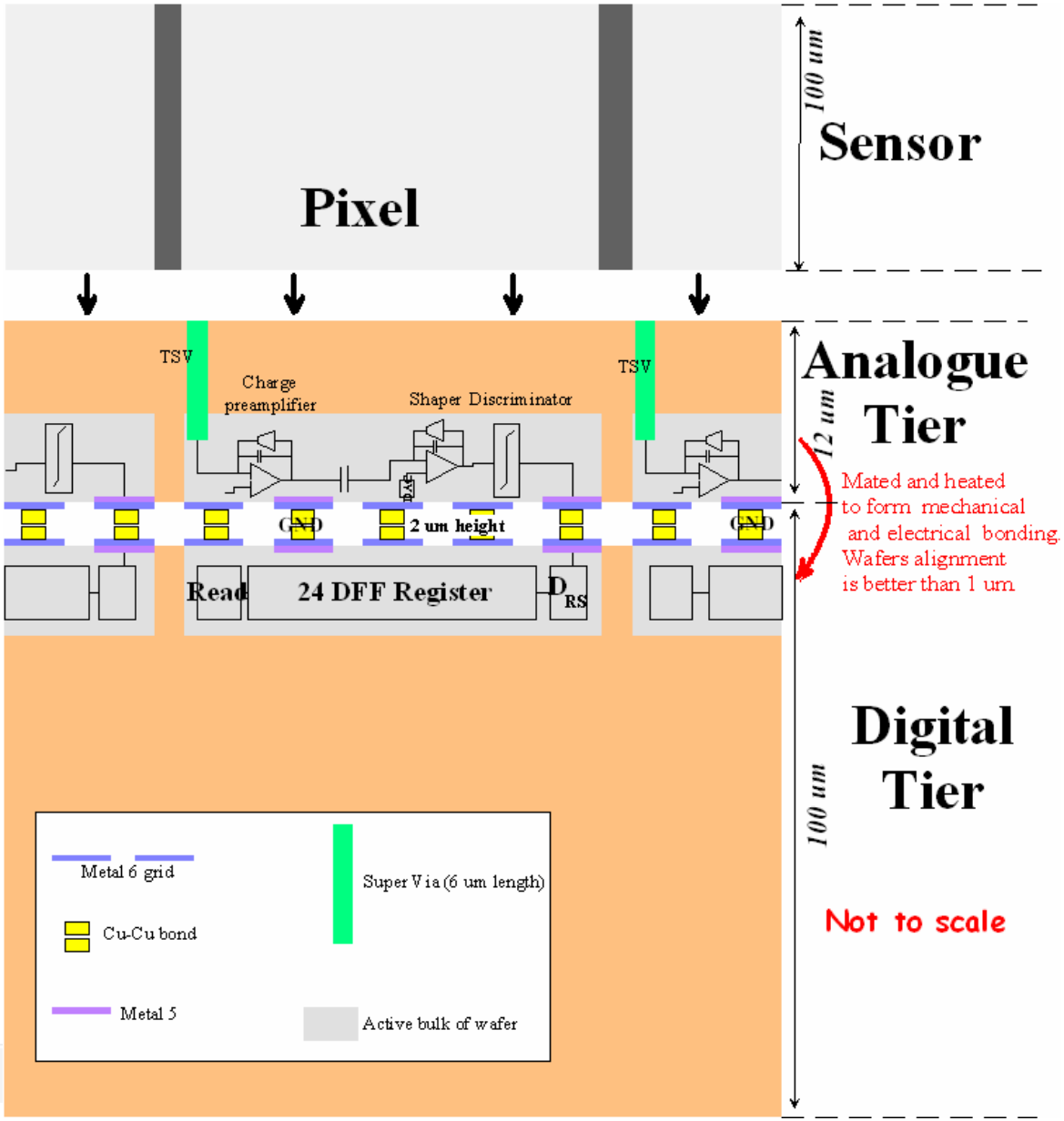
Plannar pixel sensor designed at MPI (Munich)

- ✓ n^+ pixels on p-type substrate
- ✓ 6,85 x 3,26 mm²
- ✓ 400 pixels
- ✓ 50 x 50 µm²
- ✓ 18 GRs
- ✓ thikness: ~ 100 µm but 75 µm expected at term





OMEGAPIX: first 3D IC prototype



OMEGAPIX is a two stacks 3D chip: analogue tier + digital tier. Sensor will be bonded directly on the back side of the thinned analogue layer.

Analogue channel: preamplifier + shaper + discriminator + DAC to fix the threshold

Digital channel: one 24 DFlipflop register

OMEGAPIX includes 1536 channels divided in 24 columns and 64 ch/col.

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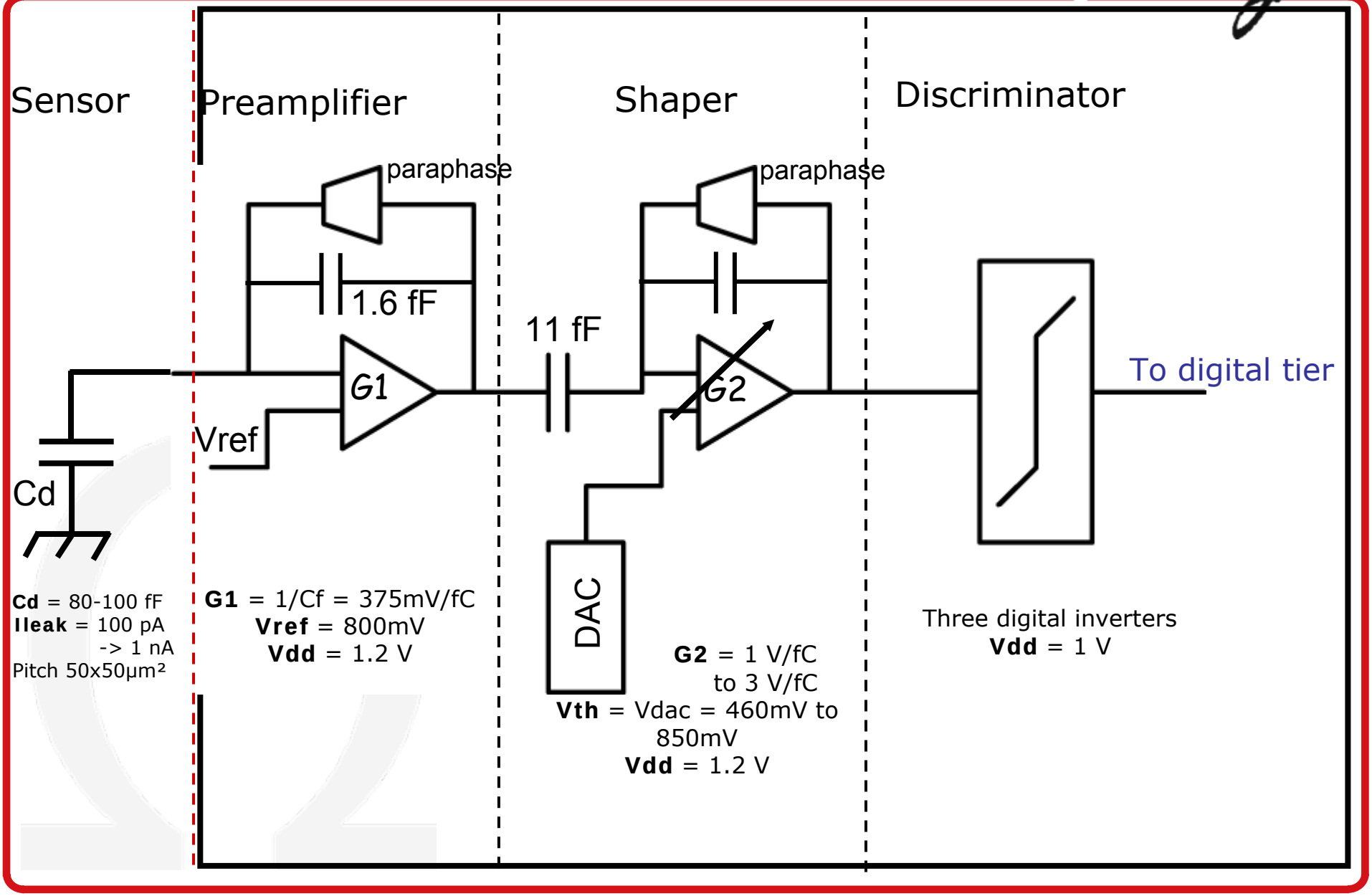
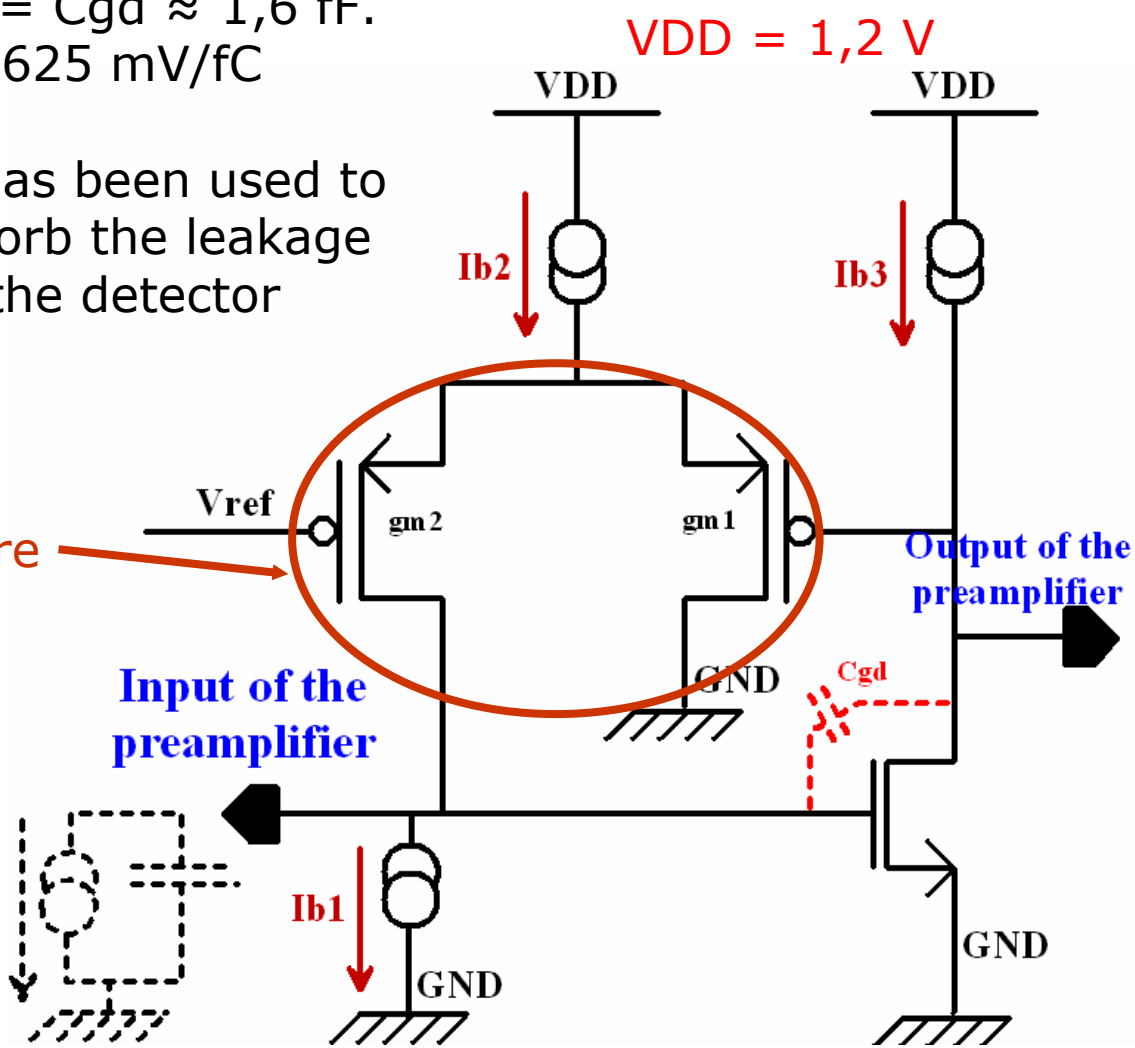
OMEGAPIX: Analogue tier



✓ Parasitic capacitance Cgd performs the feedback capacitance: Cf = Cgd ≈ 1,6 fF. Ideal gain is 1/Cf -> 625 mV/fC

✓ A paraphase structure has been used to fix the DC points and absorb the leakage current coming from the detector



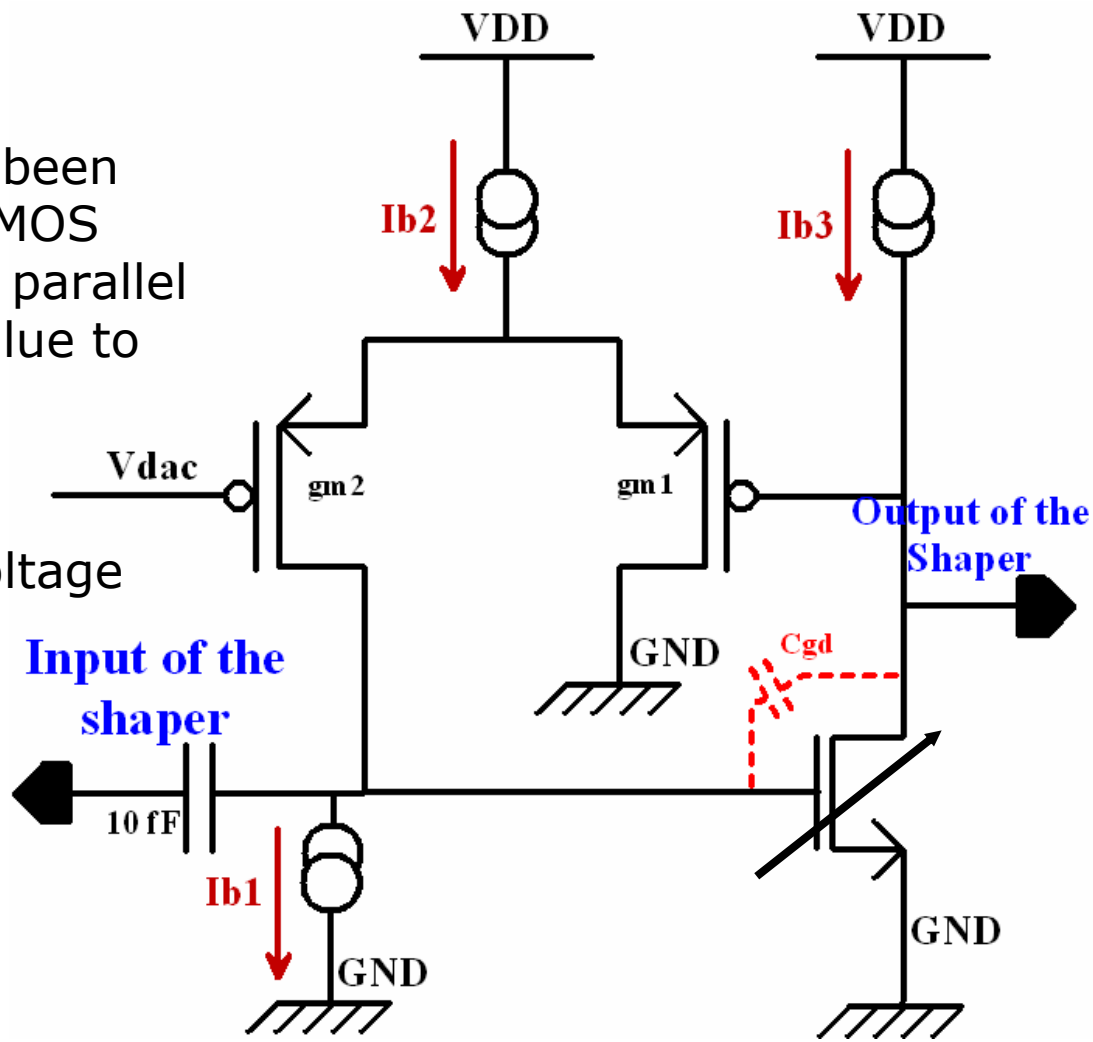
Ib1 = 100 pA, Ib2 = 2 nA, Ib3 = 1 µA

Req = 180 MΩ if Ib1 = 100 pA
Req = 74 MΩ if Ib1 = 1 nA

Ib1 = 2.5 nA, Ib2 = 5 nA, Ib3 = 50 nA

A shaper variable gain has been designed; four different NMOS transistors can be switched in parallel which leads to make Cgd value to vary

DAC fixes the output DC voltage



OMEGAPIX: typical simulation

Simulation conditions: Qinj = 1000 e-
DAC: 1000 (only 2.5/0.5 nmos_1p5_lvt as shaper), Vth = 800 mV

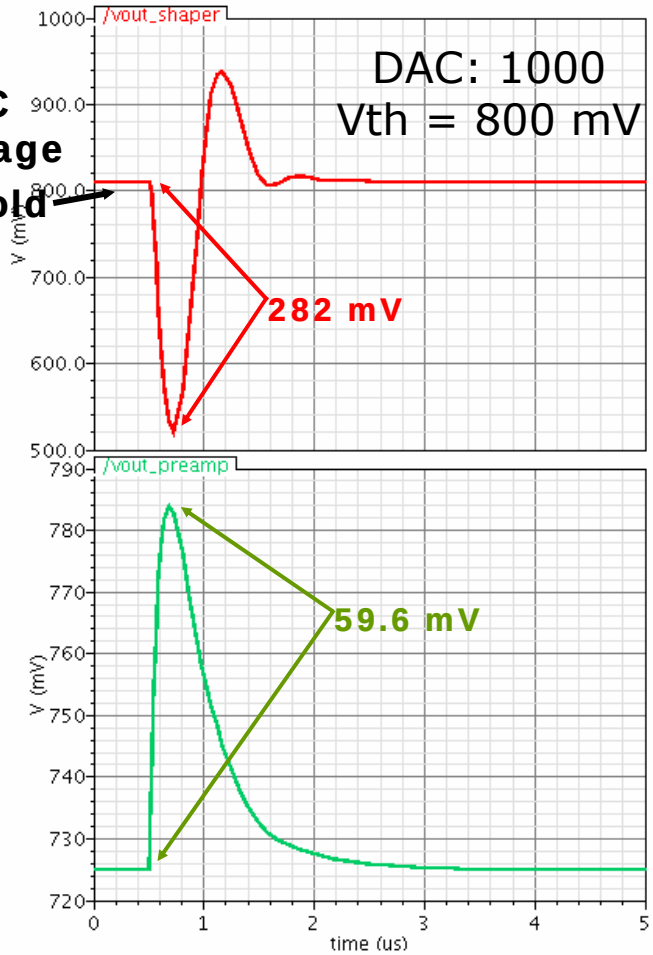
Shaper

DAC fixes the DC shaper output voltage and so the threshold

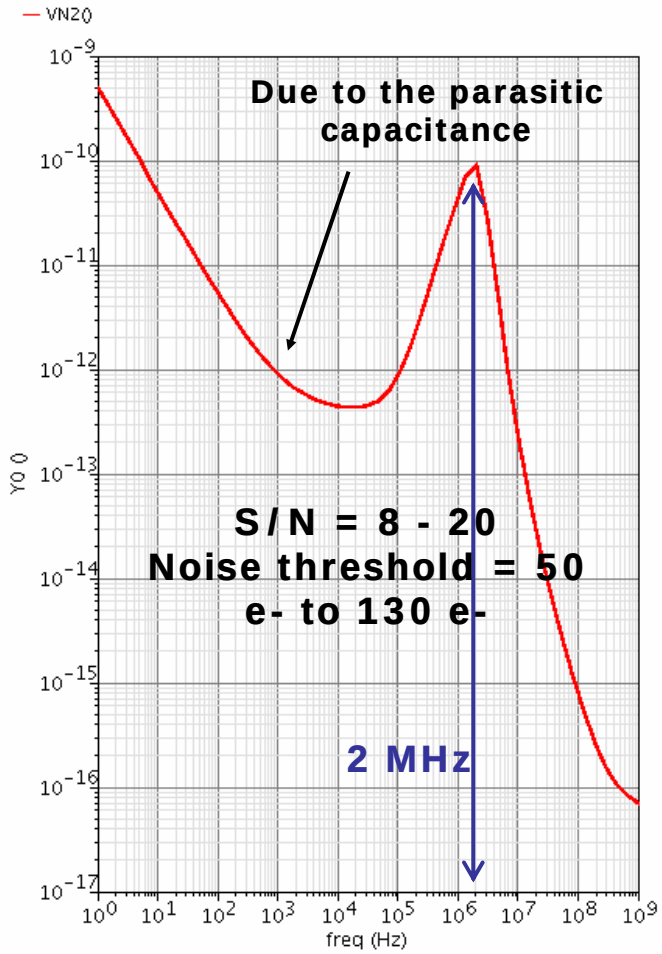
Preamplifier

Vmax = Q/C => 60 mV

Transient response



Noise at the output of the shaper



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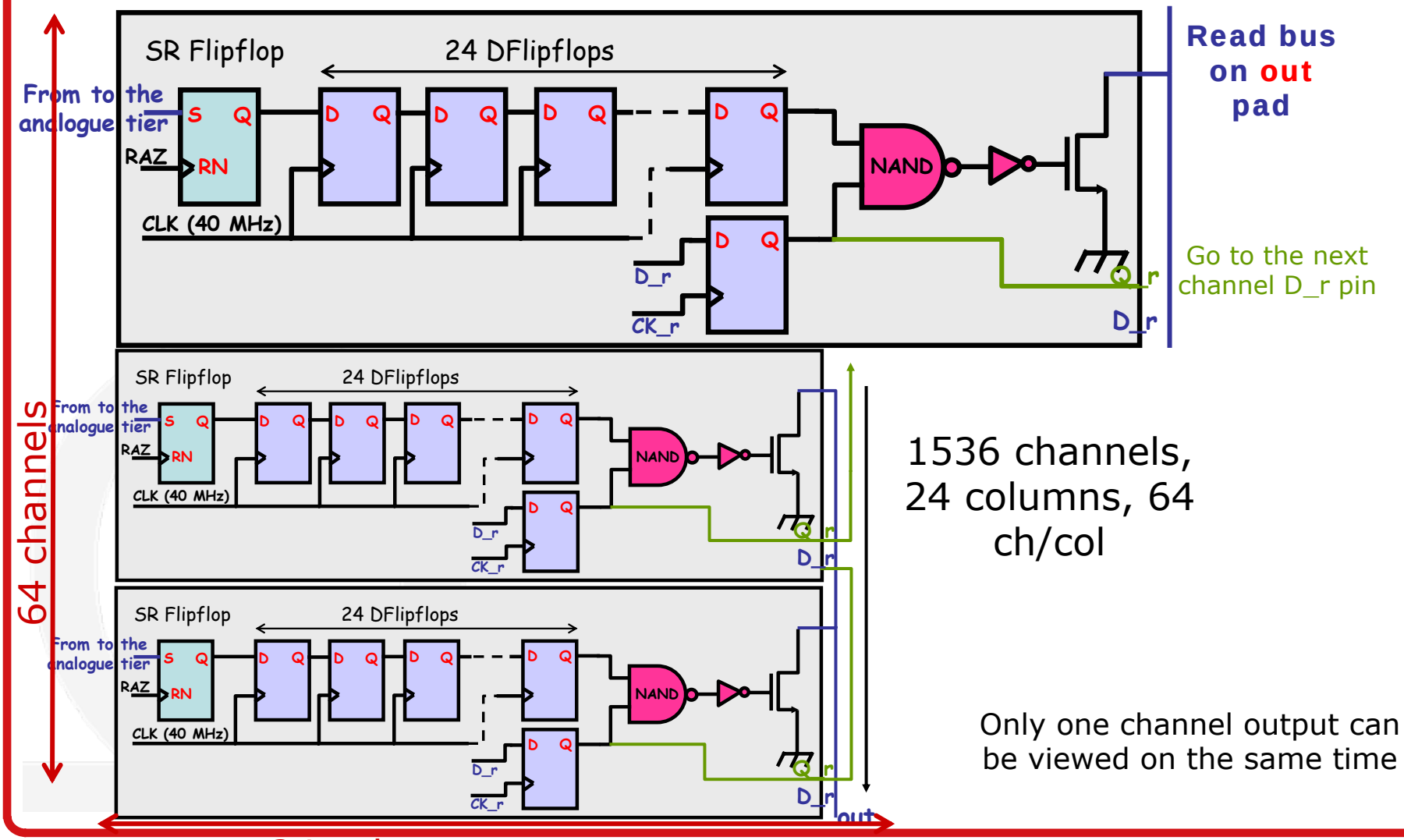
OMEGAPIX: Digital tier

Digital tier has been designed by Yixian Guo from LPNHE.
Each channel includes a 24 DFlipflop register: main tests will focus about the noise study



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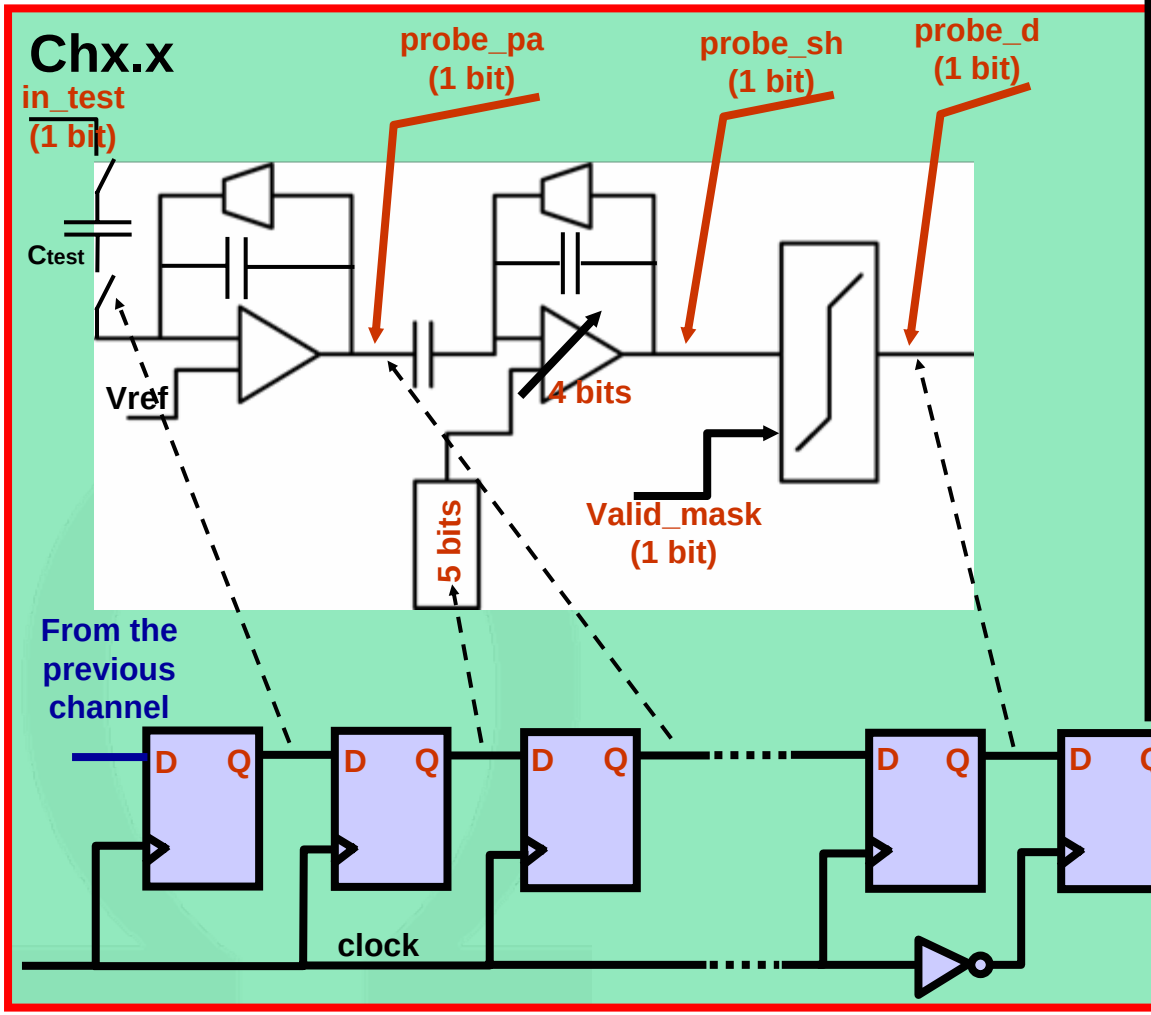
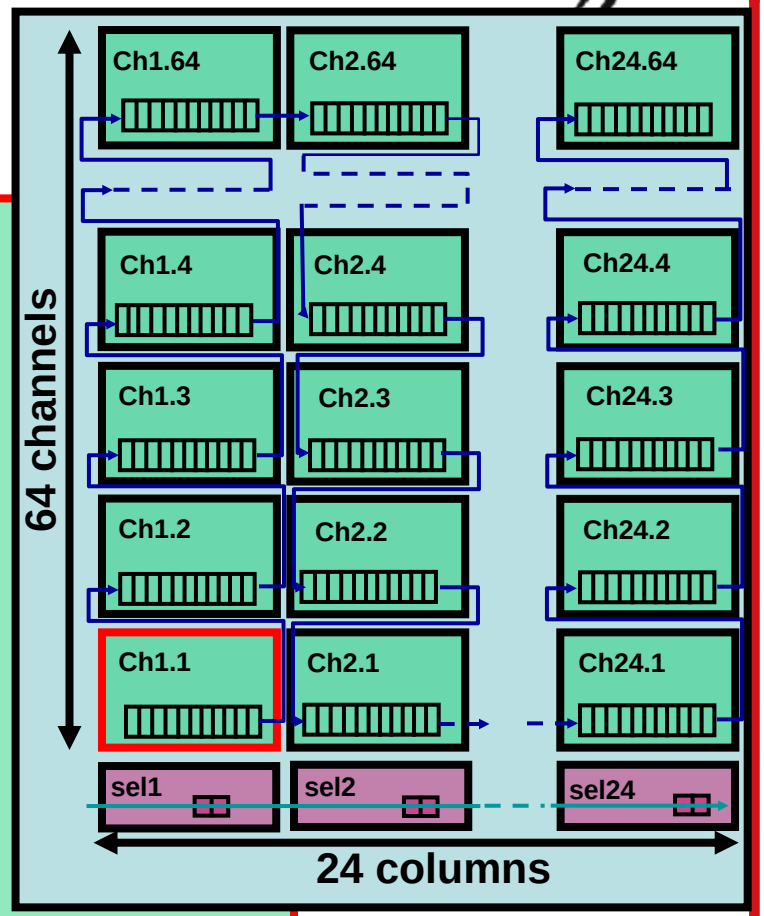
OMEGAPIX: dedicated test chip – Slow Control

24 columns, 64 channels/columns -> 1536 channels
14 SC bits/channel -> 21504 SC bits
2 SC bits/selectColumn -> 48 bits



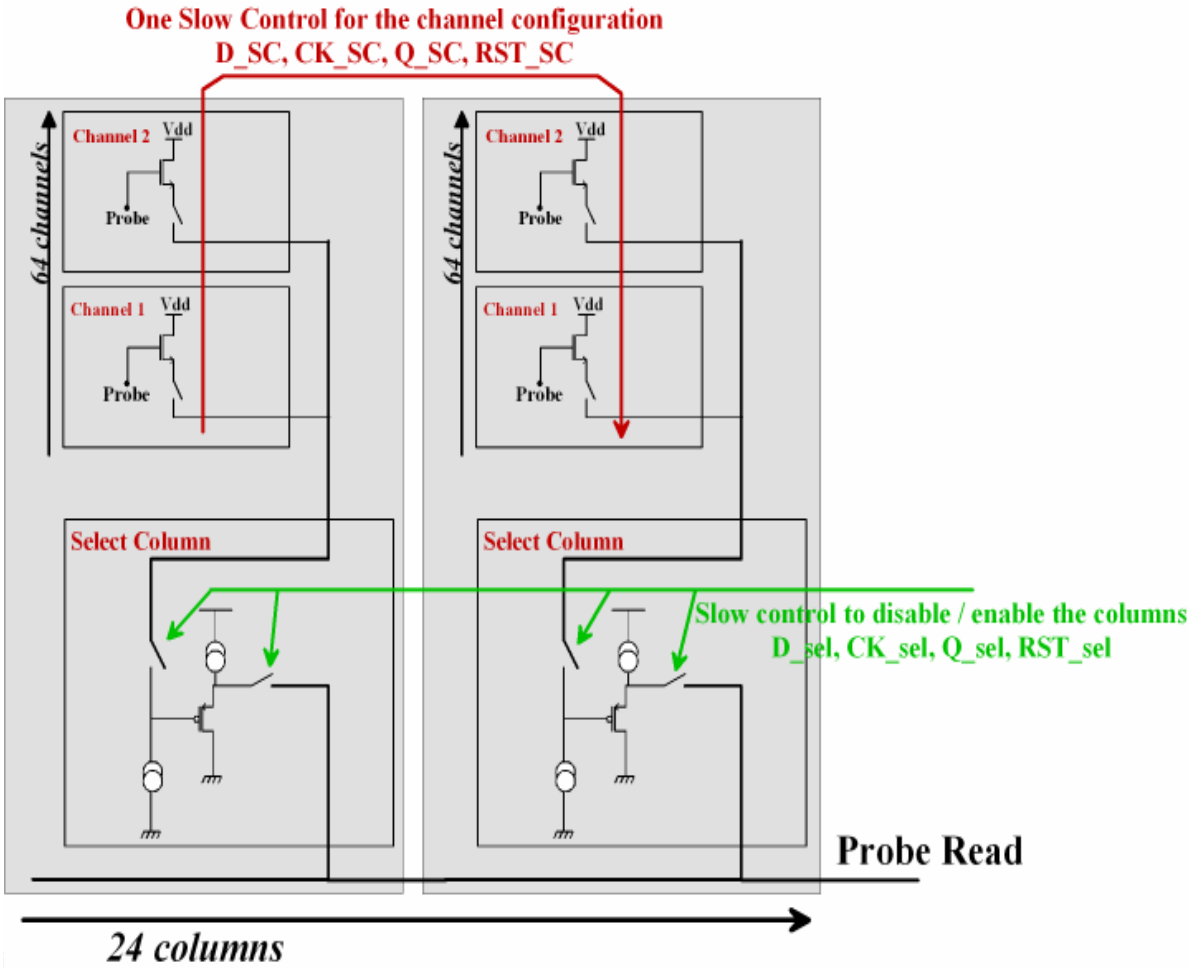


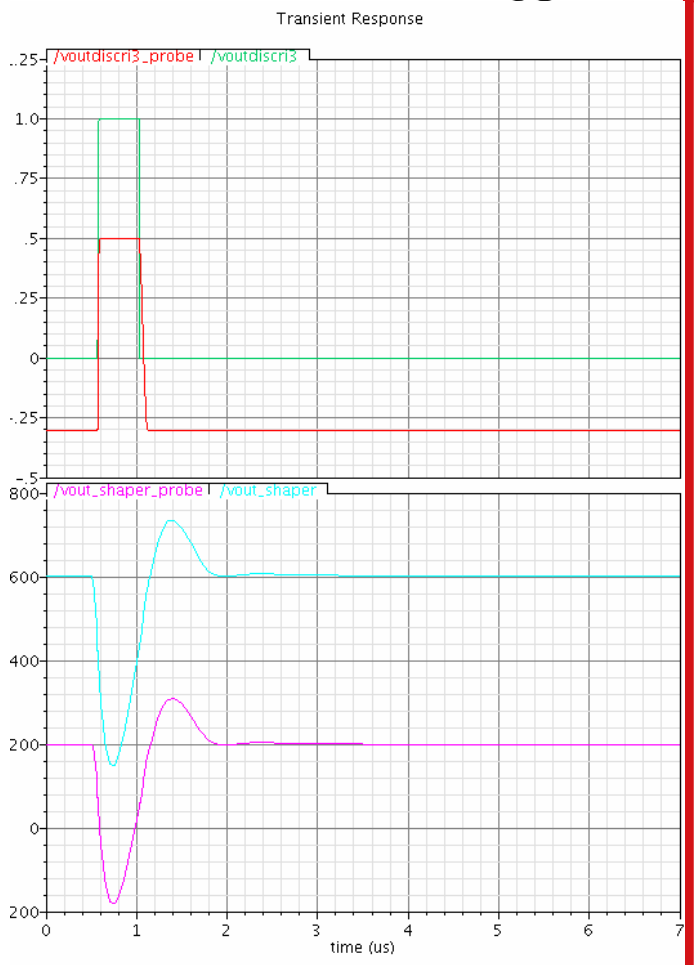
- In_test -> 1 bit
- 3 probes: preamplifier, shaper, discriminator -> 3 bits
- DAC -> 5 bits
- Shaper: variable gain -> 4 bits
- Discriminator: mask -> 1 bit

-> 14 SC bits / channel

OMEGAPIX: dedicated test chip - probes

One channel can be viewed on the same time





OMEGAPIX: different columns

Several column types have been designed allowing us to study various flavours of transistor types (normal, low VT, 3p3), noise, oscillations…

- ✓ Columns 1 to 10: reference channels
- ✓ Columns 11 to 18: various preamplifier transistor types have been integrated
- ✓ Column 19 to 22: without variable gain
- ✓ Column 23: discriminator has been removed
- ✓ Column 24: shaper has been removed

At the first time, the sensor will not be bonded, nevertheless there is the possibility to inject charge via a pad

Some others possibilities are available…

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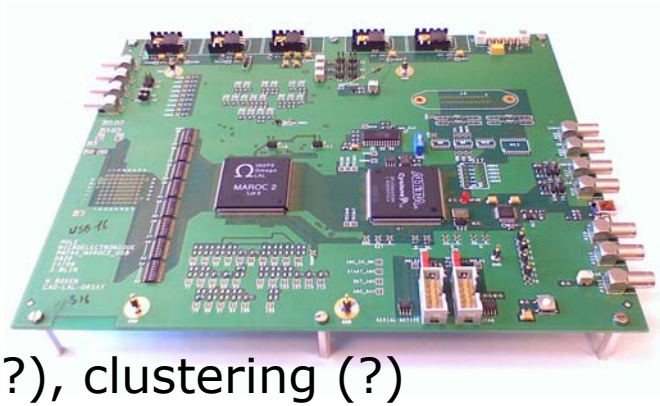
Measurements

✓ Technology characterization: measurements of various transistor types, noise, layers coupling, radiation hardness

✓ At first, tests will be perform without sensor (test board and Software OK), then with the Munich planar pixel prototype (test board to be defined)



Up-coming design

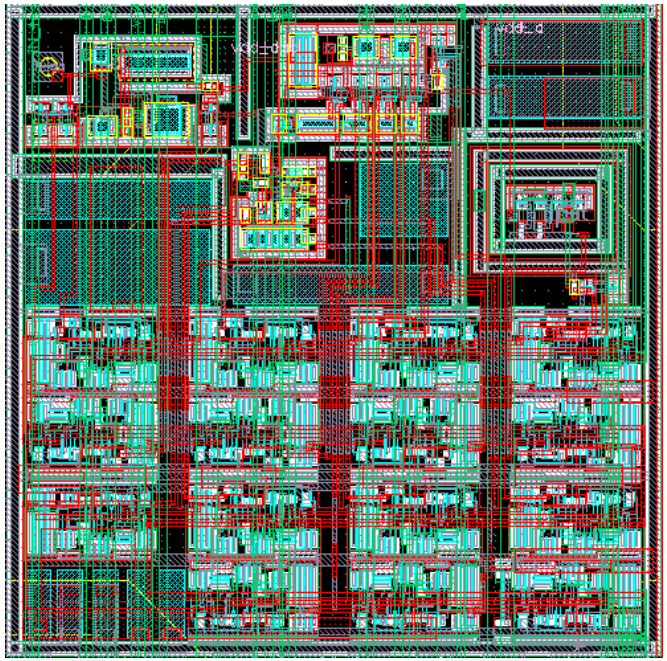
✓ Digital tier with the readout system: TOT (?), clustering (?)

✓ Analogue tier finalization and optimization

Backup Slides

Layout: some pictures…

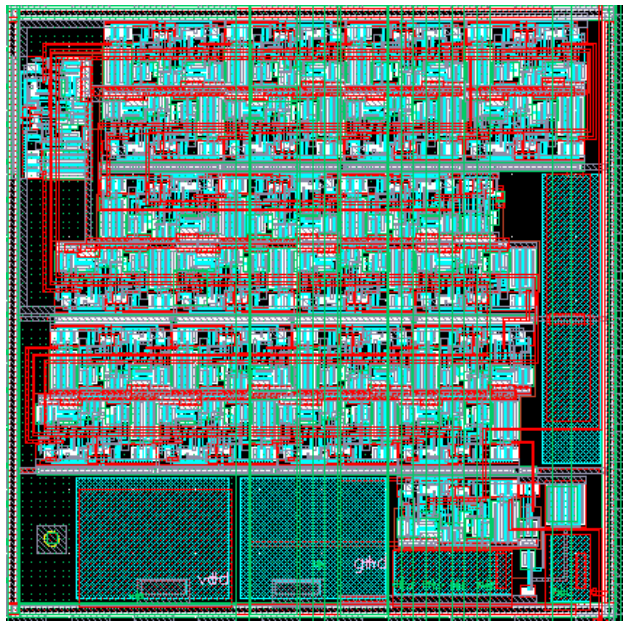
One channel: analogue part



50 µm

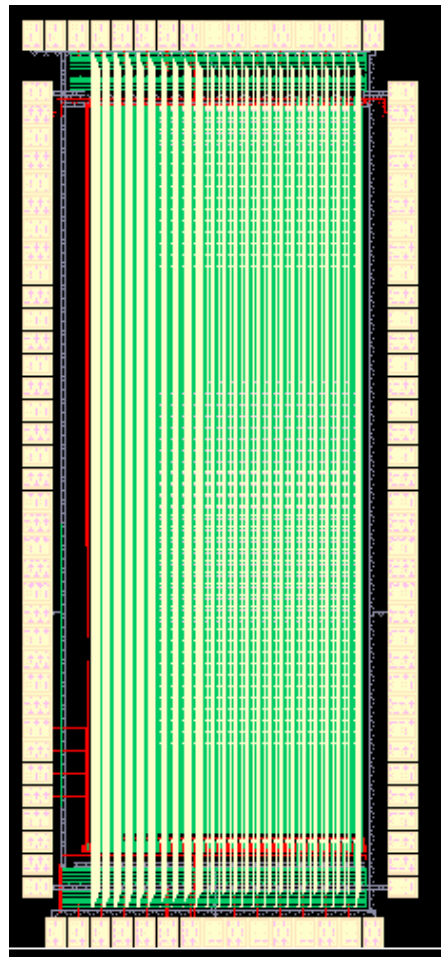
50 µm

One channel: digital part



1,74 mm

4 mm



Entire analogue tier

3D consortium: VITESSE

VITESSE: a new international consortium for development of **V**ertical **I**ntegrated **T**echnologies for **E**lectronics and **S**ilicon **SE**nsors (3D), gathers 15 institutes

- Fermilab (Batavia) and LBNL (Berkeley) in USA
- 6 IN2P3 laboratories (France) in particular LAL Orsay
- 6 Italian institutes
- University of Bonn (Germany)
- AGH University of Science & Technology (Poland)

This chip will be designed with the 3D Tezzaron process with wafers from 0.13 um Chartered Semiconductor

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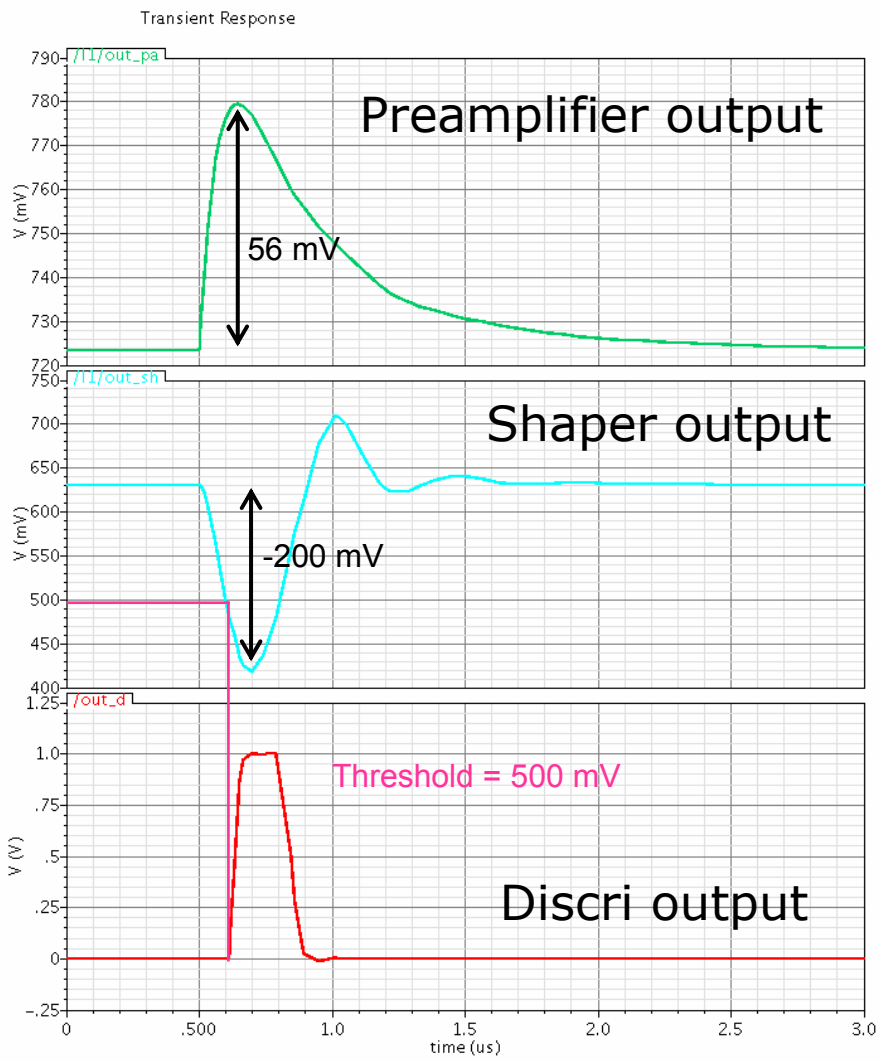
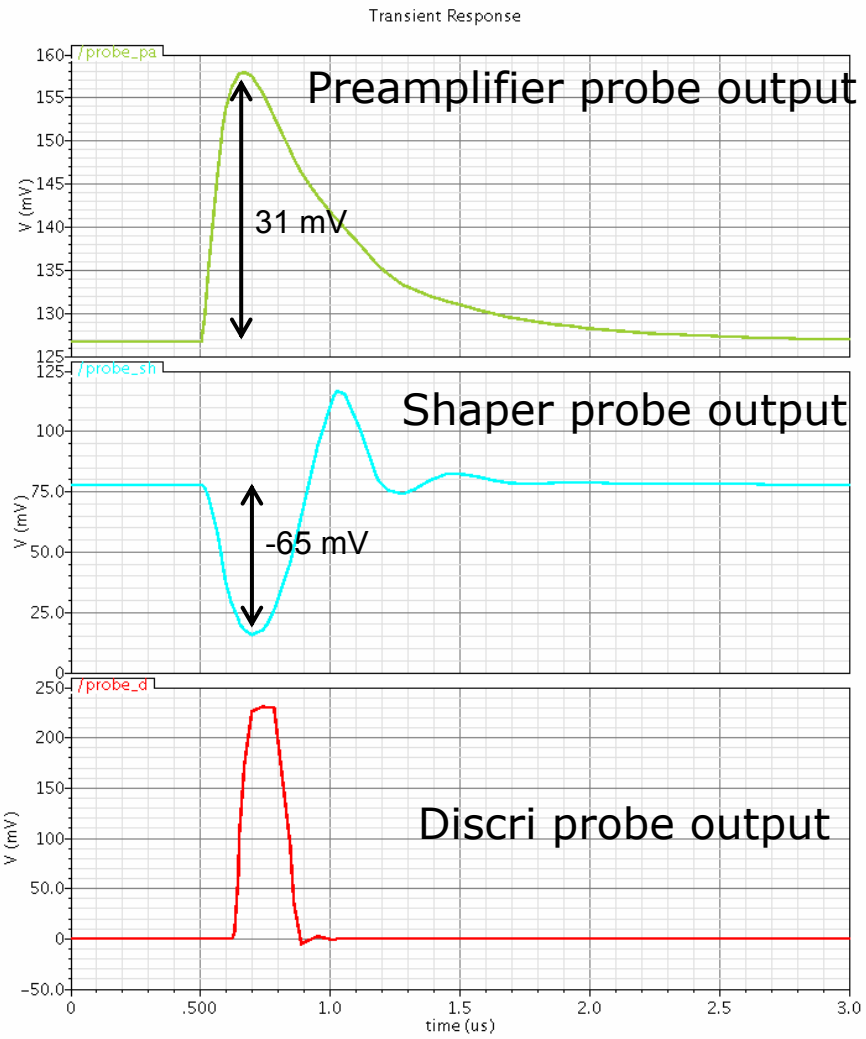
LAL **purpose**: sub-micron readout circuit dedicated for innovative high granular planar pixel sensors for ATLAS upgrade Pixel detector

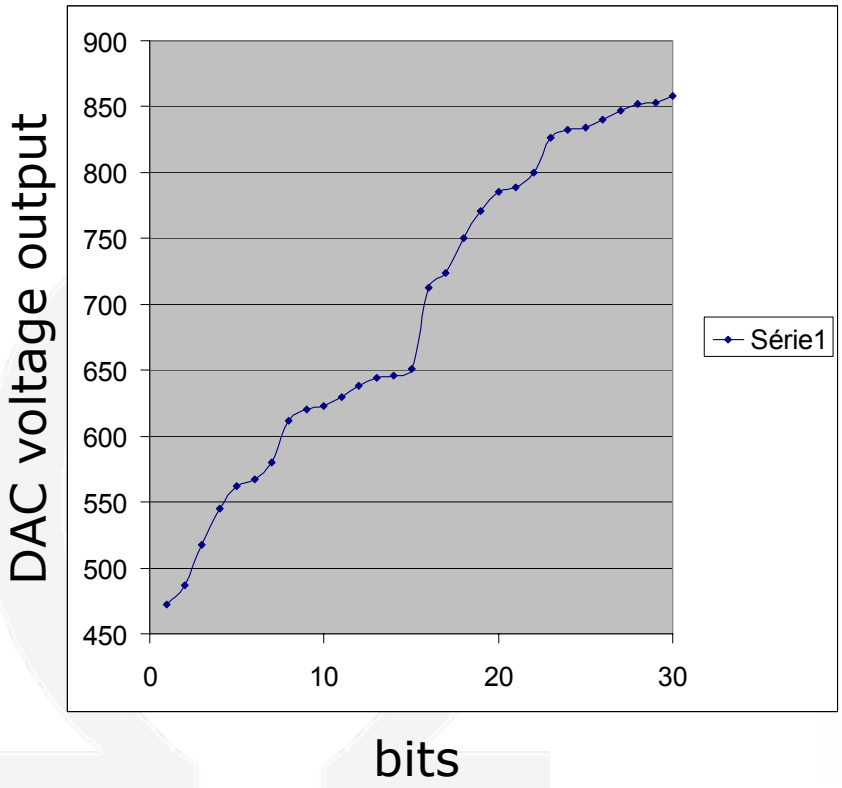
OMEGAPIX: Analogue simulation

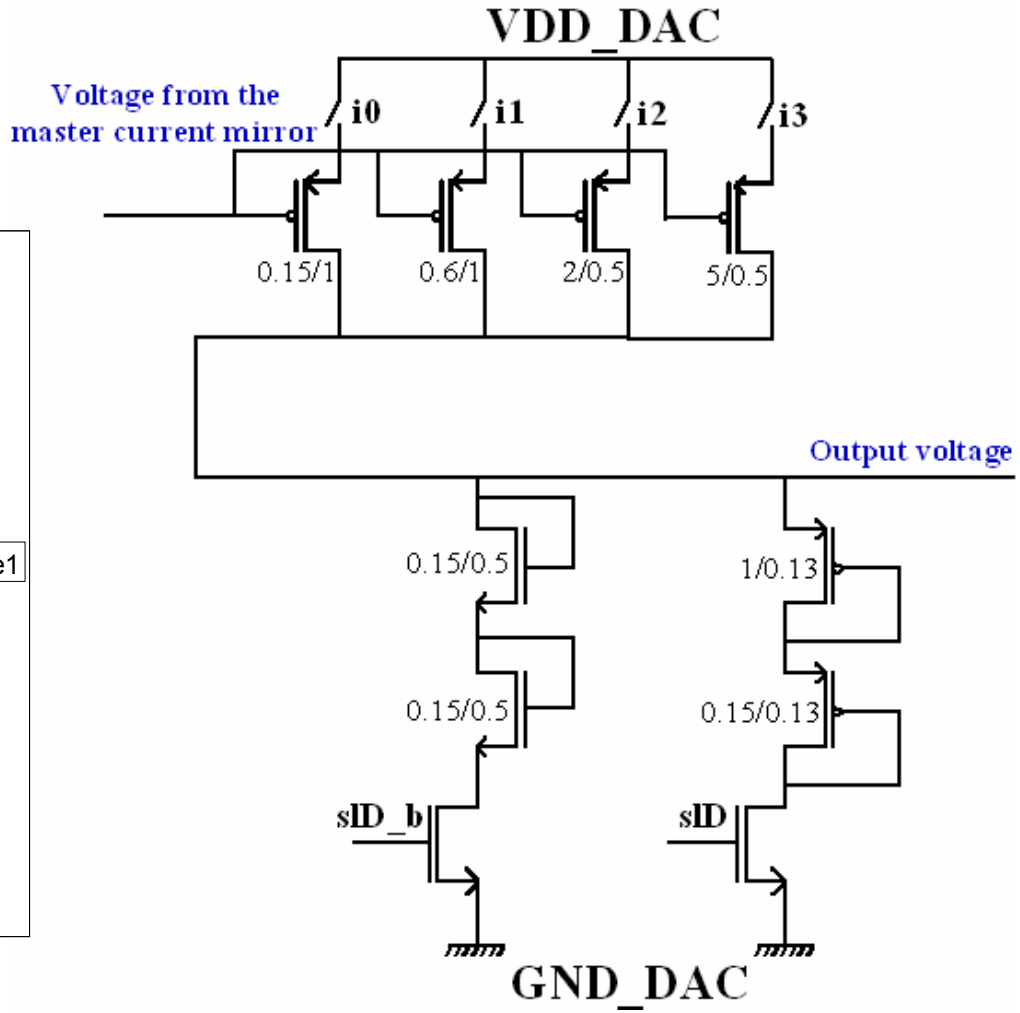
Simulation conditions: Qinj = 1000 e-, Shaper gain = 1000; DAC = slDb, 0001





The DAC fixes the treshold voltage
In fact, only 4.5 bits

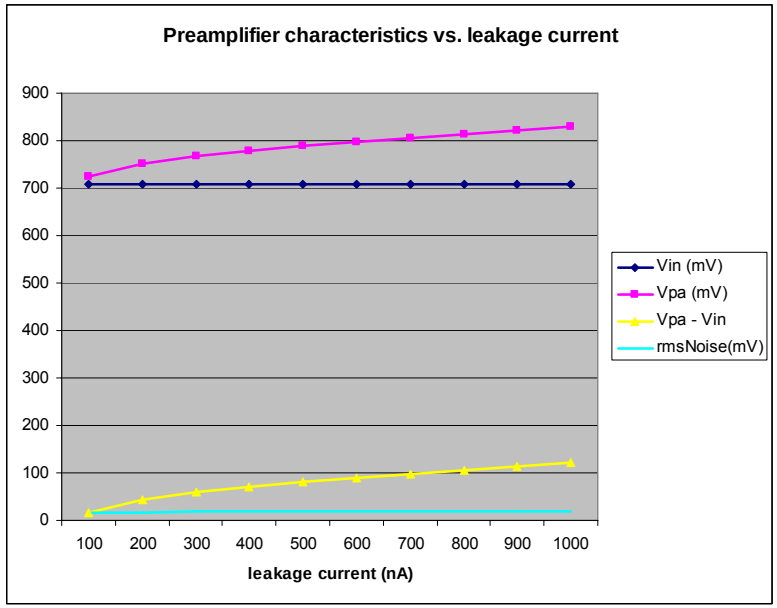




Preamplifier simulation

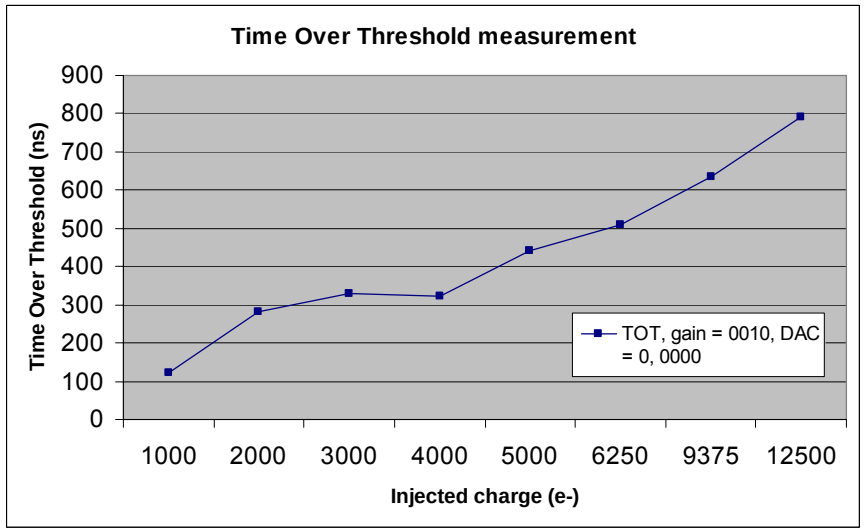
- Paraphase behavior
  - Leakage current variation

    when leakage current increase output preamplifier voltage increase

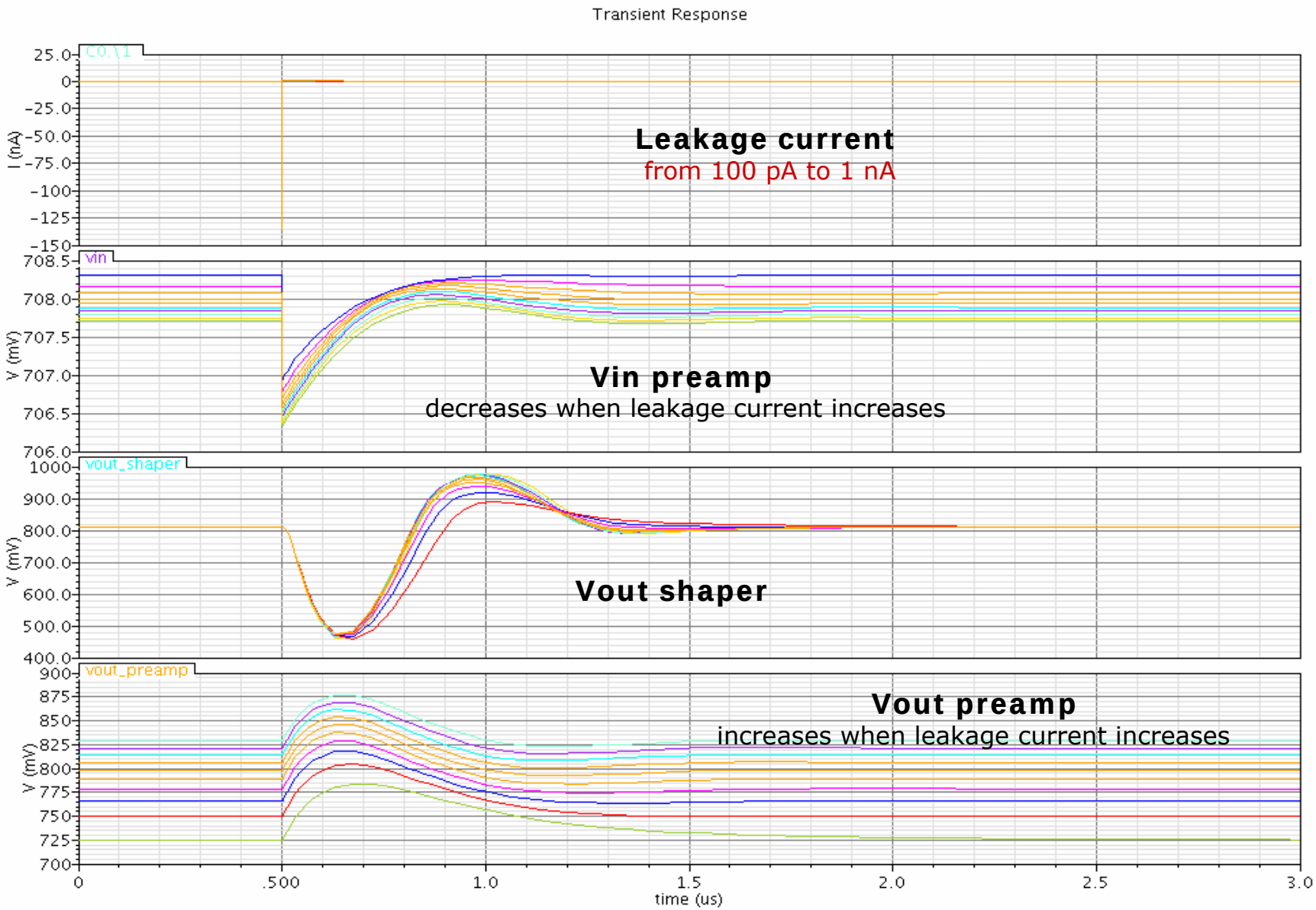


- TOT measurement

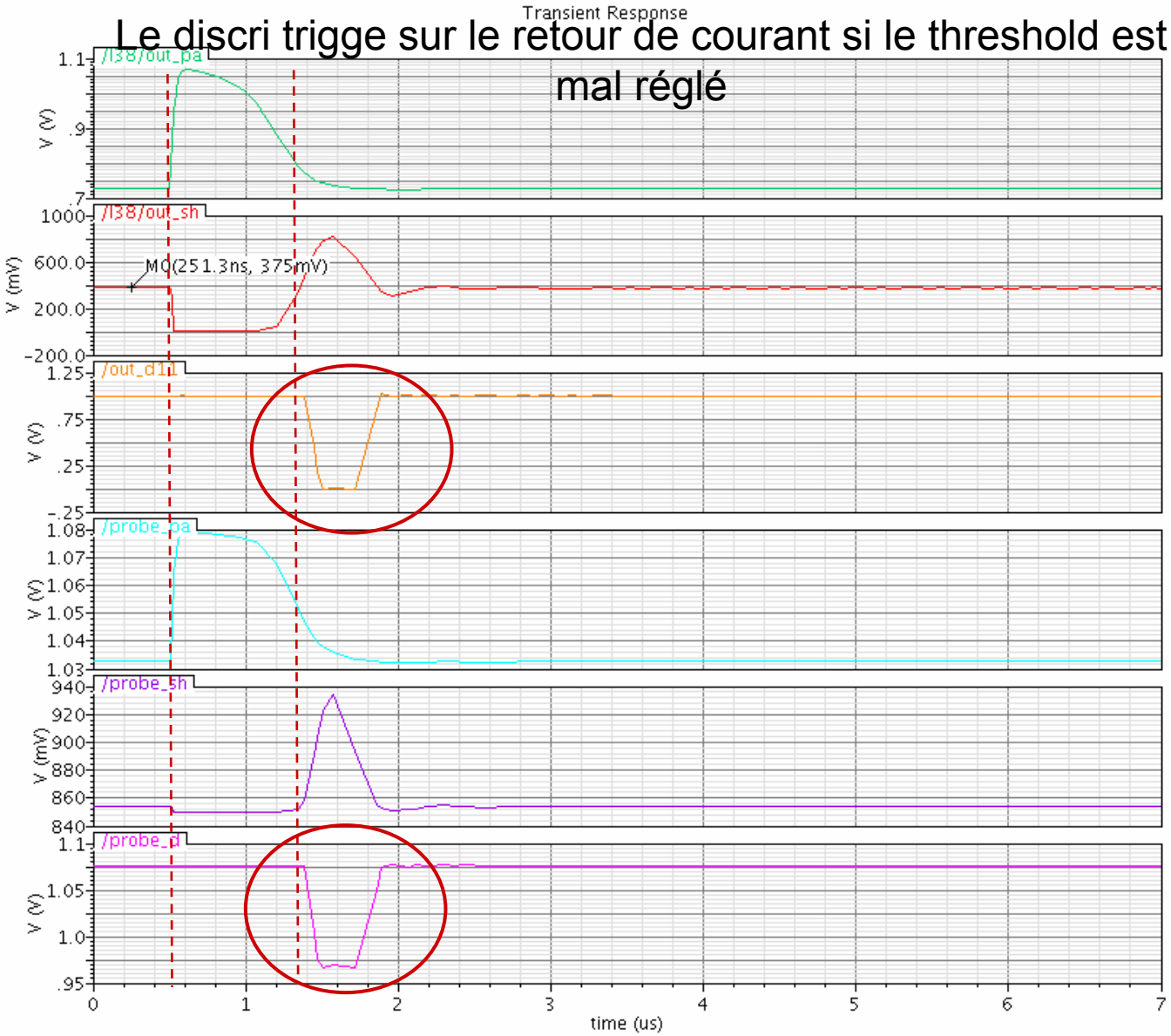
  not very good because of the shaper saturation



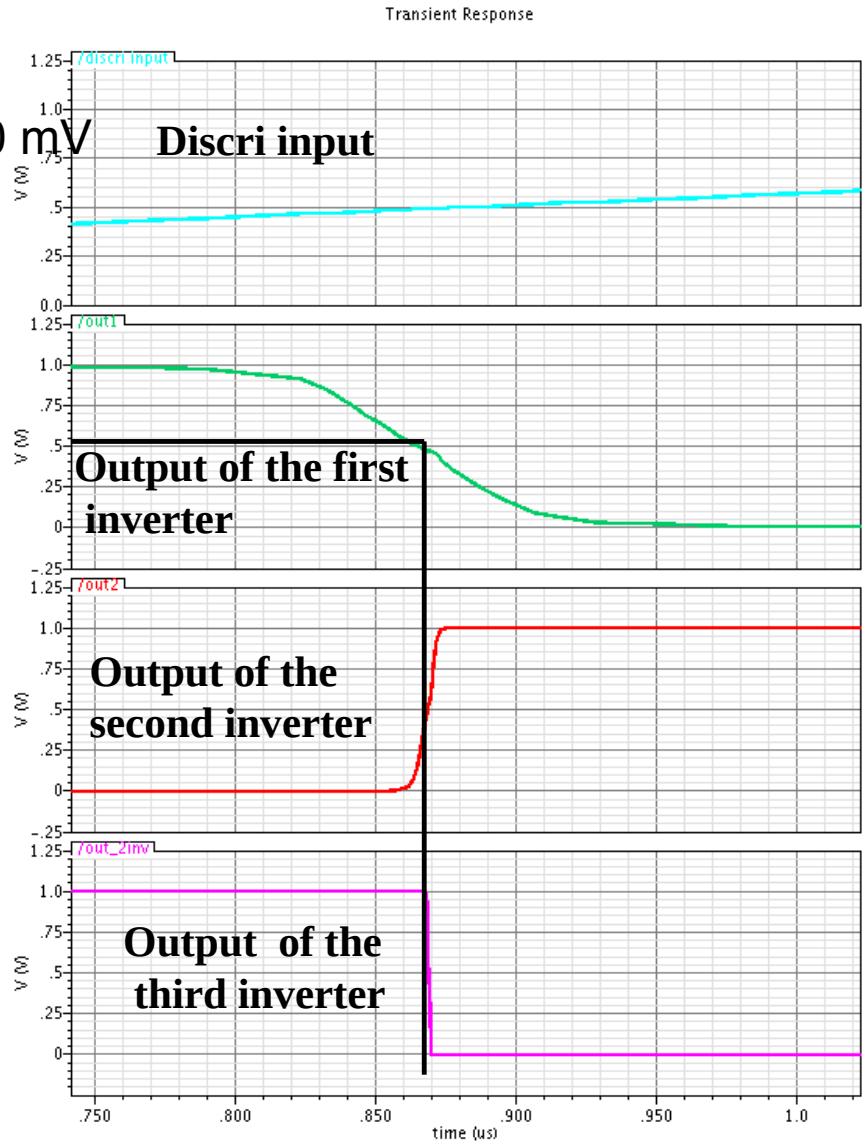
Leakage current variations



Le discri trigge sur le retour de courant si le threshold est mal réglé



Intrinsèque threshold ~ 500 mV



Vthn = 497 mV
Vthp = - 470 mV
VDD = 1 V

Intrinsic threshold = 0.5 mV

Gain preamp et shaper