Ecole IN2P3 de Microélectronique

La Londe-Les-Maures, 12-15 Octobre 2009

Infrastructure for Microelectronics & MEMS

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CMP

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http://cmp.imag.fr

Summary

- Motivation
- CMP short review
- Mixed signals processes from AMS
- Advanced processes from ST
- IPs
- MEMS
- Activity results in 2008
- Cooperation with other services
- What's New in 2009 and 2010 (TSV)
- Conclusion

Motivation

MPC/MPW Infrastructures for Education, Research and Industry

Why?

- to well educate students, who will become good engineers
- to produce good researchers
- to provide small volume production

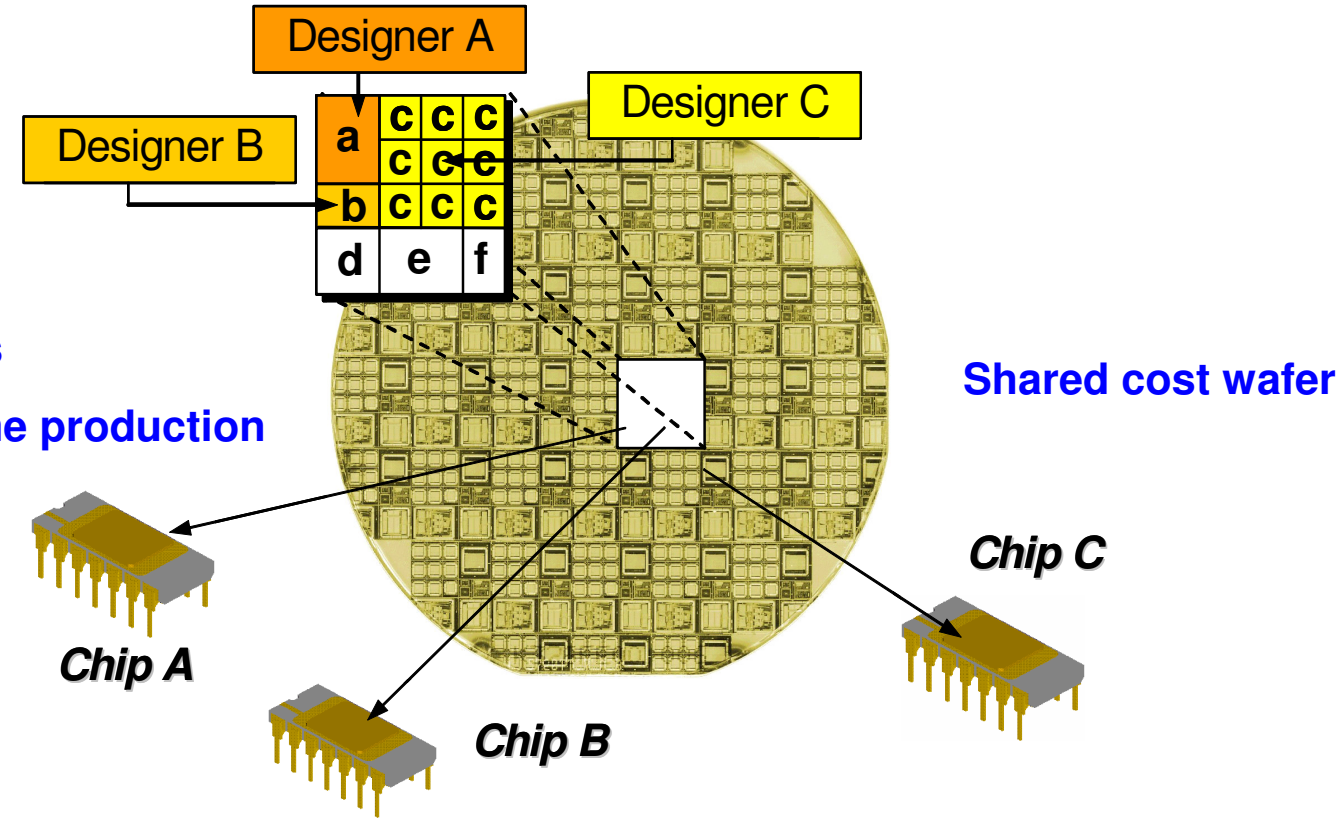
How?

- sharing the wafers, to share the cost
- sharing various needs

Multi-Project Wafer

Multi-Project Wafer runs allow to share the price by sharing the reticle area.

- ❒ **Prototype fabrication.**
- ❒ **Low volume productions (some hundreds to hundred thousands parts)**



Review

- CMP created in 1981
- Offering industrial quality process lines

(University process lines cannot offer a stable yield)

- Design-kits to link CAD and MPW, to facilitate the design.
- Customer base development
  + Universities / Research Labs
  + Industry
  + 1000 Institutions in 70 countries
- Non-profit, Non-sponsored

Technology Portfolio

ICs :	austriamicrosystems	0.35 µ CMOS 0.35 µ SiGe 0.35 µ CMOS-Opto 0.35 µ CMOS HV 0.35 µ CMOS HV EEPROM
	STMicroelectronics	40nm CMOS (New) 65nm CMOS | 65nm SOI 90nm CMOS 130nm CMOS | 130nm SOI 0.25 µ SiGe:C BiCMOS
	OMMIC	0.2 µ GaAs HEMT
MEMS :	CMP / austriamicrosystems	0.8 µ BiCMOS bulk micromachining
	CMP / OMMIC	0.2 µ HEMT bulk micromachining
	CMP / austriamicrosystems	0.35 µ CMOS bulk micromachining (New)
	MEMSCAP	PolyMUMPS | MetalMUMPS | SOI-MUMPS

CAD Tools :	Tanner, ARM , Mentor Graphics, SoftMEMS
IP exploitation :	ARM cores on STMicroelectronics processes (130nm and 65nm)
Design kits :	more than 35 different kits

Packaging :	Ceramic, plastic, custom ...

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Mixed Signals Processes

From 

Processes Portfolio from AMS

0.35µ CMOS : C35B4C3

0.35µ SiGe : S35D4M5

0.35µ CMOS-Opto : C35B4O1

0.35µ CMOS-RF : C35B4M3

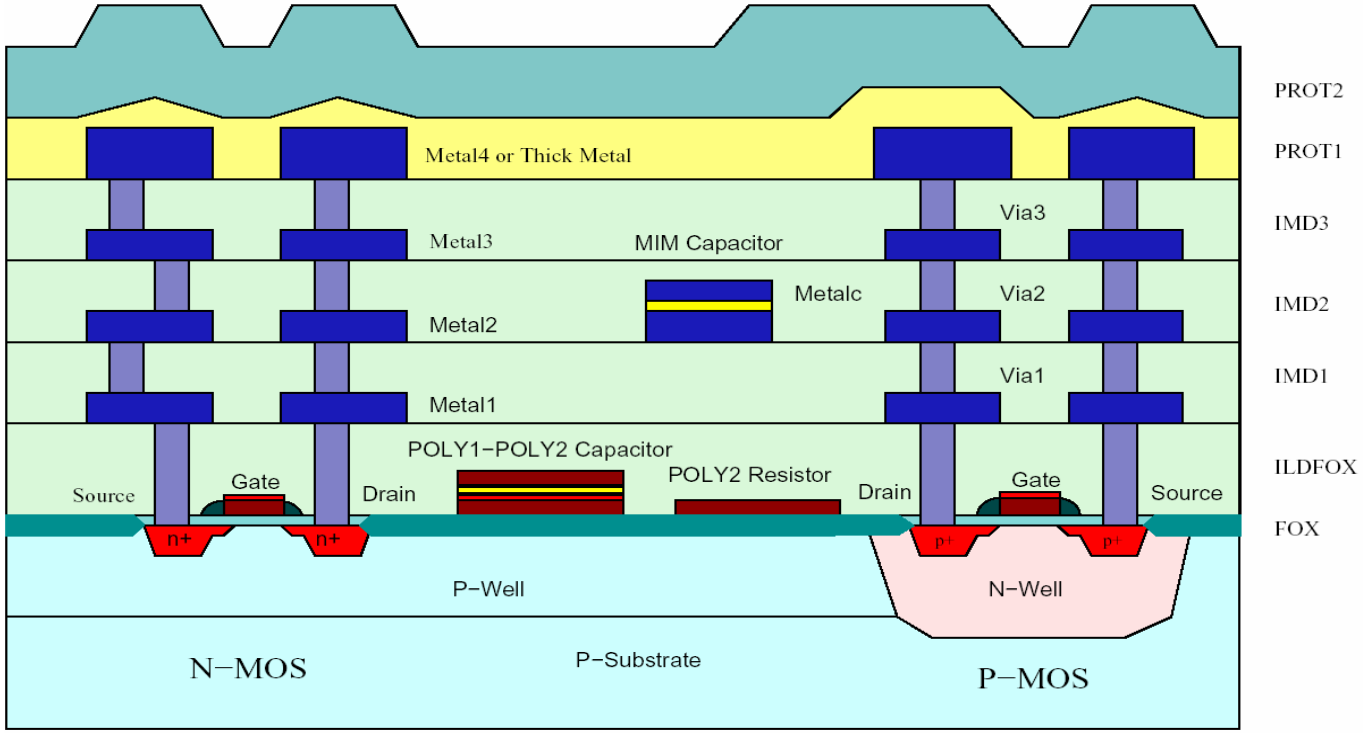
0.35µ HV CMOS : H35B4D3 (120V process module)

0.35µ HV EEPROM : H35B4H3

0.8µ BiCMOS : BYE / BYQ

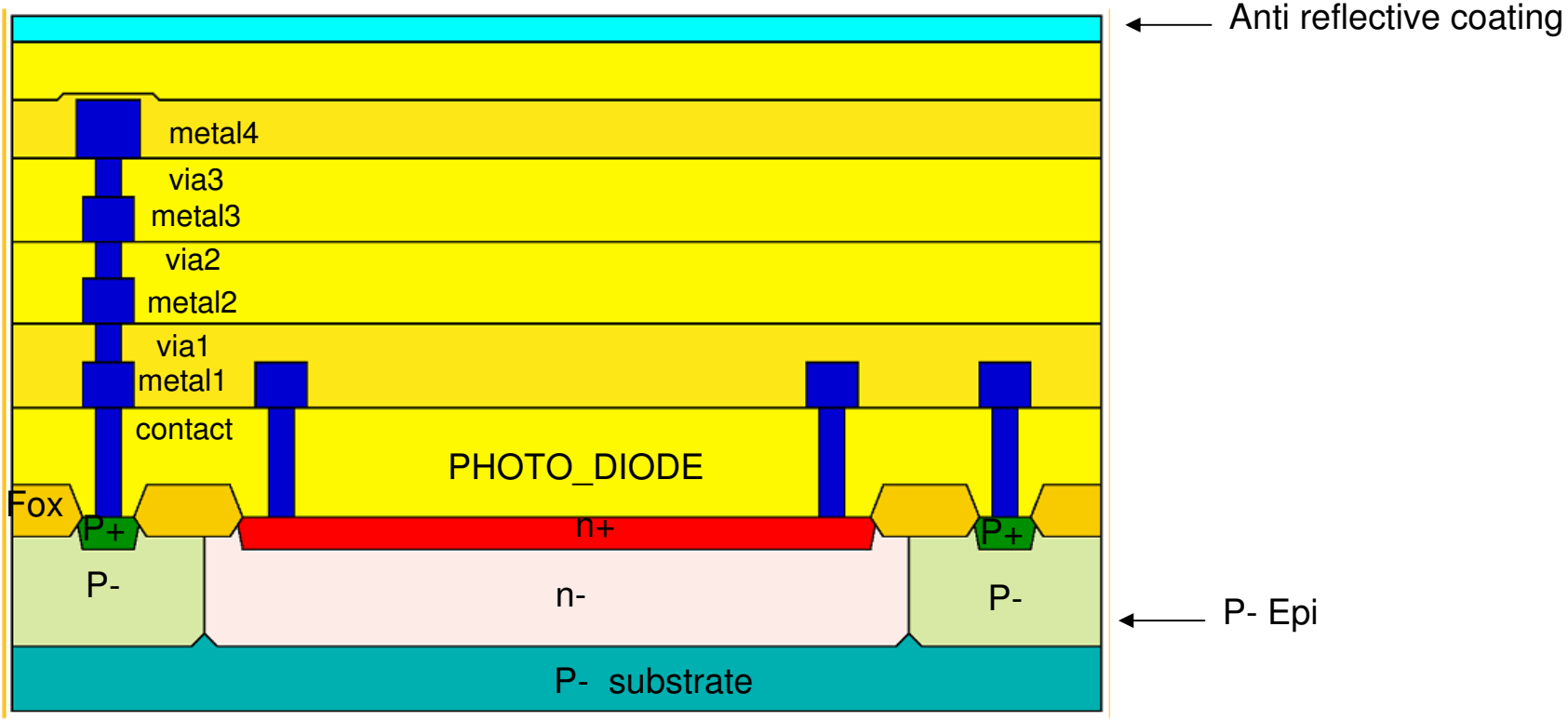
CMOS 0.35 µ C35 (C35B4C3)

- 2 Levels Polysilicon, 4 Levels Metal, 3.3V / 5.0V, High Resistive Poly.
- 3.3V / 5.0V I/O pads.
- Peripheral cells with high driving capability (from 1mA to 24mA)
- Application : Analog, Digital, Mixed A/D, RF.
- Density : 18 kgates/mm^2
- Gate Delay: 100ps (NAND2 typical)
- Libraries : Digital and Analog Standard Cells + Pads + SPIRAL Ind. + P-Cells.



CMOS-Opto 0.35 µ (C35B4O1)

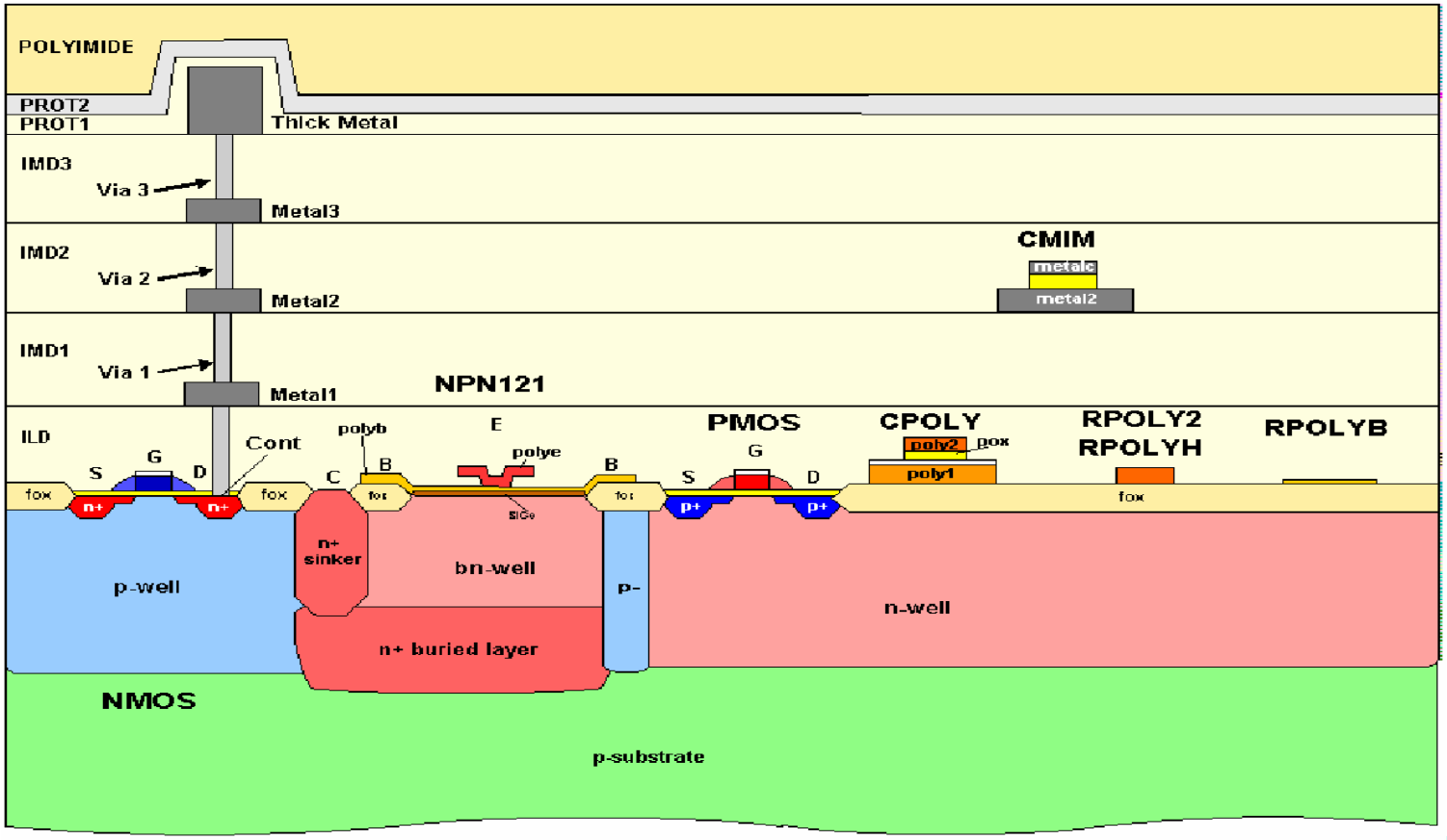
- **Planarization and anti-reflective coating allows much better optical properties than the standard CMOS.**
- **P-Epi wafers allow lower current leakage in the diode. Lower dark current.**



C35-Opto Process Cross-Section

SiGe HBT-BiCMOS 0.35 µ S35

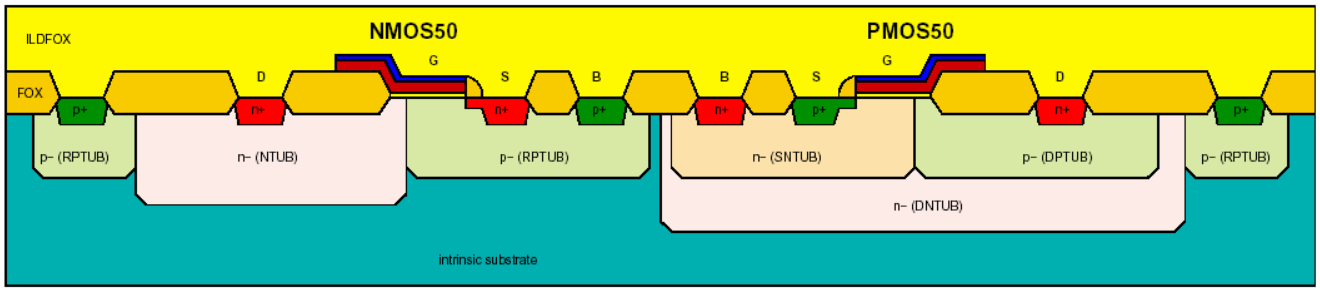
- 4 Layers Polysilicon / 4 Layers Metal.
- Power supply voltage range (2.5V – 3.6V / 5.5V)
- Vertical SiGe-HBT NPN : Ft = 70 GHz
- High Resistive Polysilicon.
- High precision Poly1/Poly2 capacitors
- High precision MIM capacitors and Thick Top Metal



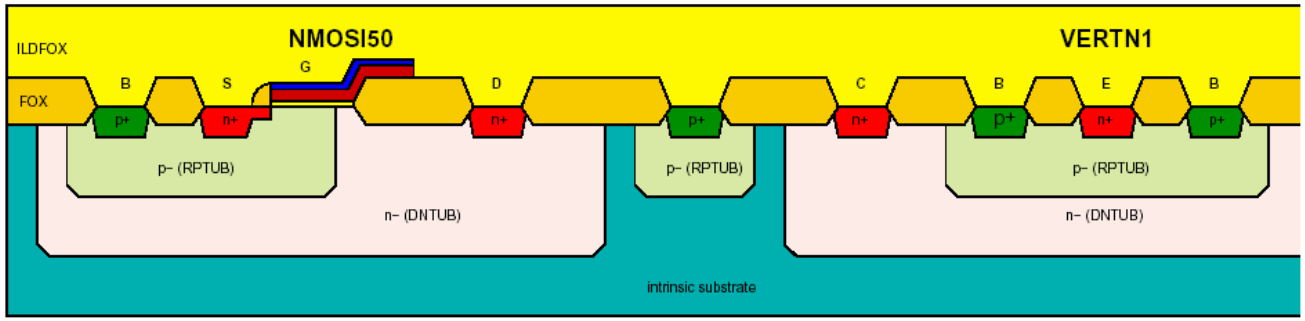
HV CMOS 0.35 µ H35 (H35B4D3)

- 2 Layers Polysilicon, 4 Layers Metal, High Resistive Poly, Thick 4th Metal.
- 50 Volts Maximum operating voltage.
- 3.3V / 5.0V / 20V Maximum gate voltage.
- R_{on} = 0.11 Ohm mm^2 for HV-NMOS
- R_{on} = 0.29 Ohm mm^2 for HV-PMOS

NMOS50 and PMOS50 transistors



NMOSI50 and VERTN1 transistors



austriamicrosystems Runs in 2008

Number of prototypes in 2008 : **176** (171 in 2007)
Number of Low volume prod. in 2008 : **35** (32 in 2007)

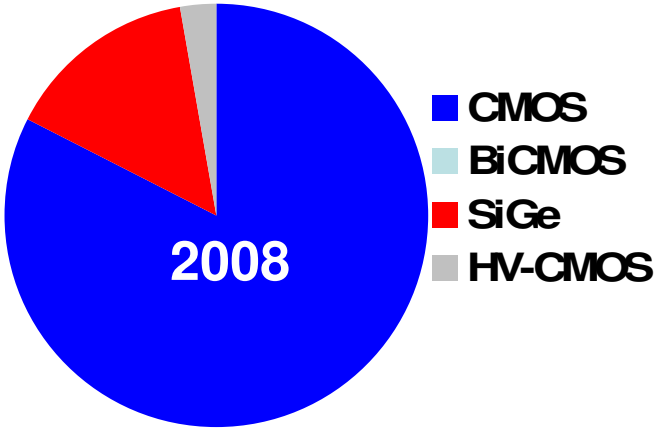
30 scheduled MPW runs (29 in 2007)
5 extra runs (Production) (5 in 2007)

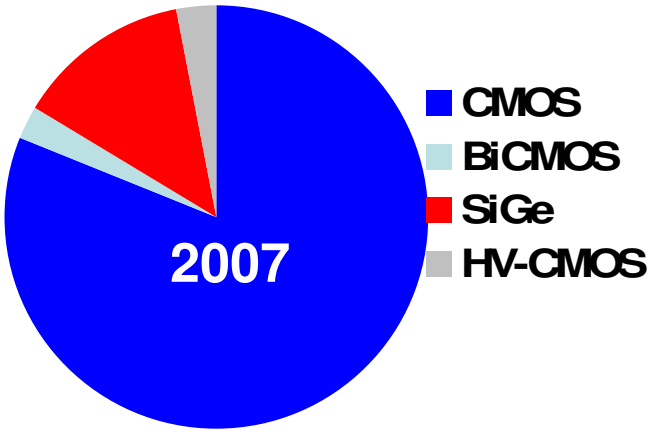
145 circuits CMOS 82% (81% in 2007)
(138 in 2007)

0 circuits BiCMOS 0% (2% in 2007)
(4 in 2007)

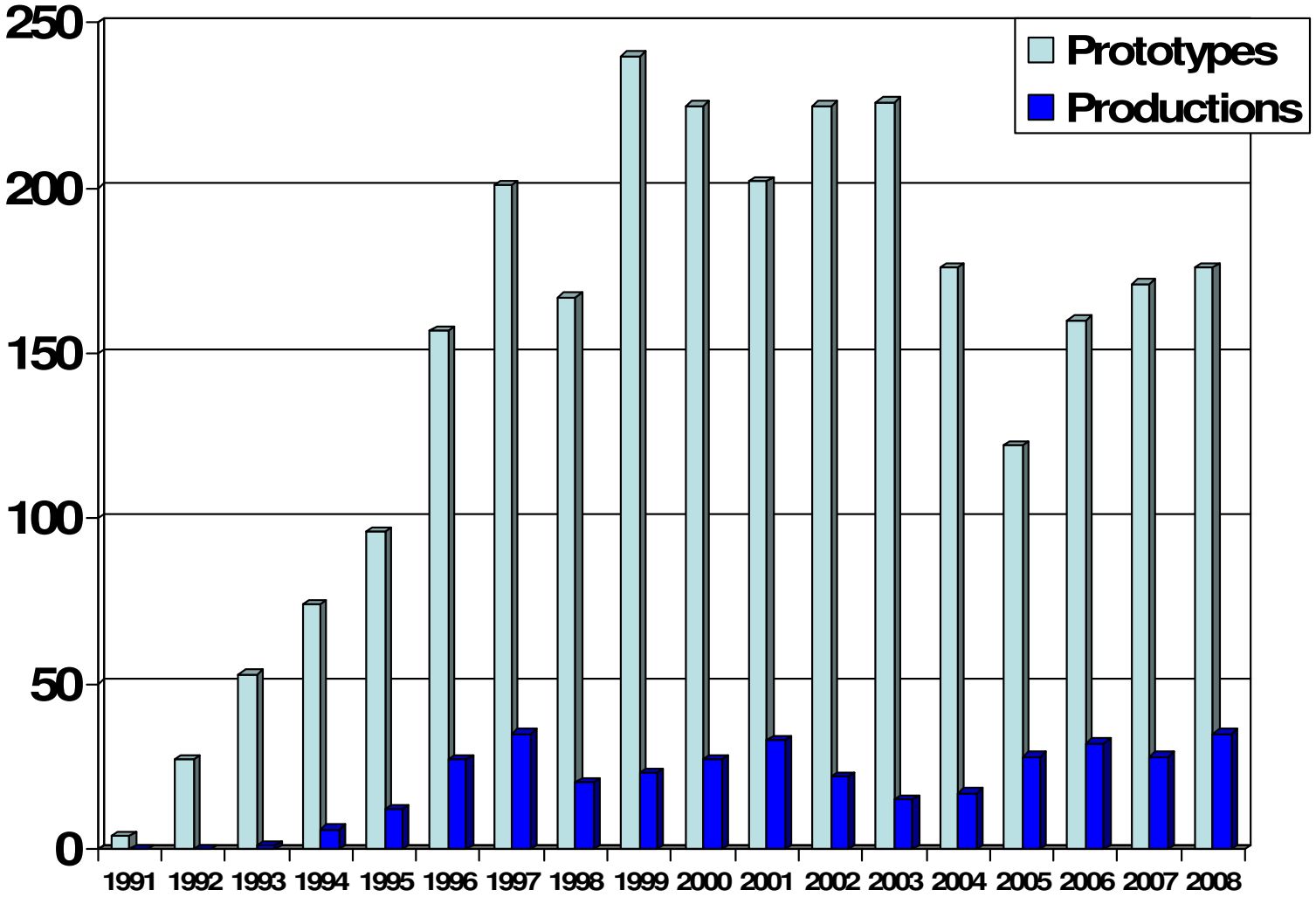
26 circuits SiGe 15% (13% in 2007)
(23 in 2007)

5 circuits HV-CMOS 3% (3% in 2007)
(5 in 2007)





Nbr of Circuits histogram



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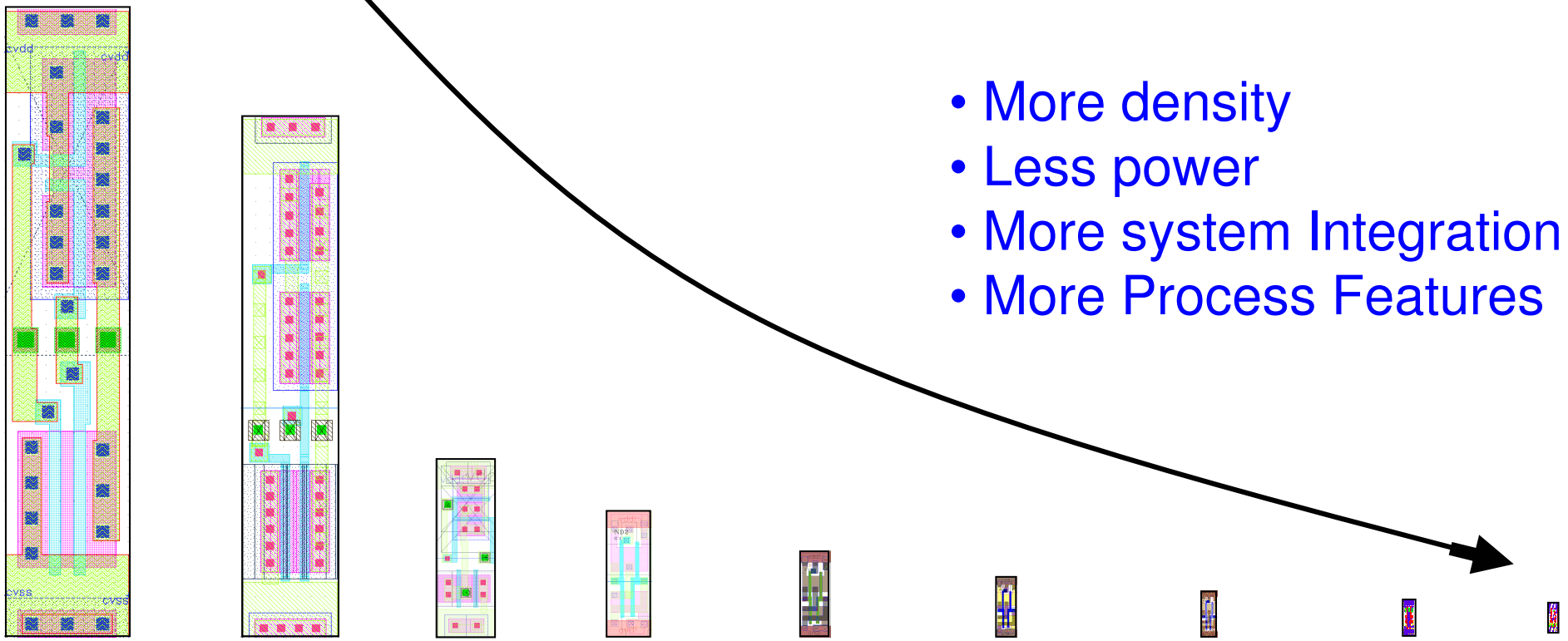
Avanced Processes From

CMP's Process Roadmap



- More density
- Less power
- More system Integration
- More Process Features

AMS 0.8µ 1.2k gates/mm²

AMS 0.6µ 3k gates/mm²

AMS 0.35µ 18k gates/mm²

ST 0.25µ 35k gates/mm²

ST 0.18µ 80k gates/mm²

ST 0.12µ 180k gates/mm²

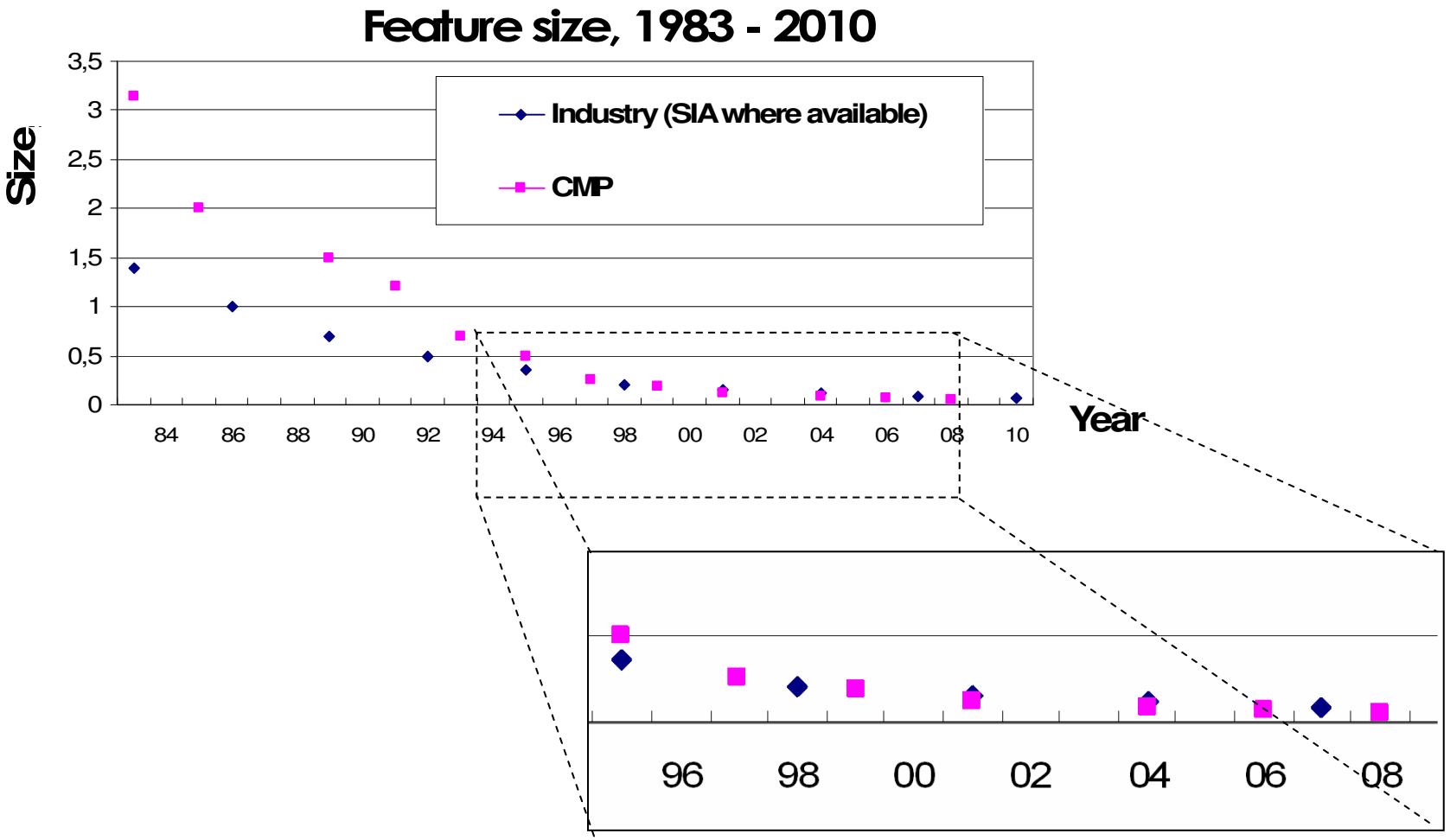
ST 90nm 400k gates/mm²

ST 65nm 800k gates/mm²

ST 45nm 1.6M gates/mm²

1994 at CMP → **2008 at CMP**

Process Roadmap



Process Portfolio from ST

Moore's Law	More than Moore
130nm CMOS : HCMOS9GP	0.25µ SiGe : BICMOS7RF ← STOPPED
90nm CMOS : CMOS090 ← STOPPED	130nm SiGe : BICMOS9MW New
65nm CMOS : CMOS065	65nm SOI : CMOS065-SOI
45nm CMOS : CMOS045 ← STOPPED	130nm SOI : HCMOS9-SOI
40nm CMOS : CMOS040LP New	

90nm designs fabricated in 2007

- **86** designs **(+85%)** have been fabricated in 90nm CMOS in **2007**.
- From **22** customers :

North America (10)

- University of Virginia
- University of Washington
- MIT
- CMC*
- Stanford University
- UCLA
- BWRC
- University of Michigan
- Georgia Institute of Technology
- University of Texas at Dallas

Europe (12)

- ISEN Lille
- Instituto Microelectronica Sevilla (IMSE)
- Linköping University - ISY
- University of Modena and reggio emilia
- NORWEGIAN UNIV., SCIENCE & Tech
- UNIVERSTY OF OSLO
- University of Parma
- University of Perugia
- University of Turku
- University of Pisa
- VTT Information Tech.
- Novelda AS

(*) 18 Canadian Universities

90nm designs fabricated in 2008

- **160** customers received design rules, design-kits
- **67** designs have been fabricated in 90nm CMOS in **2008**.
- From **22** customers :

North America (6)

- MIT
- CMC*
- BWRC
- University of Michigan
- Georgia Institute of Technology
- Univ. Texas, Dallas

(*) 18 Canadian Universities

Asia (2)

- University of Philippines
- University of Macau

Europe (14)

- CERN
- Instituto Microelectronica Sevilla (IMSE)
- Linköping University - ISY
- University of Modena and reggio emilia
- NORWEGIAN UNIV., SCIENCE & Tech
- University of OSLO
- Novelda AS
- Politecnico di Milano
- RWTH Aachen
- THALES (110 mm^2)
- University of Turku
- University of Pisa
- University of Paderborn
- University of Stuttgart

65nm designs fabricated in 2007

- **23** designs have been fabricated in 65nm CMOS in **2007**.
- From **9** customers :

North America (4)
7 designs

- CMC* (4)
- BWRC (1)
- Georgia Institute of Technology (1)
- University of California, Davis (1)

(*) 13 Canadian Universities

Europe (5)
16 designs

- IMS-Bordeaux (7)
- ISEN Lille(1)
- ENST (1)
- LAAS (1)
- LETI / CEA Grenoble (6)

65nm designs fabricated in 2008

- **140** customers received design rules, design-kits
- **32** designs have been fabricated in 65nm CMOS in **2008**.
- From **16** customers :

North America (5)

- CMC*
- BWRC
- University of Michigan
- University of Minnesota
- University of Virginia

(*) 15 Canadian Universities

Europe (9)

- IMS-Bordeaux
- ISEN Lille
- ENST
- KU-Leuven
- LAAS
- LETI / CEA Grenoble
- Politecnico di Milano
- UPC Catalunya
- University of Stuttgart

Asia (1)

Nanyang Tech. Univ. (Singapore)

Africa (1)

Univ. Of Pretoria (South Africa)

The more complex design ever fabricated through CMP

A 55 million transistor many-core chip made on ST's 65nm CMOS, Courtesey of B.BAAS et al, University of California, Davis

- STMicroelectronics 65nm CMOS
- 40 mm^2
- BGA 304 pins
- Ultra fine pitch bonding (pad openings 34 micron)
- First Functional tests successful

Summary of Advanced Processes Fabrications

130 nm 2001 : 285 ICs to date

90 nm 2004 : 180 ICs to date

65 nm 2006 : 85 ICs to date

45nm 2008 : 3 ICs to date

Total: about 550 ICs to date

IP Portfolio

- Design-kits come with core & IO standard libraries
- Memory blocs available free of charge (RAM, ROM, DPRAM, ...)
- High speed IOs (LVDS, ...) may be available on request
- PLL / DLL available on request
- ARM IP cores from ST available free of charge for Universities and Research.
- ARM 946EJ-S available in 130nm CMOS
- All ARM IP cores (7, 9, 11) are available in 65nm CMOS
- Analog library from Autriamicrosystems available with license fees.

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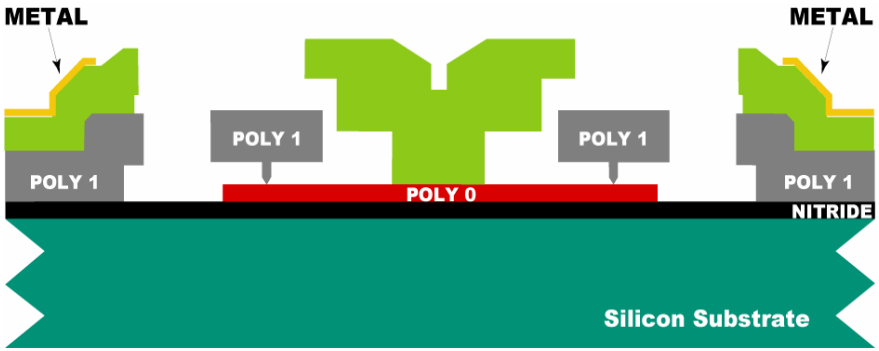
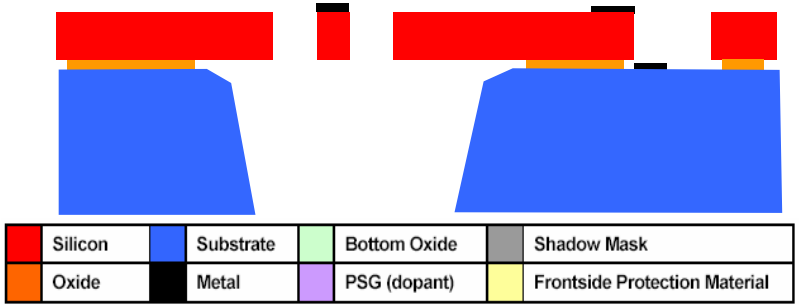
MEMS

MEMSCAP Processes

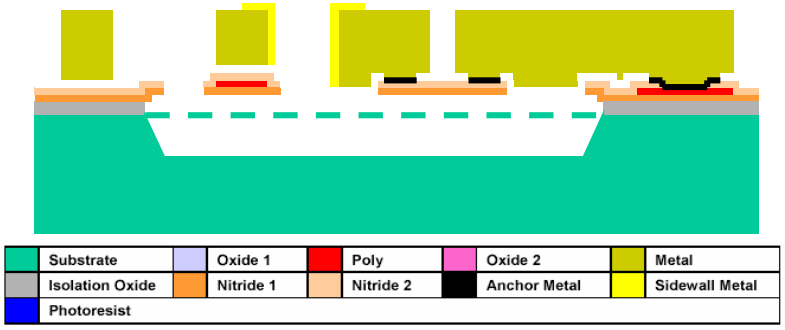
- **PolyMUMPs**
  - 8 lithography levels, 7 physical layers
  - 3 Poly Layers
  - 1 Metal Layer



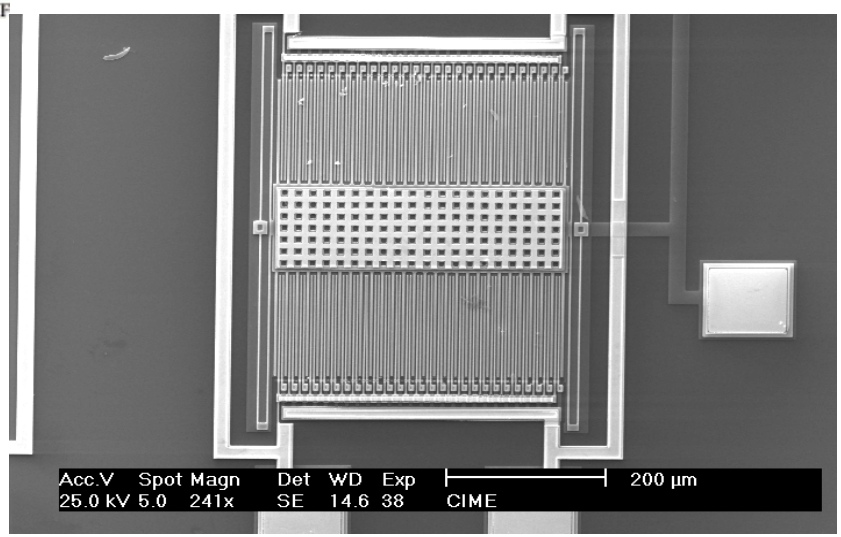
- **SOIMUMPs**
  - 10 or 25µ structure layer
  - Double-side pattern/etch
  - 2 Metal layers



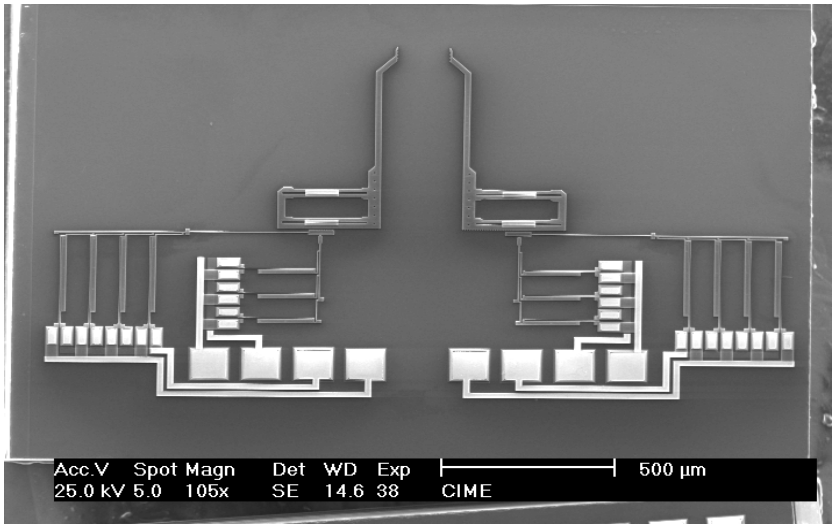
- **MetalMUMPs**
  - 10 lithography layers
  - Thick electroplated Ni (18-22µ)



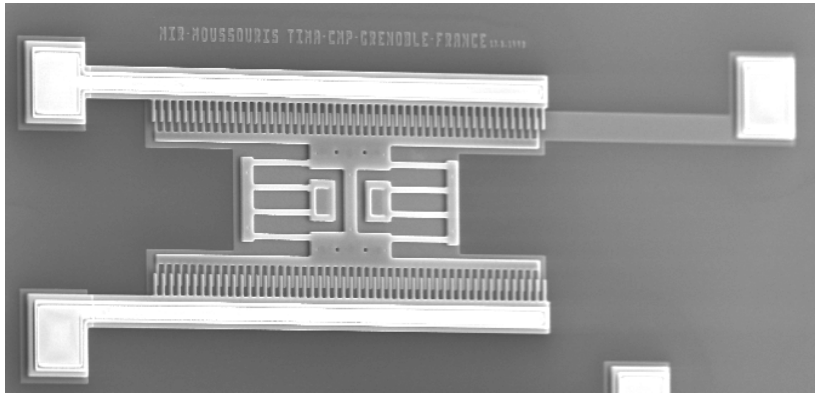
MUMPS Surface Micromachining Applications



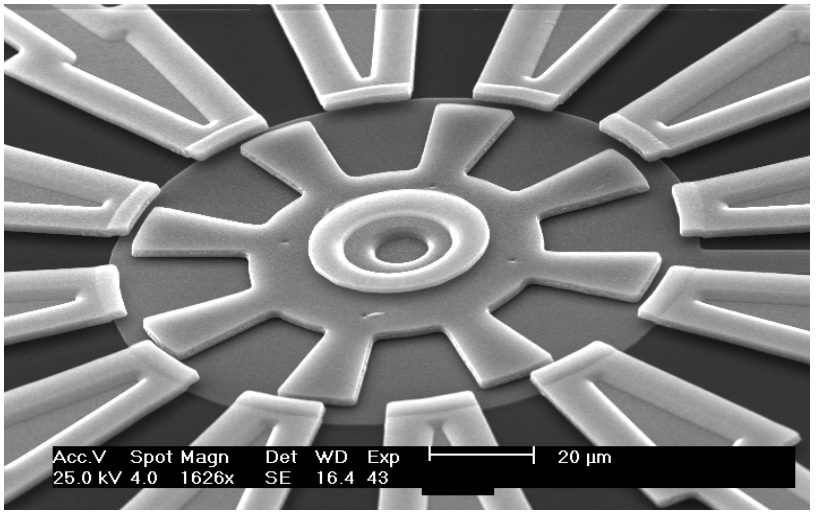
Accelerometer



Microgripper



Electrostatic comb drive resonator

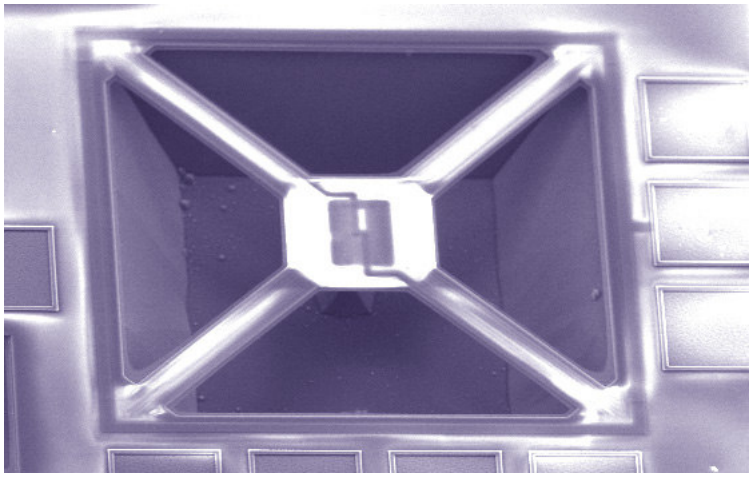


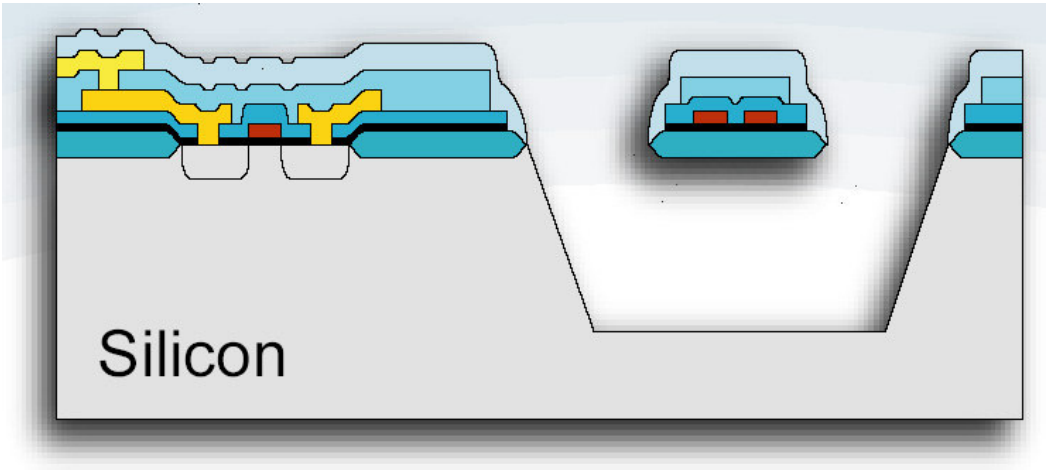
Electrostatic micro motor

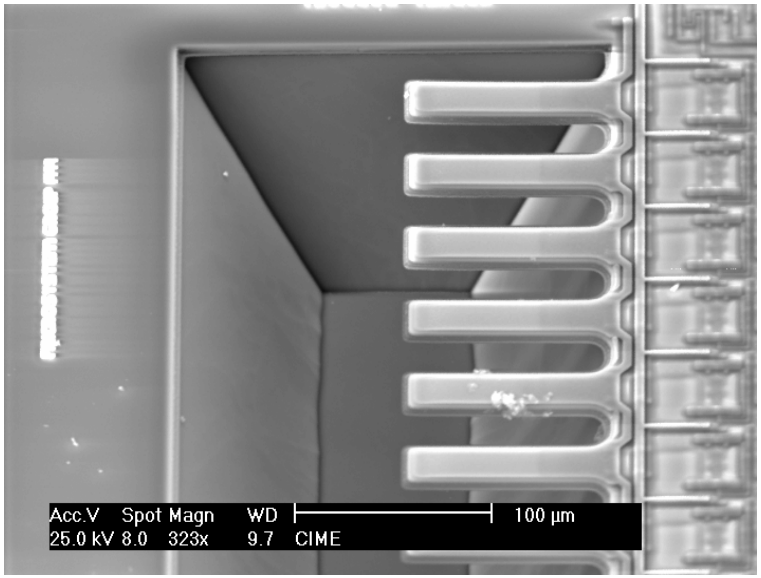
Bulk micro-machining on Silicon

CMOS FSBM

- Bulk Micro-machining on the AMS 0.35 µ CMOS
- Anisotropic Etching without additional mask

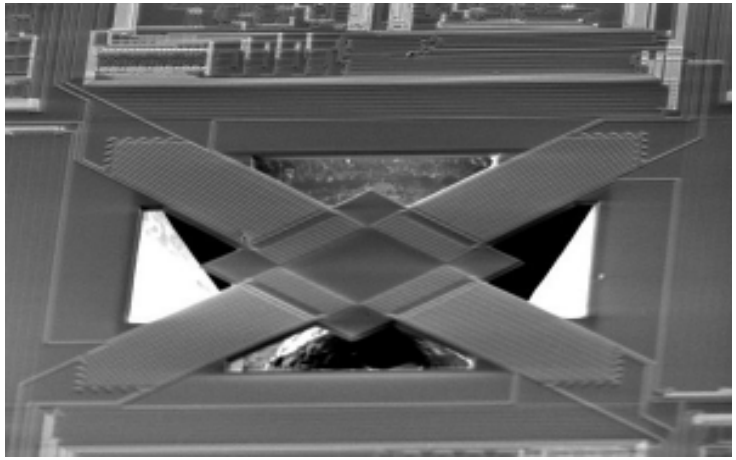




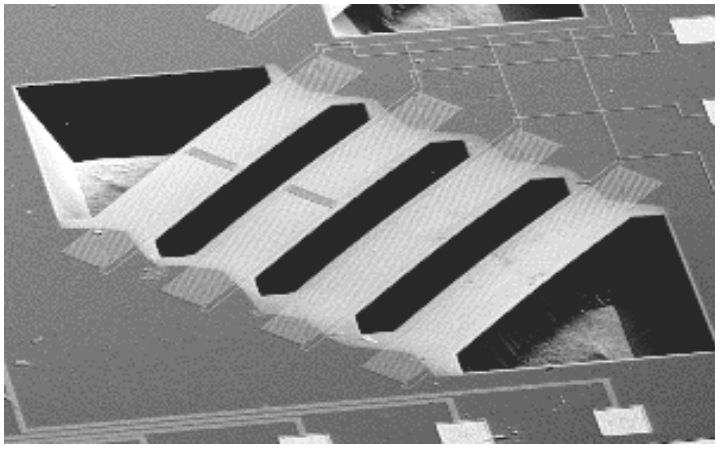


Embedded with electronics

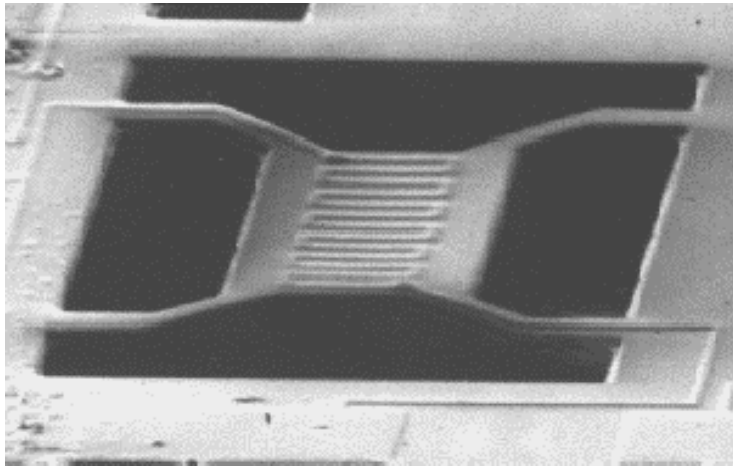
CMOS/BiCMOS Compatible MEMS



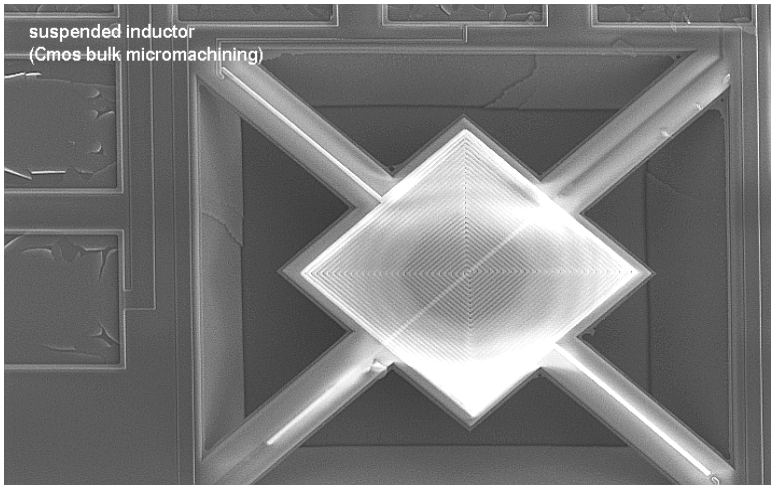
Gas flow sensor



Thermopiles



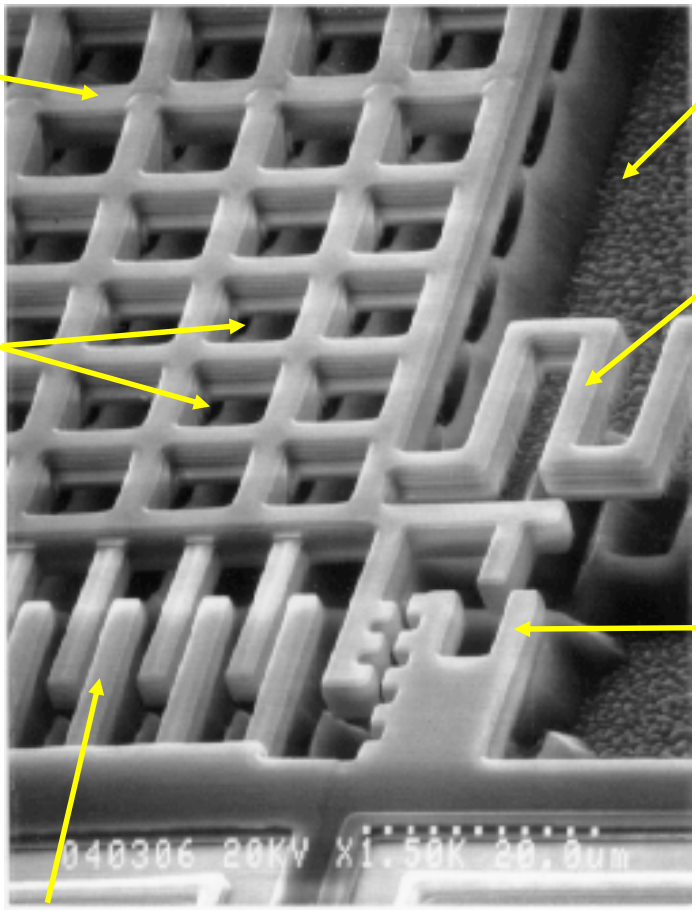
Thermal pixel



Suspended inductor

ASIMPS Process from CMU

- Low-cost integration with CMOS
- Rapid prototyping capability
- Fine line, fine gap microstructures
- Low parasitic capacitance
- Multiple isolated conductors
- Built-in piezoresistors



G. Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

Sandia MEMS process

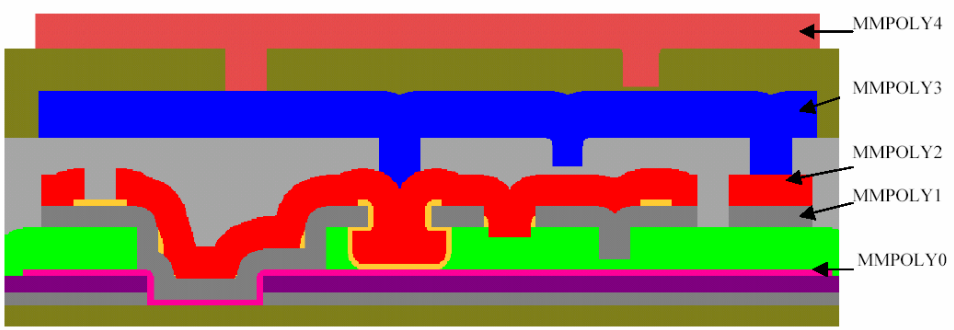
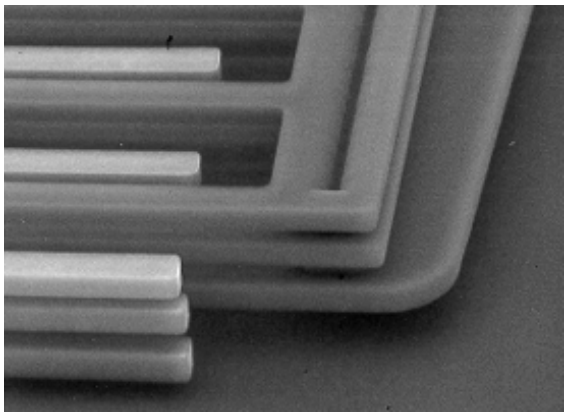
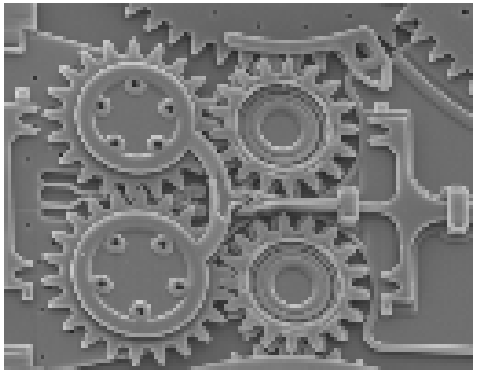
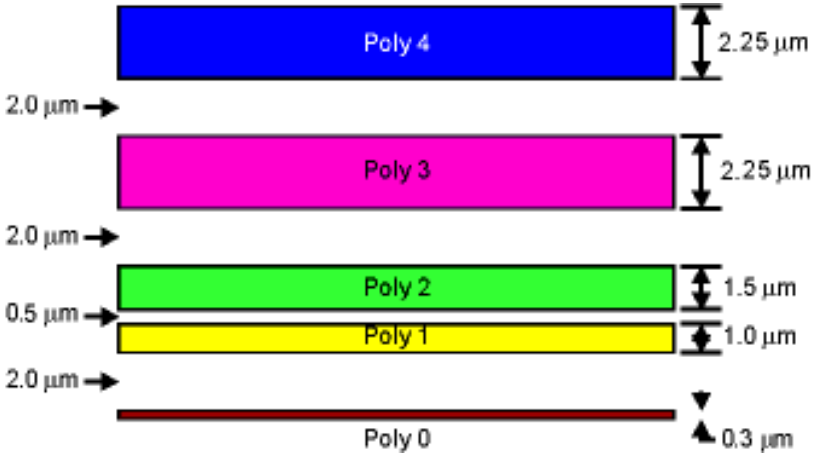
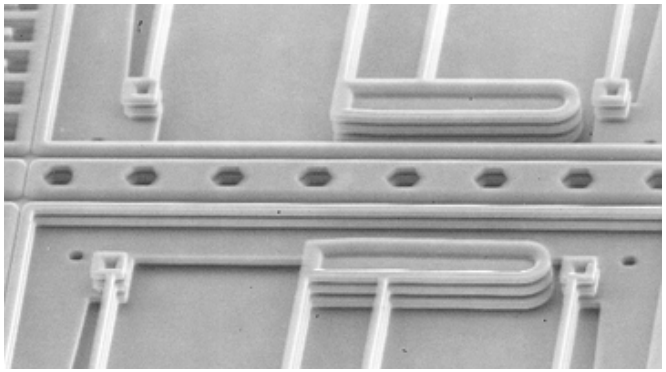


Figure 2. Cross-section of SUMMiT V stack showing features realizable through the fabrication process.









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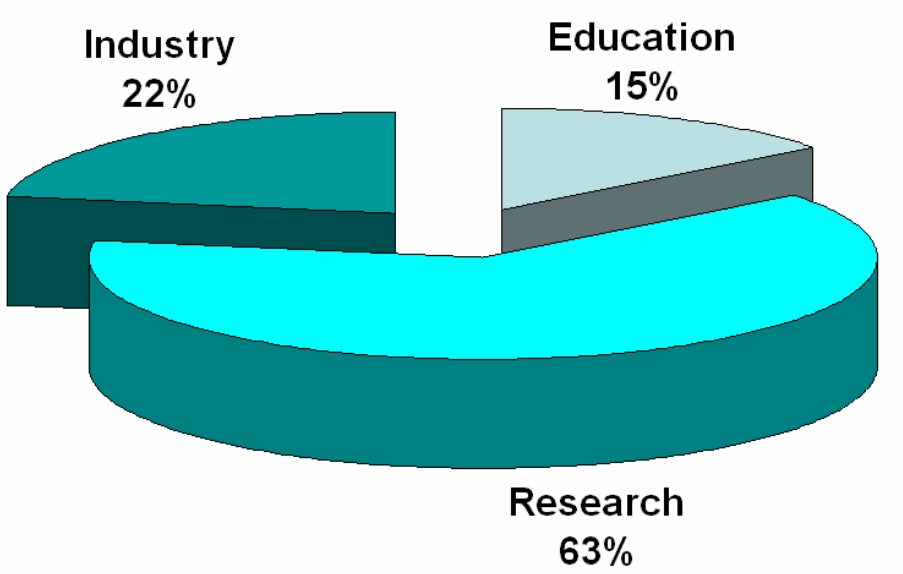
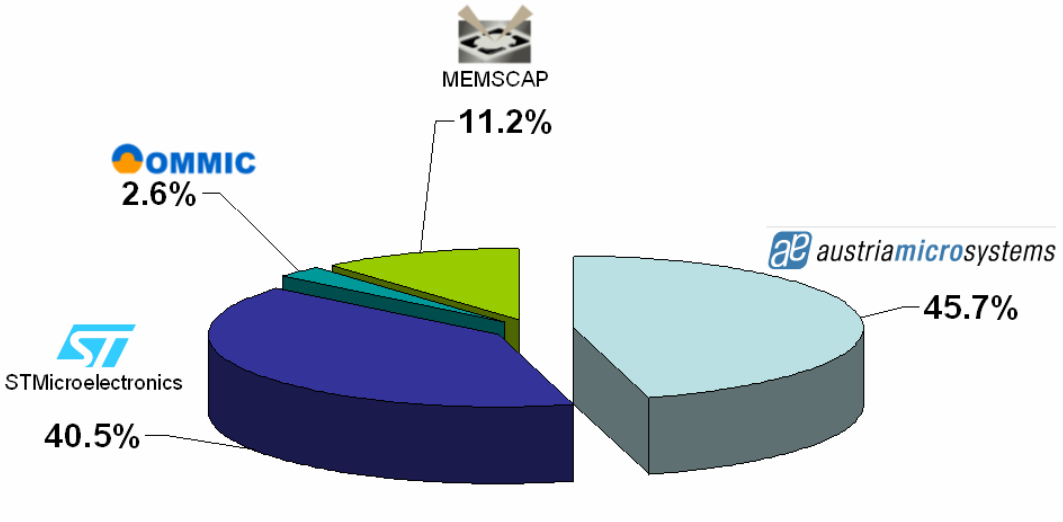
Activity Results for 2008

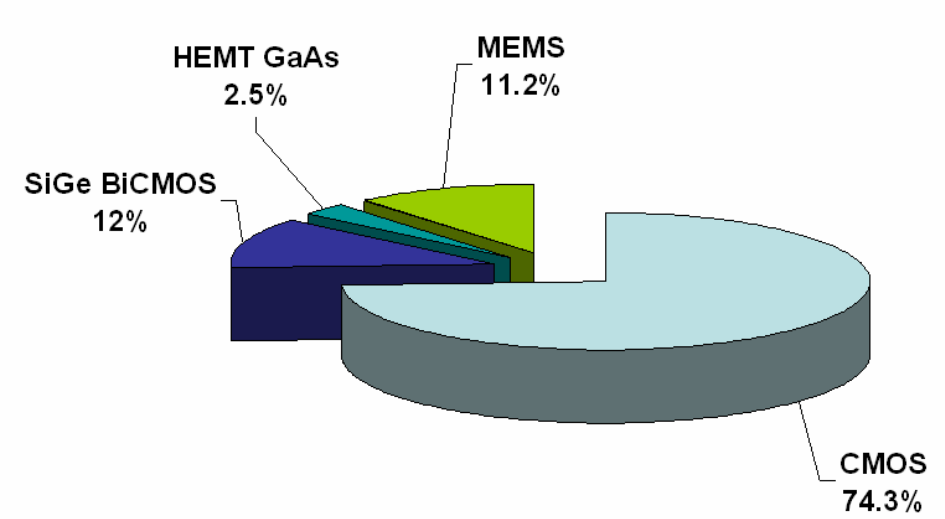
Circuits Fabricated in 2008

386 circuits fabricated
Coming from 92 Institutions

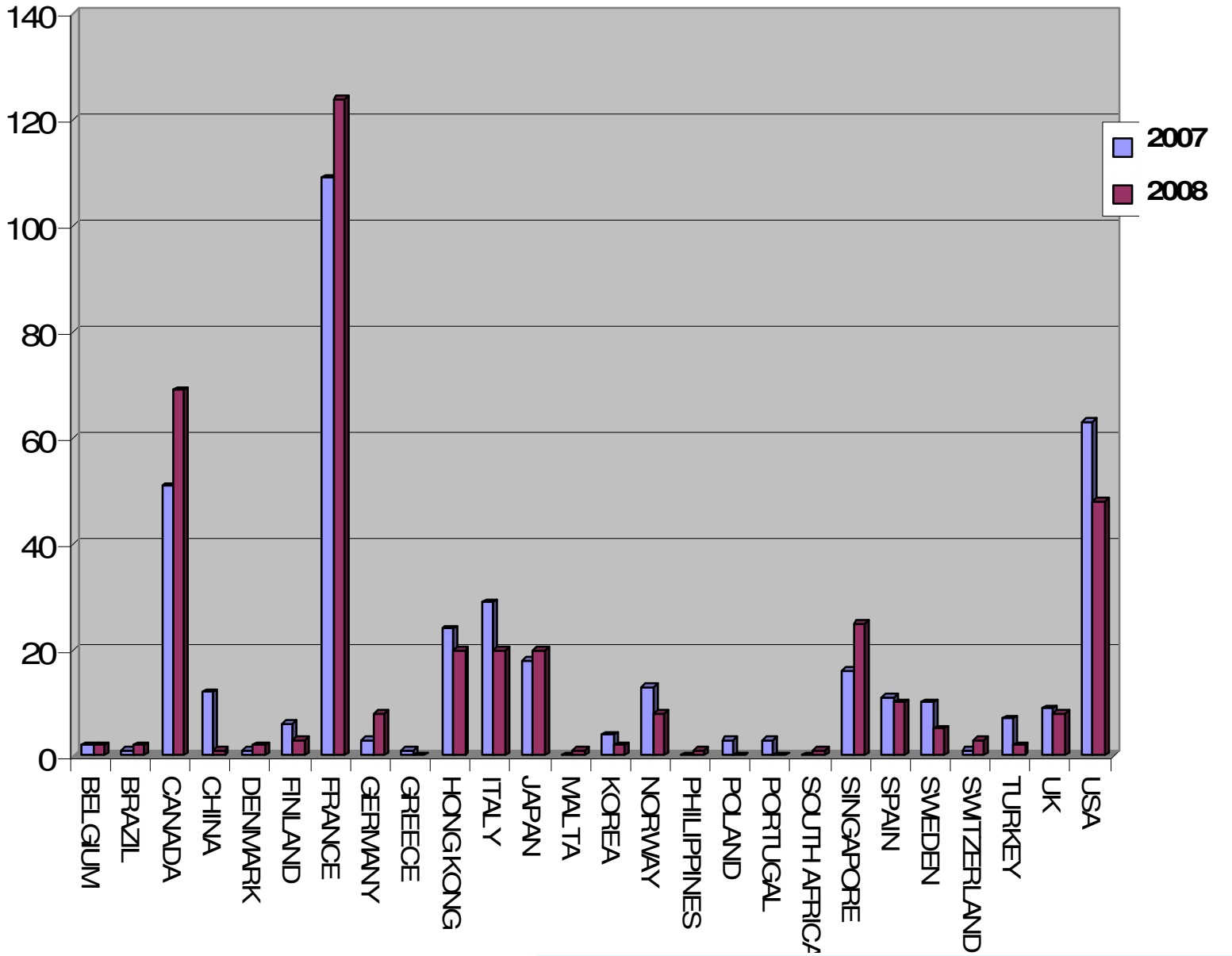
47 low volume productions
Coming from 18 Institutions



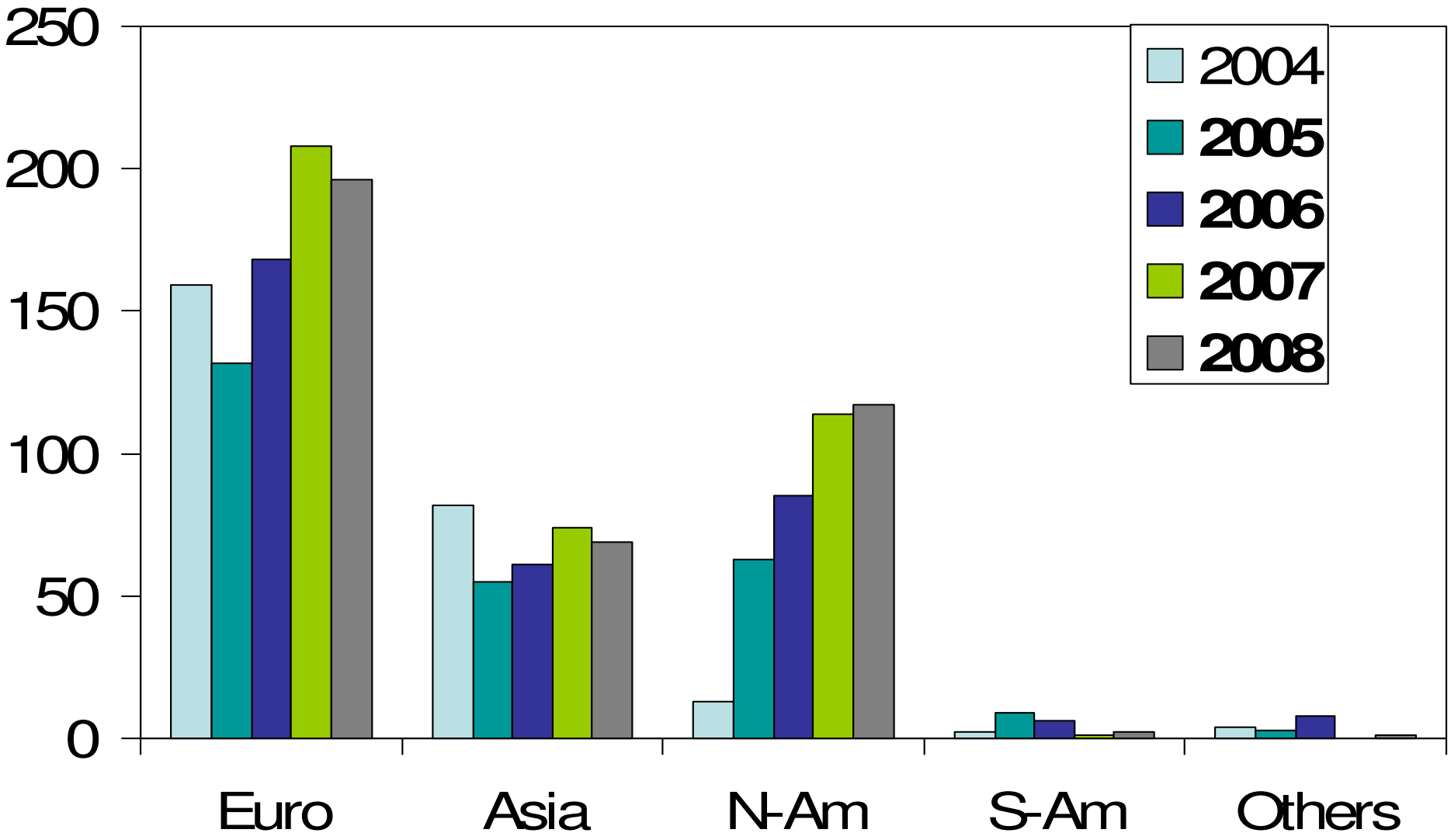




Nbr of Circuits per country in 2008



Nbr of circuits per Geographical Area

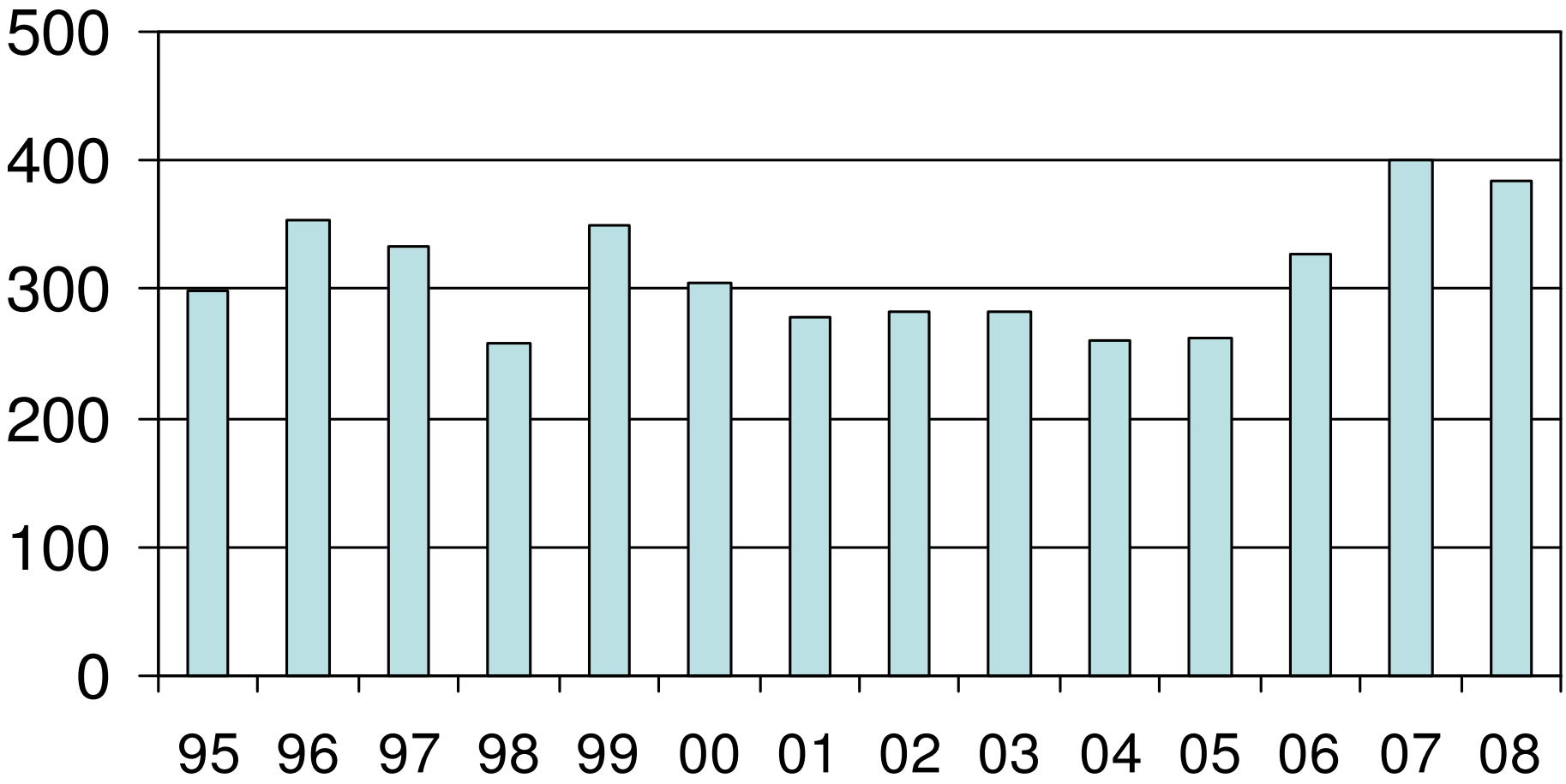


Participant Centres in France

CEA-SACLAY	GIF SUR YVETTE
Centre Microélectronique de Provence - Georges Charpak	GARDANNE
ENSEA	Cergy-Pontoise
ENSEEIHT	TOULOUSE
enseeith/inp	TOULOUSE
ENSERG	GRENOBLE
ENSI-Caen-lpc	CAEN
ENSIEG	GRENOBLE
ENSSAT-UNIVERSITE DE RENNES 1	LANNION
ENST	PARIS
Groupe ESIEE	NOISY Le GRAND
ID-MOS	GRADIGNA
IMS	TALENCE
INSA de lyon	VILLEURBANNE
Institut d'Electronique du Solide et des Systèmes	STRASBOURG
INSTITUT DE PHYSIQUE NUCLEAIRE	VILLEURBANNE
Institut d'Elec. du Sud (IES), CNRS Univ. Montpellier II	MONTPELLIER
INSTITUT SUPERIEUR D'ELECTRONIQUE DU NORD	LILLE CEDEX
INT Evry	EVRY
IPHC – IN2P3	STRASBOURG
LAL / IN2P3	ORSAY
L2MP POLYTECH Marseille	MARSEILLE
LAAS	TOULOUSE
Laboratoire SPINTEC CEA/CNRS	GRENOBLE
LETI/CEA Grenoble	GRENOBLE
LIRMM	MONTPELLIER
LPC / IN2P3	AUBIERE
LPSC / IN2P3	GRENOBLE
Neurelec	VALLAURIS
Observatoire de Paris	NANÇAY
SUPAERO	TOULOUSE
THALES	PALAISEAU
Thales Systèmes Aéroportés	ELANCOURT
Tiempo	MONTBONNOT
TIMA	GRENOBLE
Université Paris 13	VILLETANEUSE

36 Centres

Number of Circuits



Present cooperative efforts
CMC, CMP, MOSIS

- Why?

  To better serve the customer base by providing access to a larger technology selection.

- How

  + Share the cost of expensive and/or unique processes with limited customer base

  + Combine submitted designs into a common run, operated by one of the partners:

  If technologies are accessed by the individual groups, the customer base may be too small to support the technology, whereas combining the customers from all groups may be adequate to support the technology in question.

  + Expand the IP basis when technologies are shared in view of SoC/SIP design

Other Agreements with CMP

- IDEC, Korea
- ICC, China
- All Swedish Universities
- FAPESP, Sao Paulo state in Brazil
- Distributors

What's New at CMP in 2009

- 40nm CMOS from ST
- 130nm SiGe from ST
- AMS/CMP 0.35µ CMOS/MEMS bulk-micromachining
- SANDIA (DK from SoftMEMS on Tanner L-Edit)

What's New in 2010

- 100µ TSV from AMS on 0.35µ CMOS
- 0.18µ High Voltage from AMS (available end of 2009)
- Tezzaron / Chartered 130nm 3D-IC
- 32nm CMOS from ST

Questionnaire addressed to IN2P3 Labs

How many projects with TSV do you plan in 2010 and 2011 ?

Please elaborate for each project your answers as follows :

- Design Area
- Process (CMOS, CMOS-Opto, or High Voltage CMOS)
- Do you need to mix tiers coming from other foundries ?
- Number of TSVs per die
- TSV pitch
- How many prototyping iterations are you expecting ?
- Prototypes or low volme production, and how many parts ?
- Which packaging process will be used for the entire stack ?
- Application area.
- Any other additional information ...

Conclusion

- **More than Moore : Various technologies addressing : electronics, photonics, mechanics, …**
- **Moore's Law : Advanced CMOS processes**
- **Perspectives : TSV, 3D-IC, Spintronics**
- **Going Global**

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