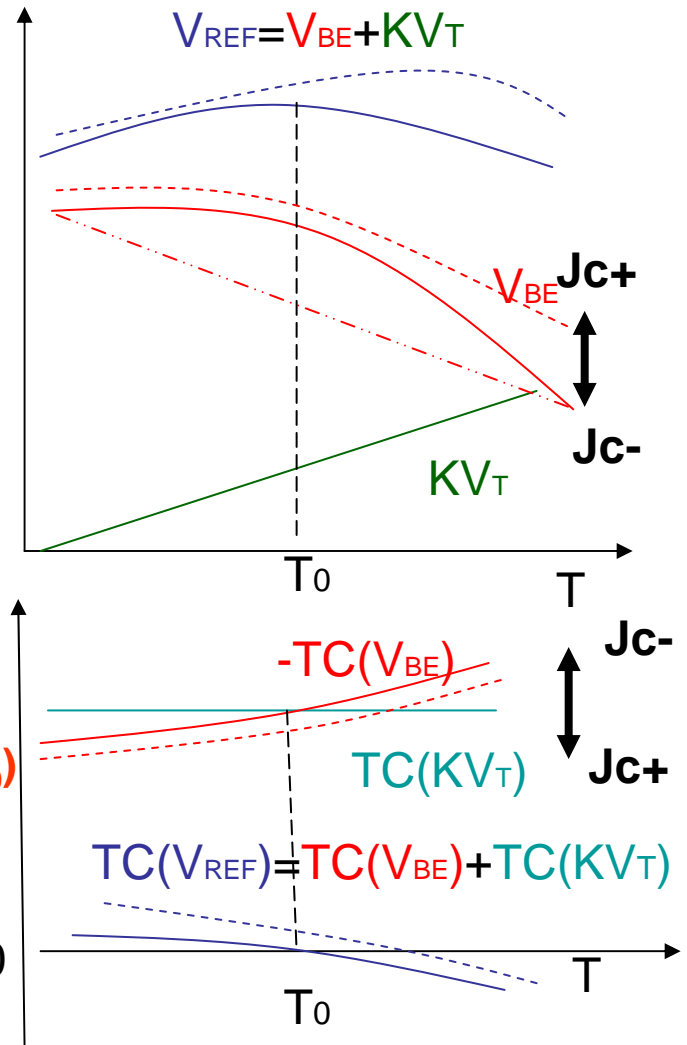
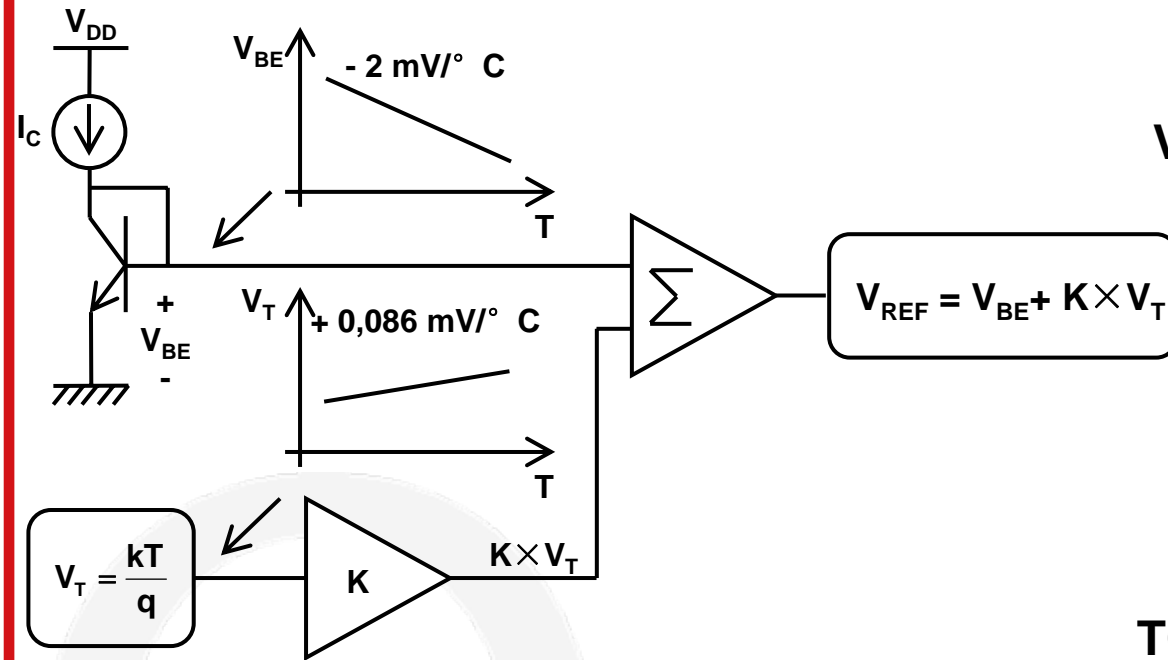
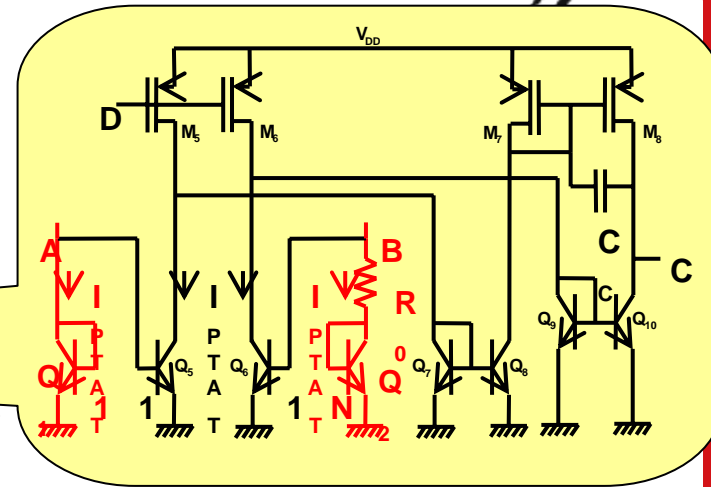
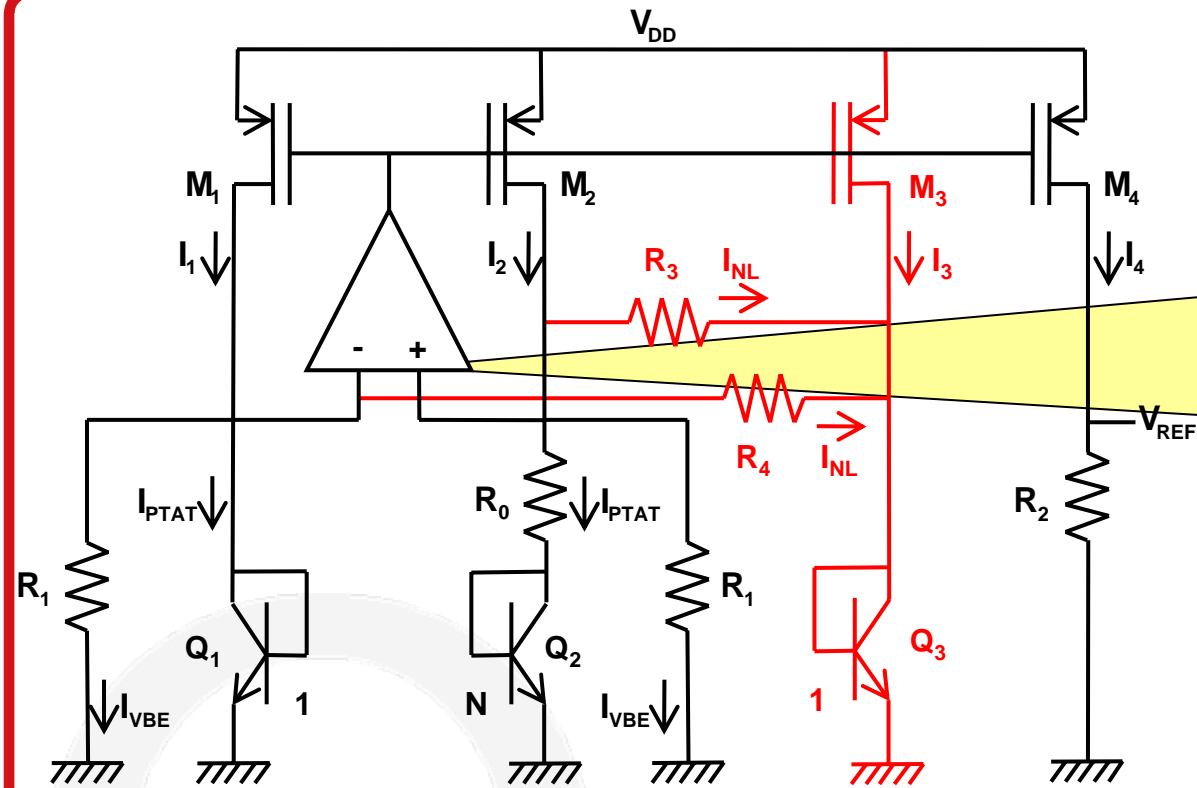


Bandgap design

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- $V_{BE}(T) = V_{G0} + (V_{BE0} - V_{G0})(T/T_0) - \gamma V_T \ln(T/T_0) + V_T \ln(J_C/J_{C0})$
- ↳ $J_C \propto T^\alpha \rightarrow V_{BE}(T) = V_{G0} + (V_{BE0} - V_{G0})(T/T_0) - (\gamma - \alpha) V_T \ln(T/T_0)$
- for $V_{G0} = 1,2 \text{ V}$, $V_{BE0} = 0,7 \text{ V}$, $\gamma = 3,5$ and $\alpha = 1$
- ↳ $\partial V_{BE} / \partial T = (V_{BE0} - V_{G0}) / T_0 - (\gamma - \alpha)(k/q) \approx -2 \text{ mV/}^\circ \text{ C @ } T_0 = 300 \text{ K}$
- $V_T = kT/q \rightarrow \partial V_T / \partial T = k/q \approx +0,086 \text{ mV/}^\circ \text{ C}$



$$N=21$$

$$R_0=10K, R_1=5*10K$$

$$R_{3,4}=2*10K, R_2=12*10K$$

$$\hookrightarrow V_{REF} = R_2 I_4 = (R_2/R_1) [V_{BE,Q1,2} + V_T (R_1/R_0) \ln(N) + V_T (R_1/R_{3,4}) \ln(T/T_0)]$$

$$\text{for } V_{BE,Q1,2}(T) = V_{G0} + (V_{BE0} - V_{G0})(T/T_0) - (\gamma - 1) V_T \ln(T/T_0)$$

$$V_{BE,Q3}(T) = V_{G0} + (V_{BE0} - V_{G0})(T/T_0) - (\gamma - 0) V_T \ln(T/T_0)$$

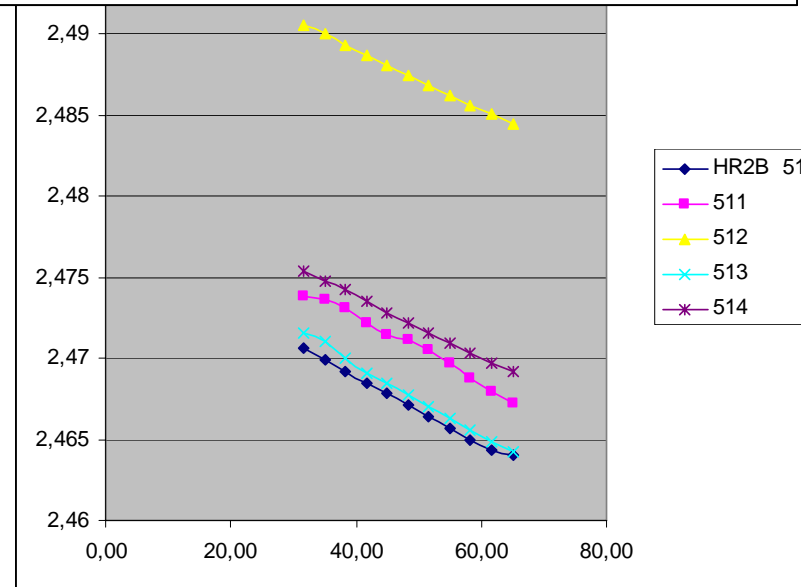
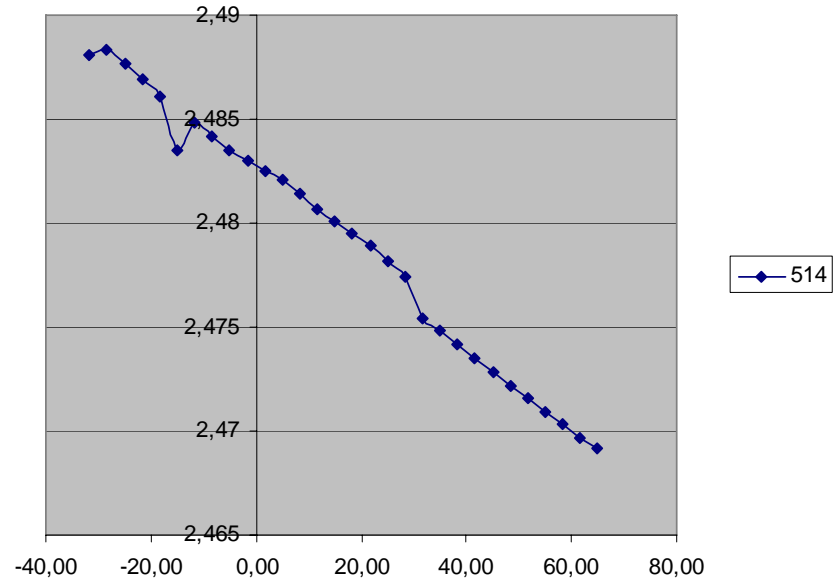
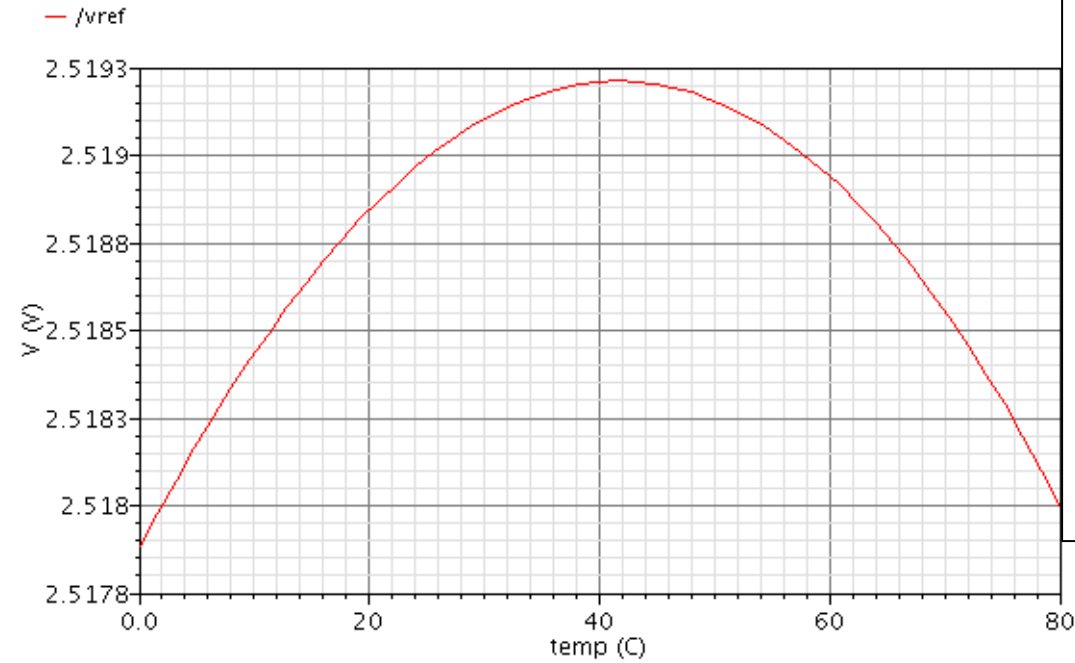
$$\hookrightarrow \text{Second order compensation} \rightarrow R_{3,4} = R_1/(\gamma - 1)$$



performance

HR2B 514

DC Response



Parameter	simulation	mearsurement
$V_{REF} @ T = 40^{\circ} C$	2.52 V	2.47 V
$\Delta V_{REF} (0^{\circ} C \leq T \leq 80^{\circ} C)$	$\pm 1,3 mV \rightarrow$ 6.5 ppm/ $^{\circ} C$ 50uV/ $^{\circ} C$	$\pm 15 mV \rightarrow$ 75 ppm/ $^{\circ} C$ 200uV/ $^{\circ} C$



Type of error	Res. Mismatch	Res. Tolerance	Res. T.C.	Trans. mismatch	Current mirror mismatch
Error in devices	2%	20%		2%	10%
Relative magnitude	Small	large	small	small	large

$$I_{PTAT} = \frac{V_T}{R_0} \ln\left(\frac{N I_{C1}}{I_{C2}}\right) = \frac{V_T}{R_0} \ln(N)$$

For Res. Tolerance:

$$I_{PTAT_R} = \frac{V_T}{R_0(1+\delta_R)} \ln(N) \approx \frac{V_T}{R_0} \ln(N)(1-\delta_R) = I_{PTAT}(1-\delta_R)$$

For current mirror mismatch:

$$I_{PTAT_I} = \frac{V_T}{R_0} \ln\left(\frac{N I_{C1}}{I_{C2}}\right) = \frac{V_T}{R_0} \ln\left[\frac{N I_{C2}(1+\delta_I)}{I_{C2}}\right] = I_{PTAT} + \frac{V_T}{R_0} \delta_I$$

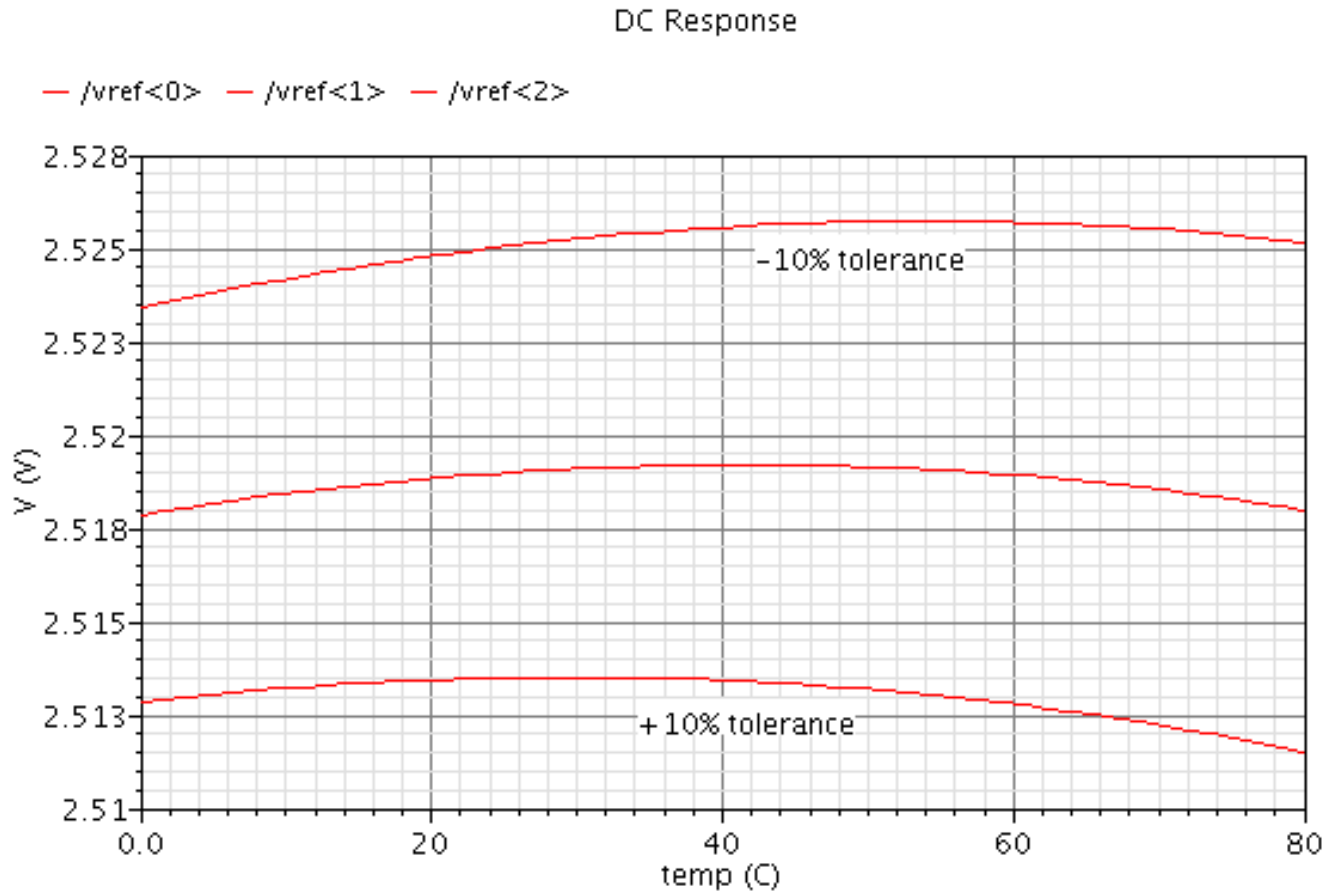
Layout:

all the transistors and resistors are common-centroid, identical

use low T.C. and low Tolerance Res.



Resistor tolerance 10%

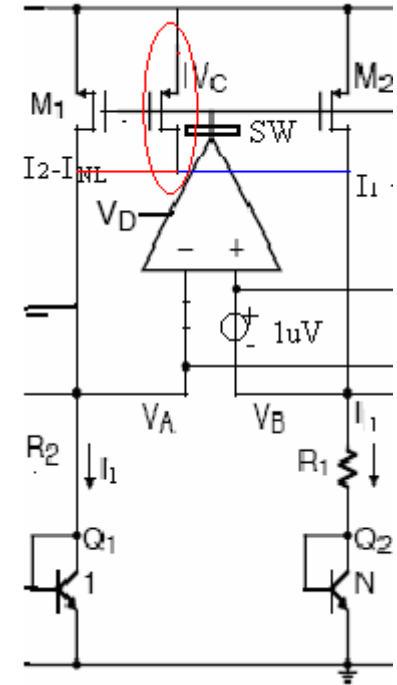
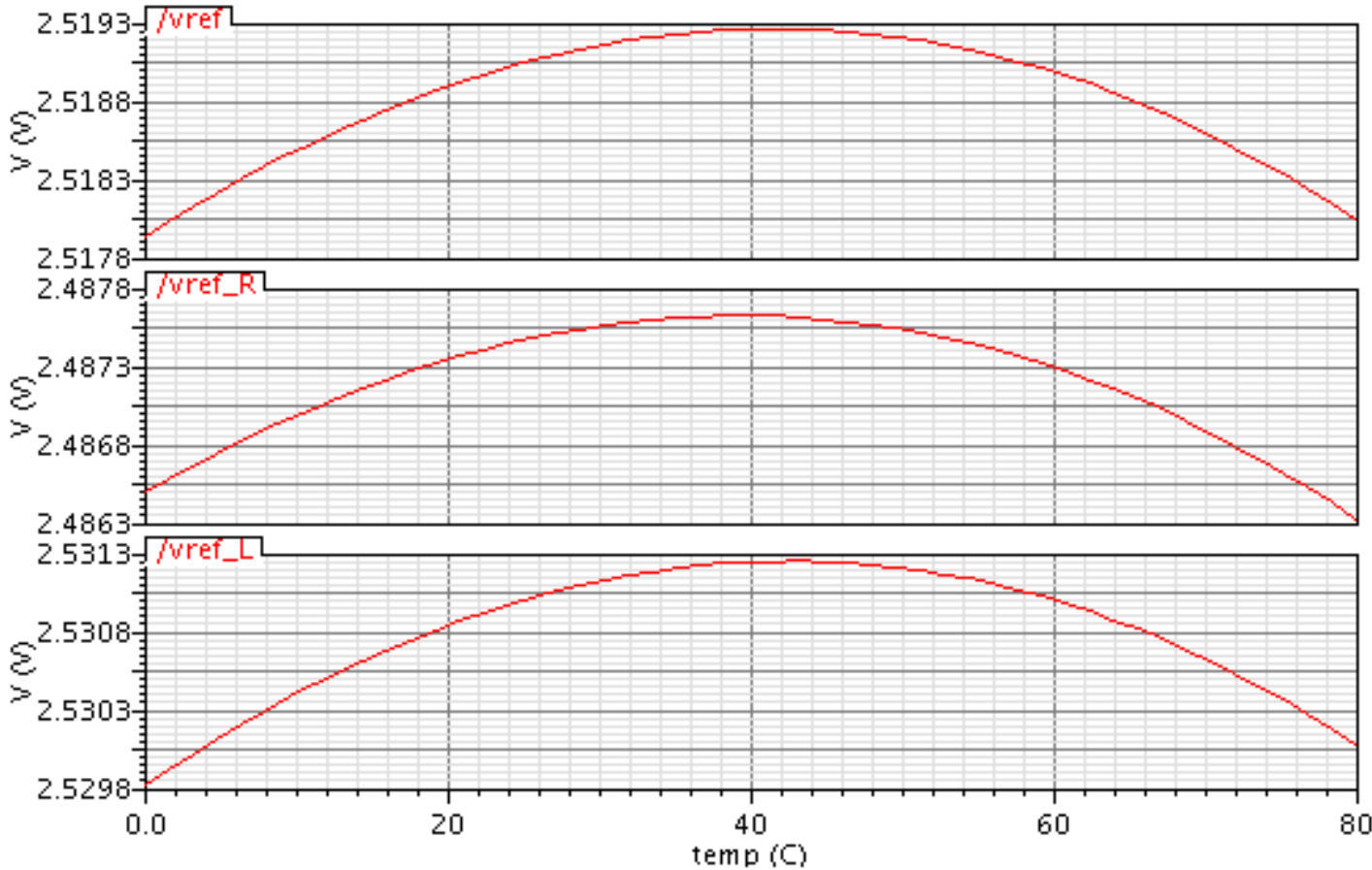


Peak diff:-6mv @30C~+10%

7mv @50C~-10%



DC Response



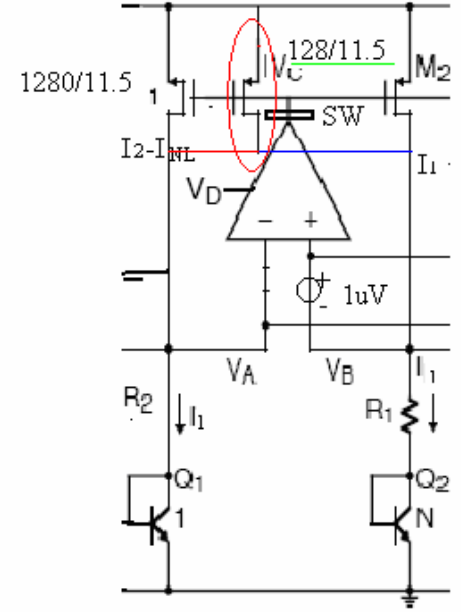
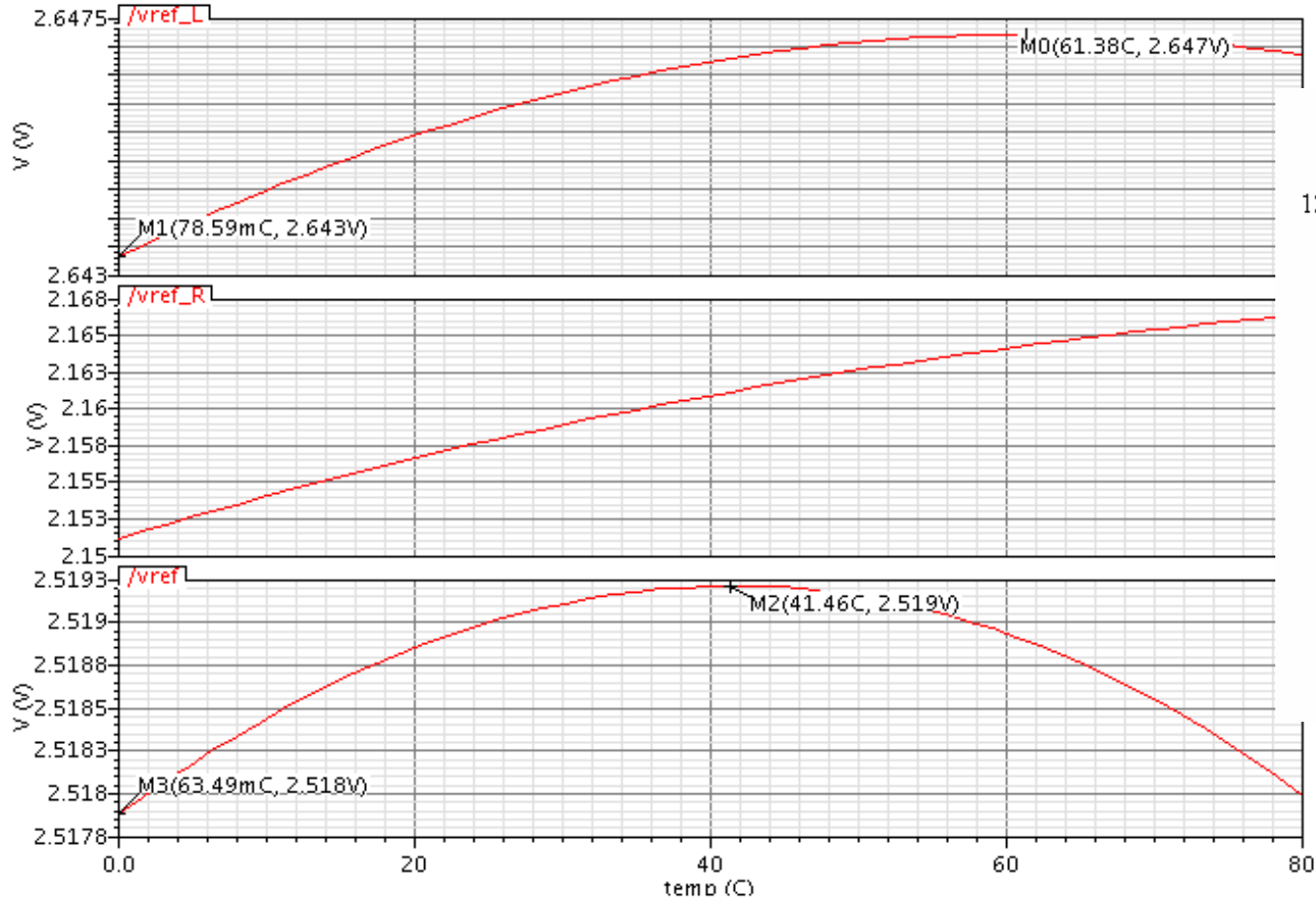
Peak diff:-32mv @35C~R

12mv @45C~L



current mirror mismatch 10% Ω mega

DC Response



Peak diff: 350 mv @ 120C ~R

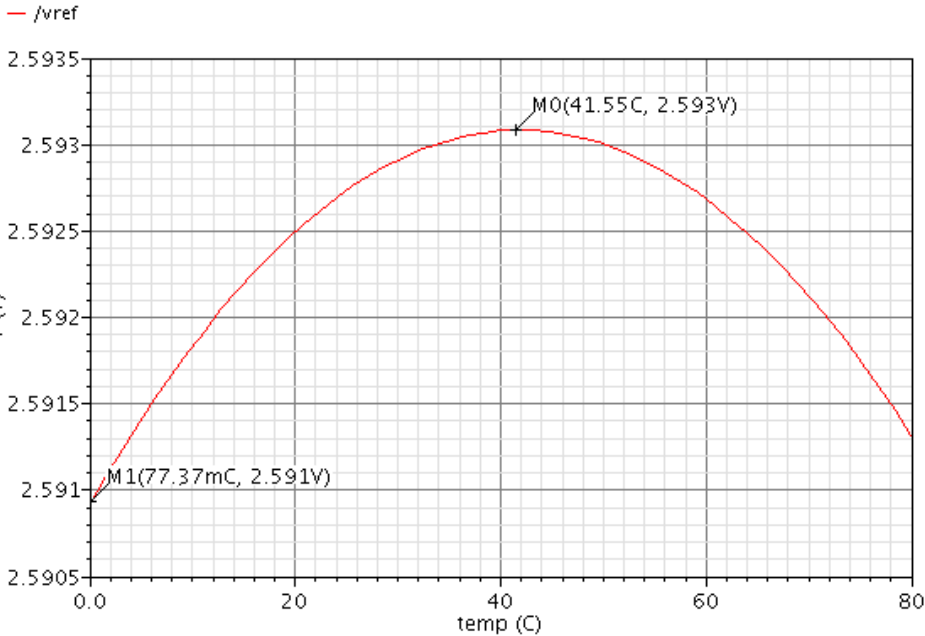
128mv @ 60C ~L



- Use Cadence -mmsim60

- Use Cadence-mmsim62

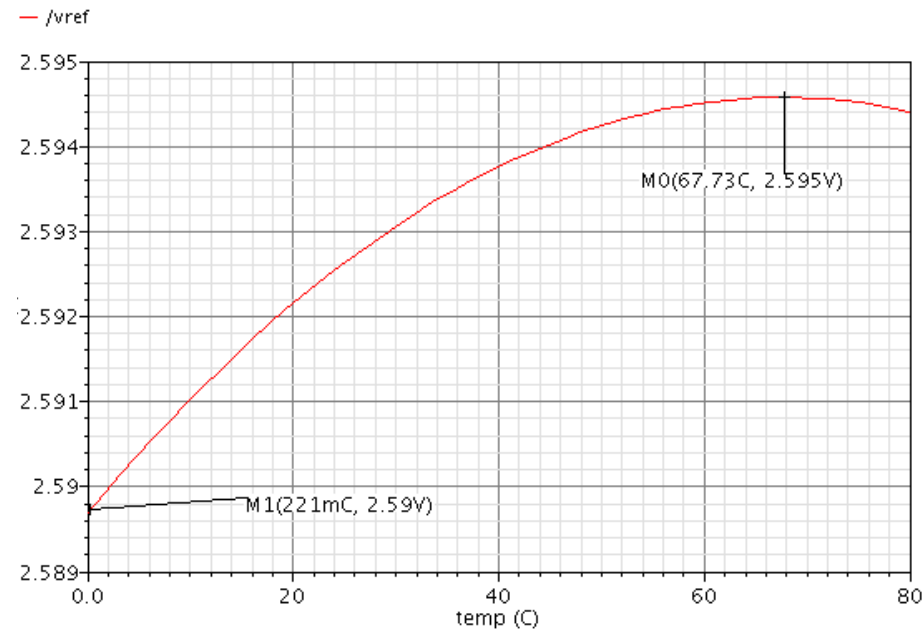
DC Response



peak:

@ 41°C

DC Response



@ 68°C



layout

