« Briques » pour ADC pipeline 8 bits 100MS/s du projet INNOTEP

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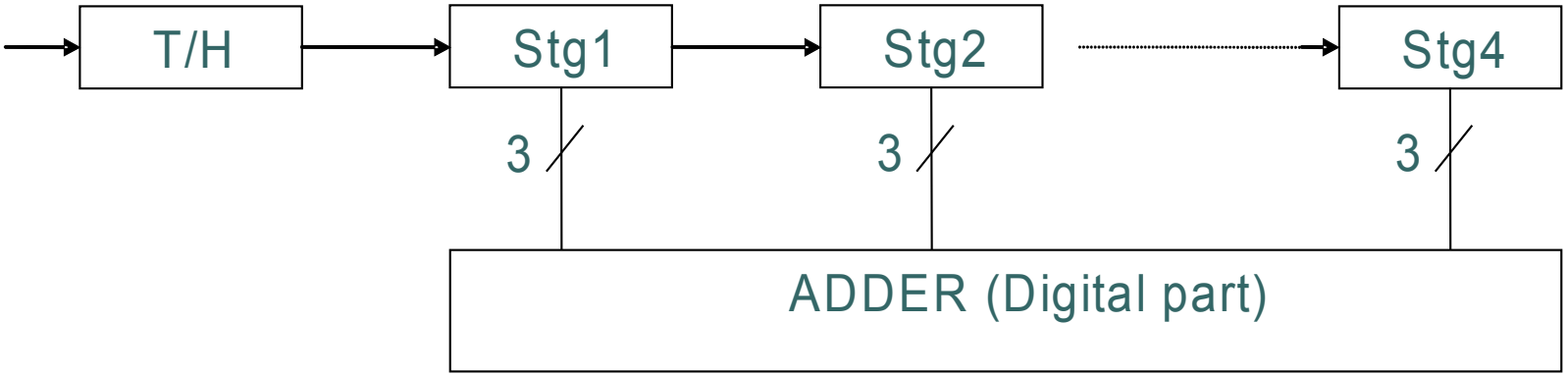
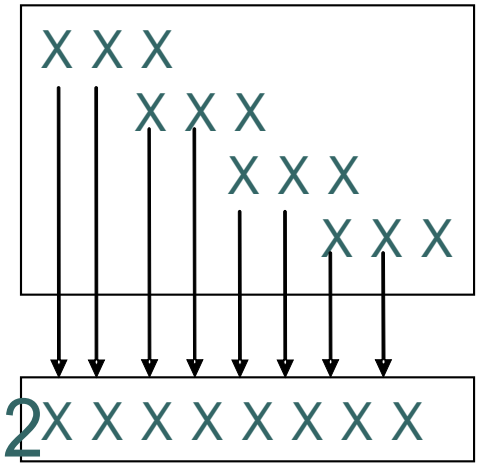
ADC design





- Differential inputs 2V p. to p.
- 100MHz Pipeline
- 2,5bits per stage
- 4 periods latency
- 24 comparators

Technology, supply and tolerances

Use of AustriaMikroSystems 350nm BiCMOS technology.

3.5 V analogue supply voltage (maximum dynamics).

3.3 V digital supply voltage.

"Smart" structures in current mode => current driven blocks

Behavioral simulations were made to determine what are the structure critical points:

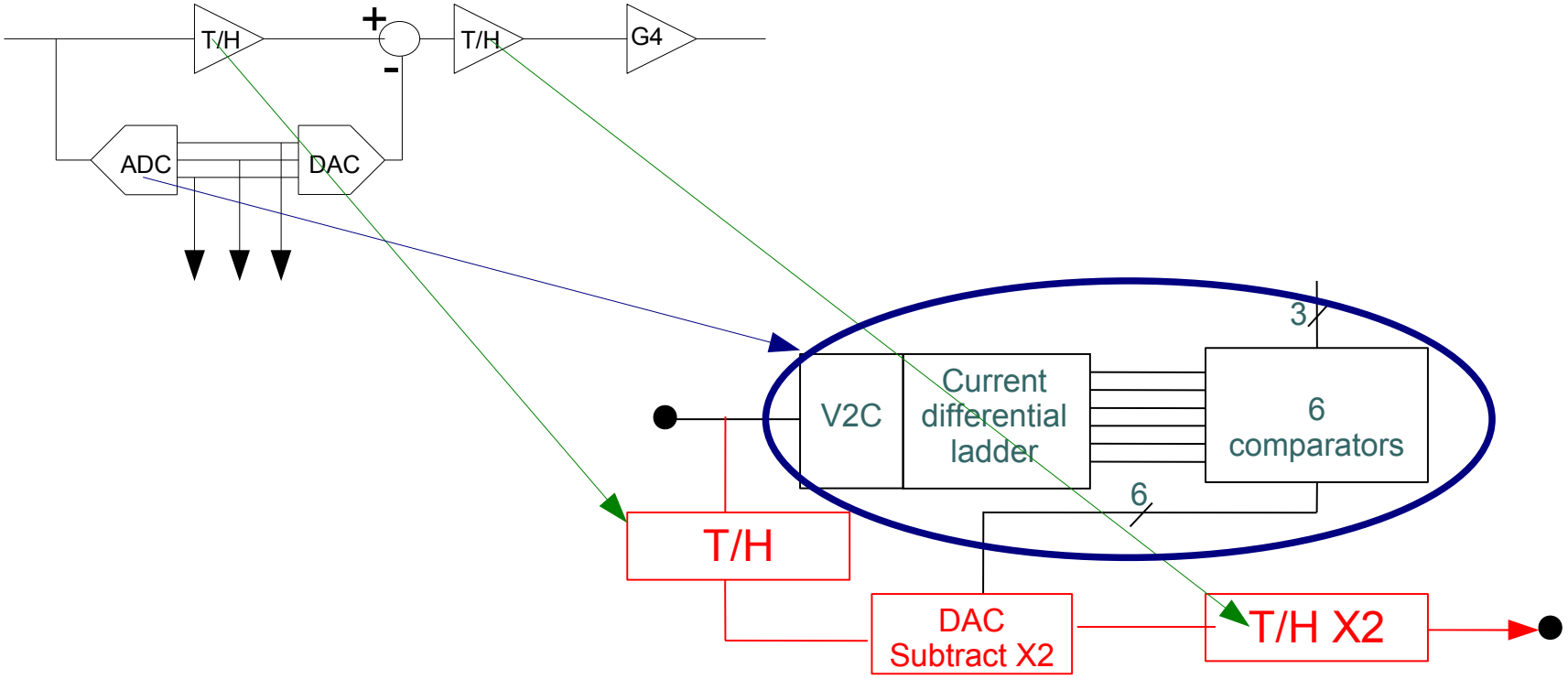
we need high sensitivities comparators.

Comparators offset uncritical (1/16 of dynamics => 125mV).

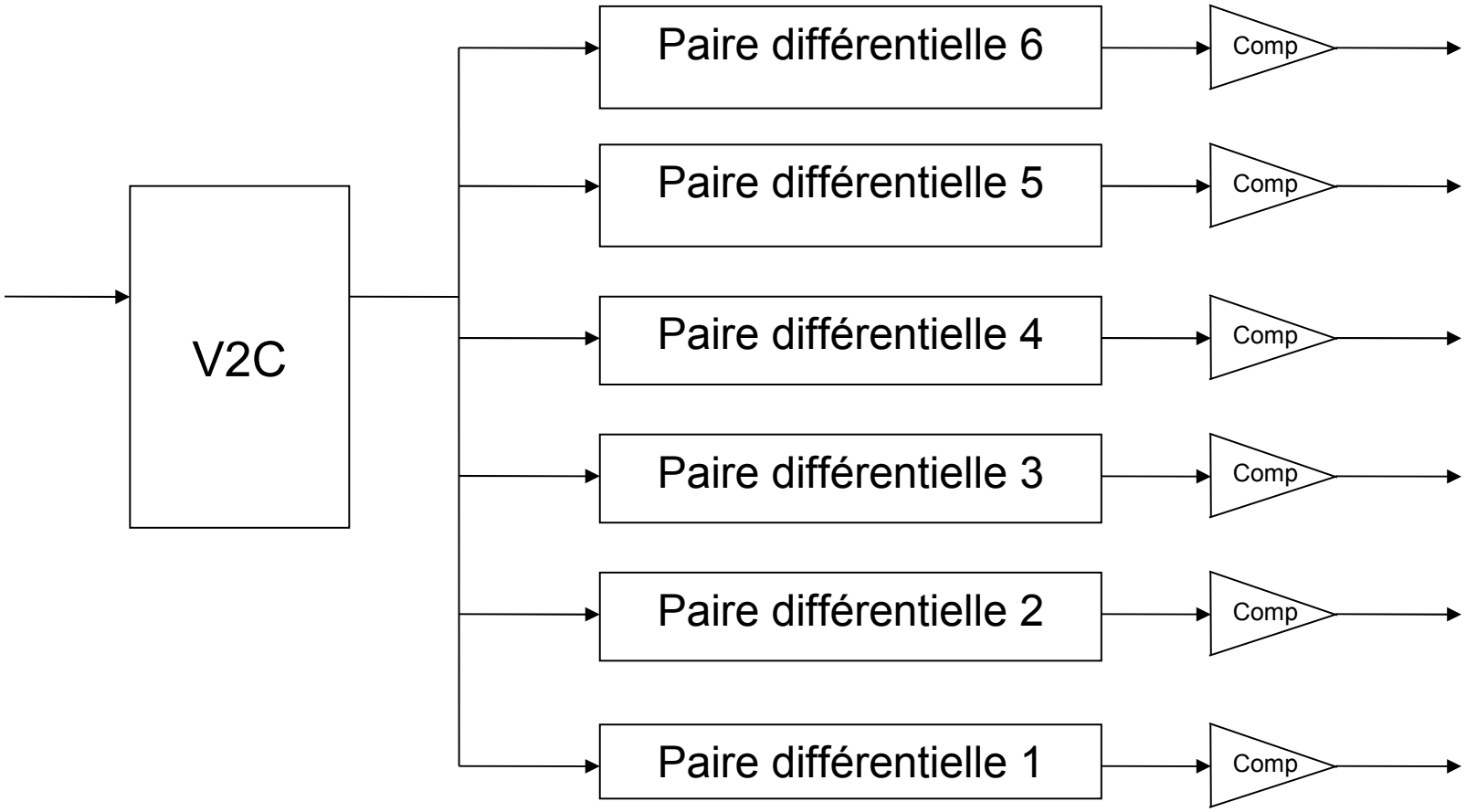
Quality of references and amplifiers is a key point in the first stage (+/- 2LSB).

The gain error max for free error conversion is 4%.

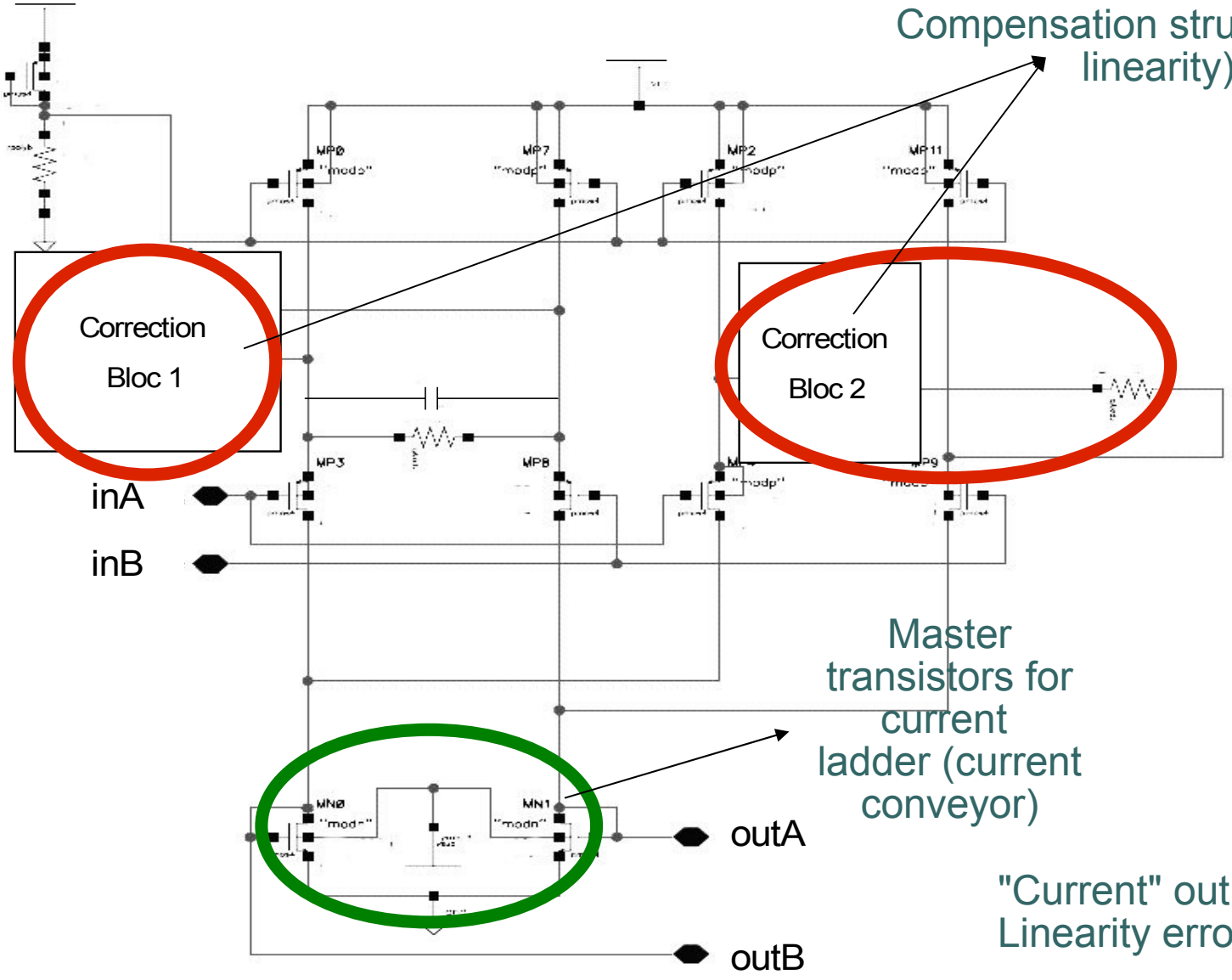
Stage theoretical structure



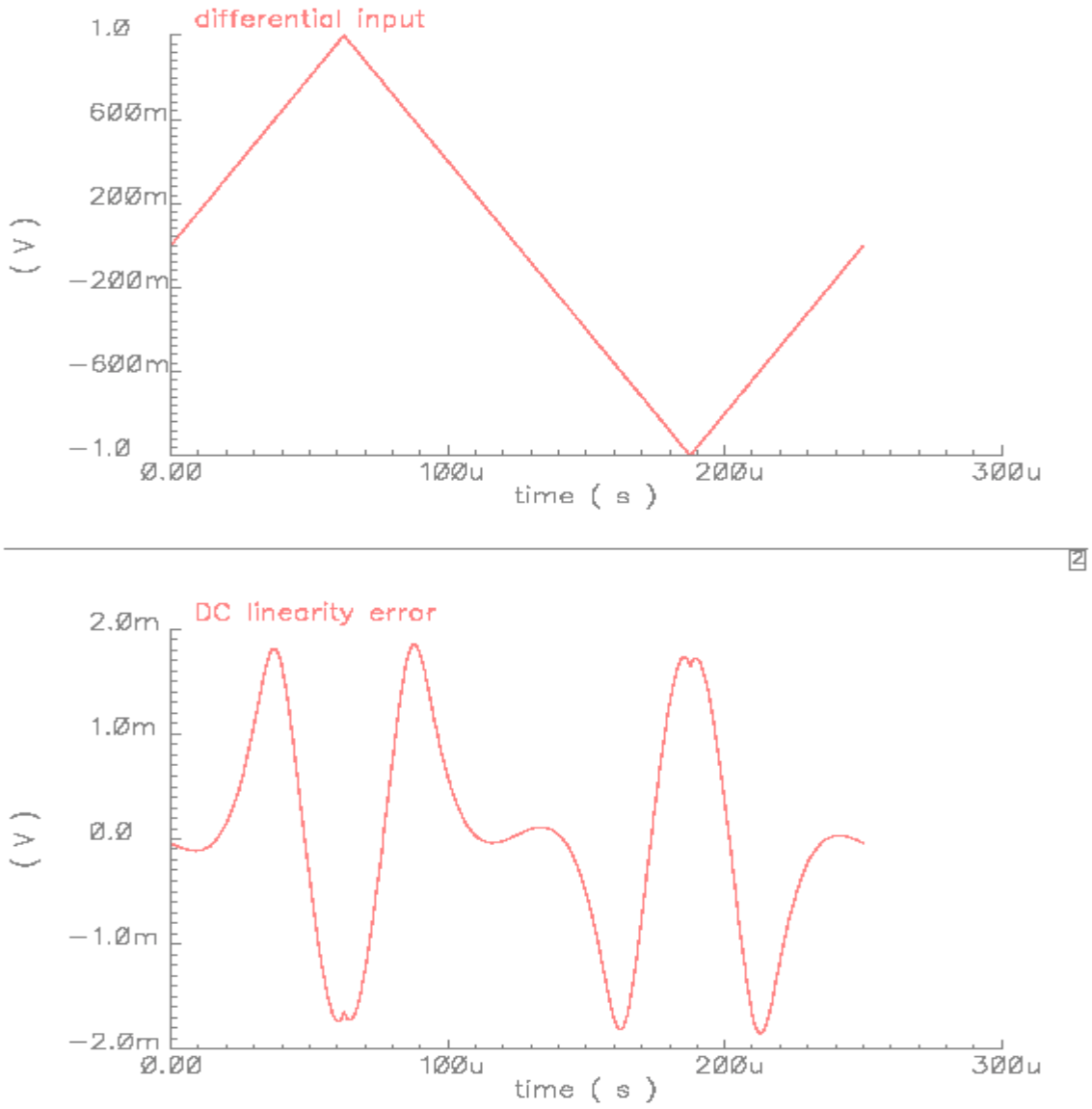
The comparison line



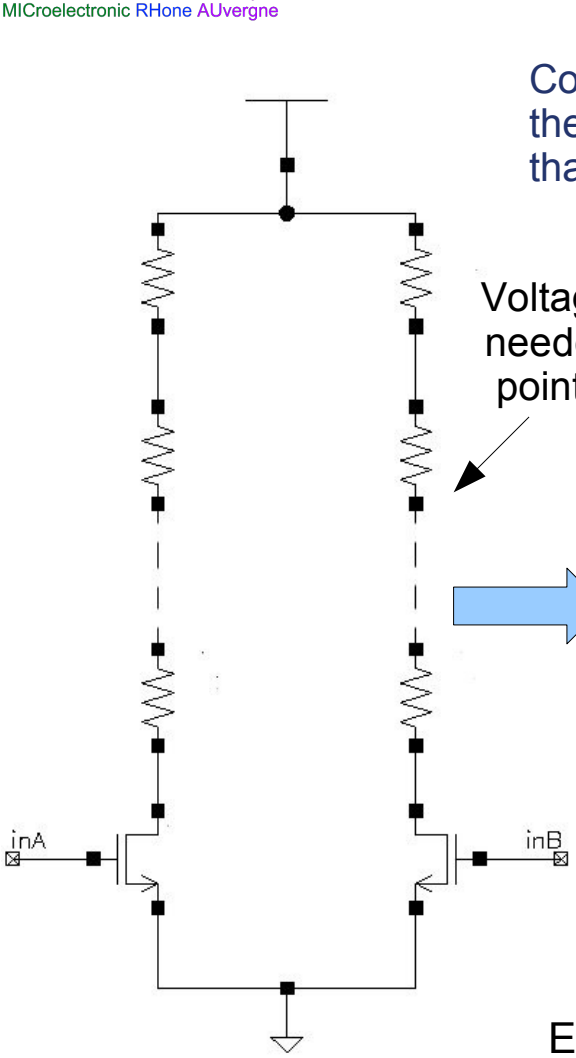
The Voltage to Current block



The Voltage to Current block



The differential ladder

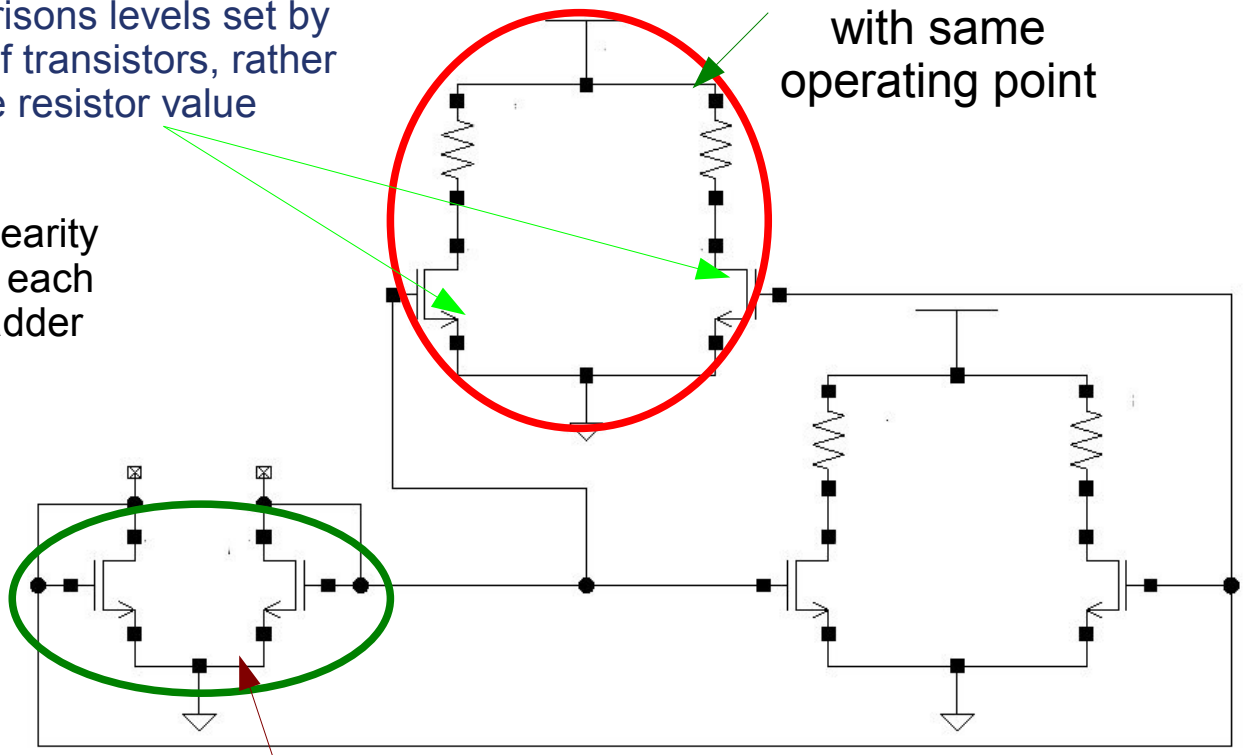


Voltage differential ladder

Comparisons levels set by the W of transistors, rather than the resistor value

Voltage linearity needed at each point of ladder

6 differential pairs with same operating point



Current master (V2C)

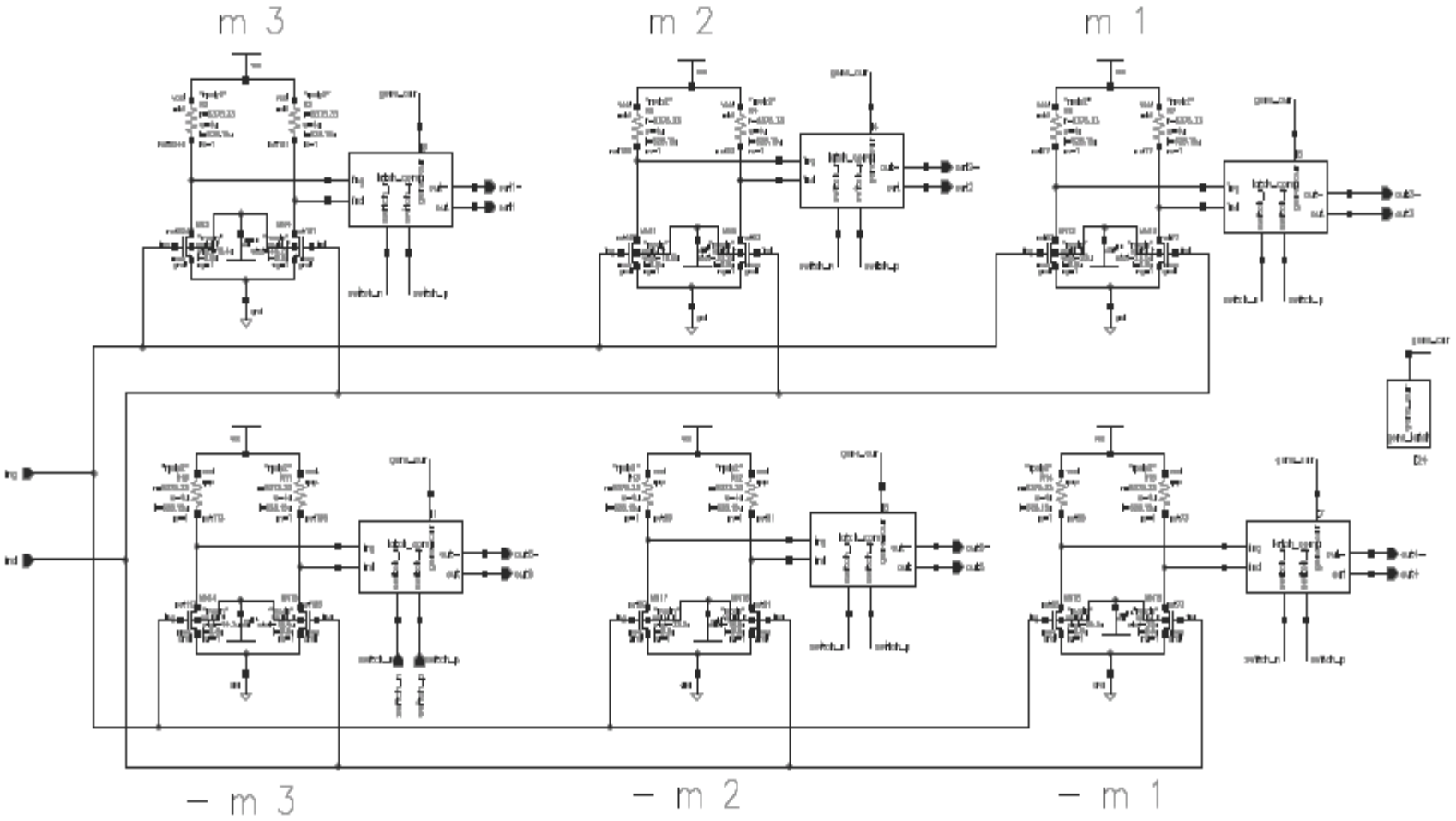
Current differential ladder

Eliminates partly of kick back noise

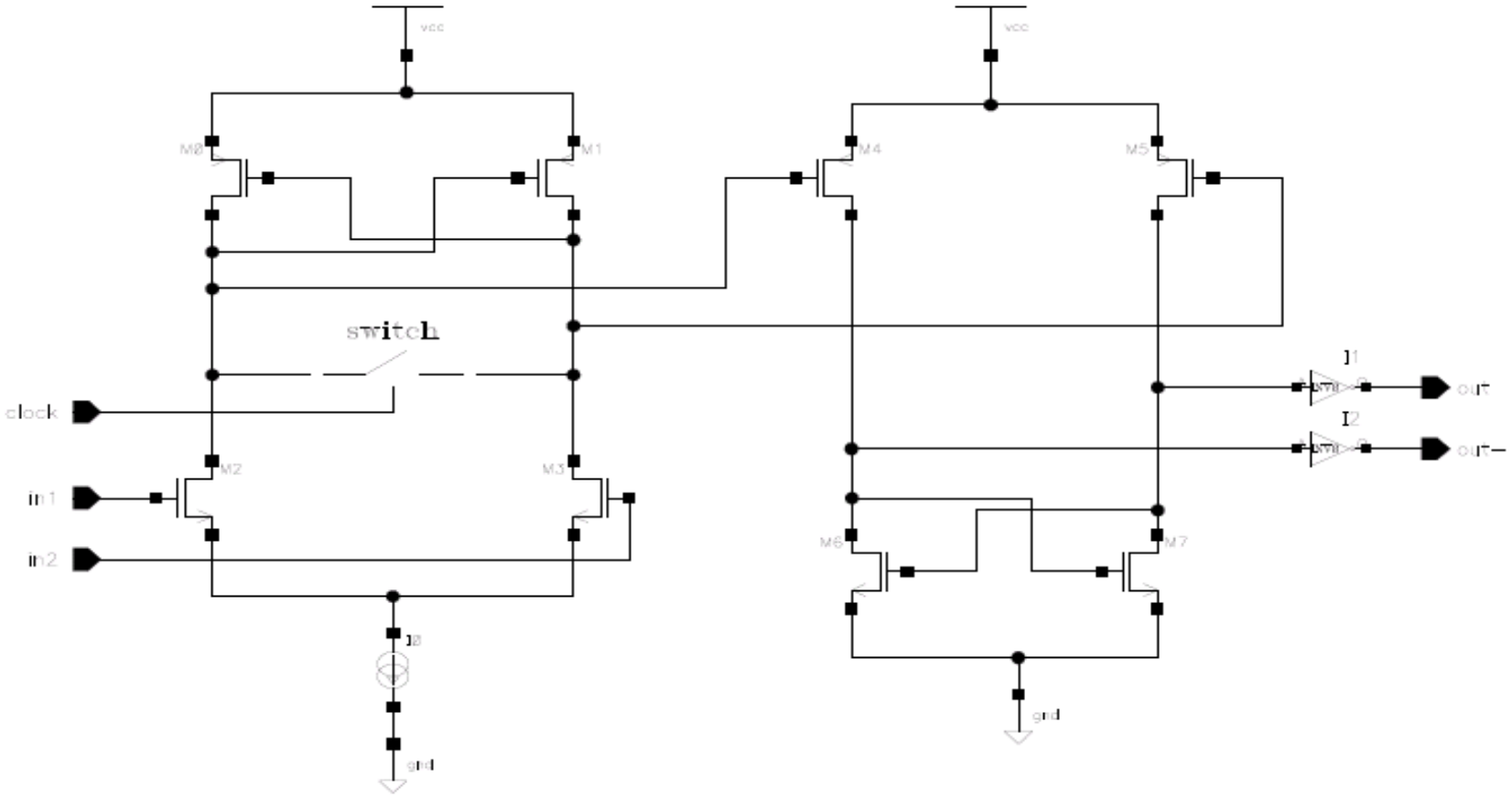
6 identical comparators

Linearity needed only at comparison point (0V diff. and the same CMV)

The differential ladder

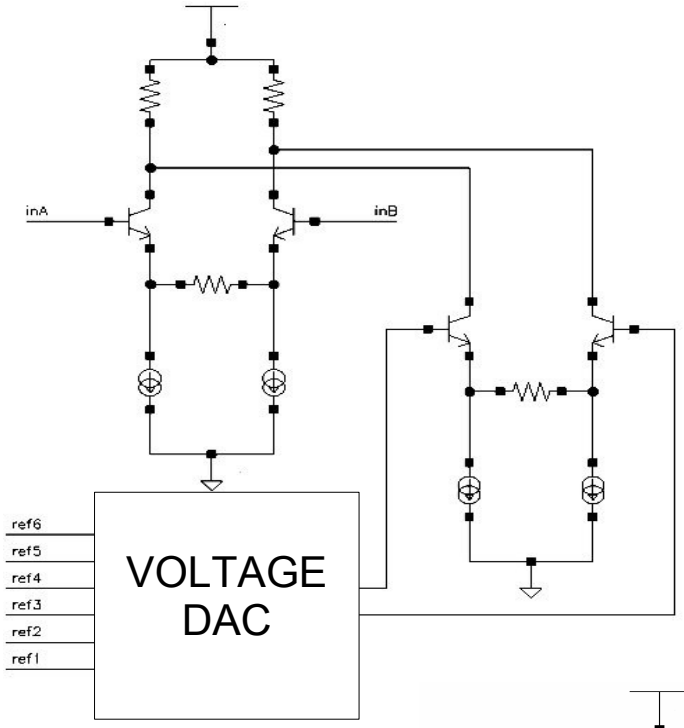


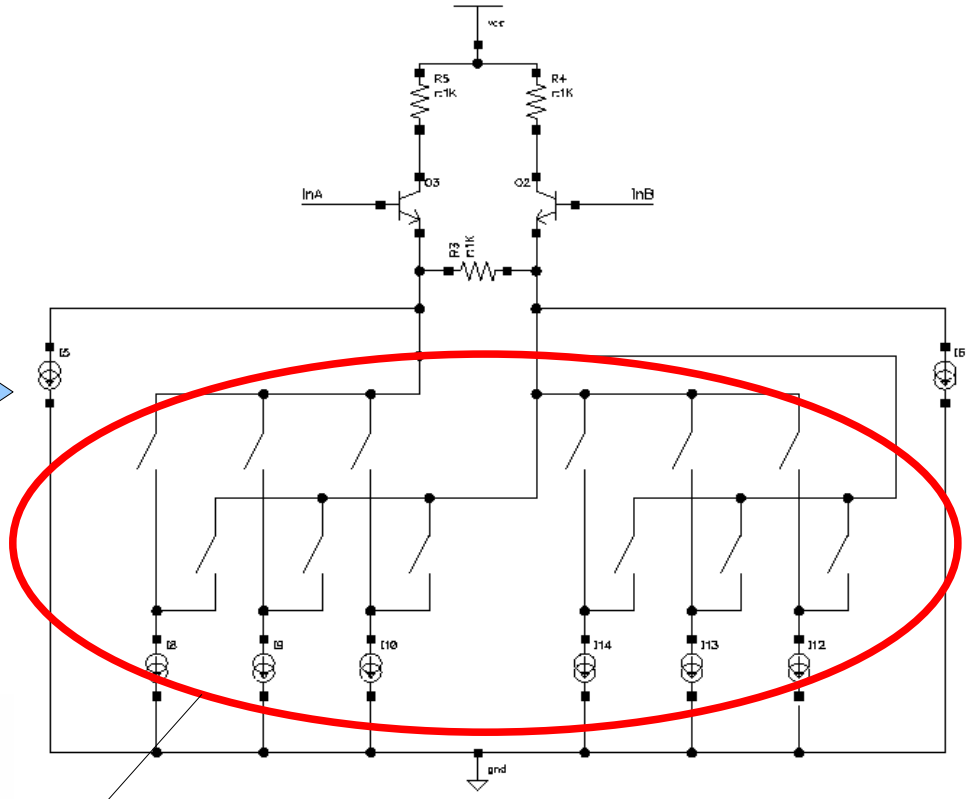
Comparators

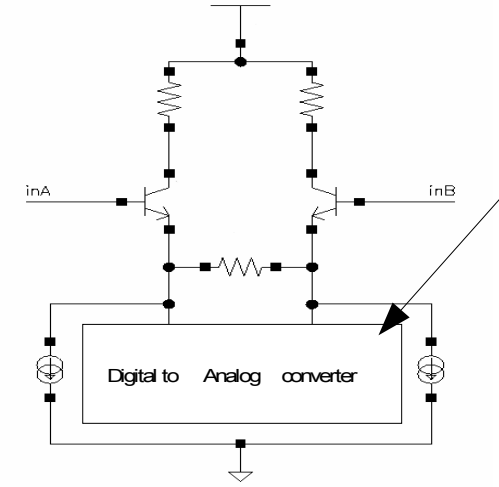


"Latched" structure pushed at an operating frequency >> 100MHz.
Sensibility ~ 150uV (due to the noise, simulated with “transient noise”)

Subtract Gain 2



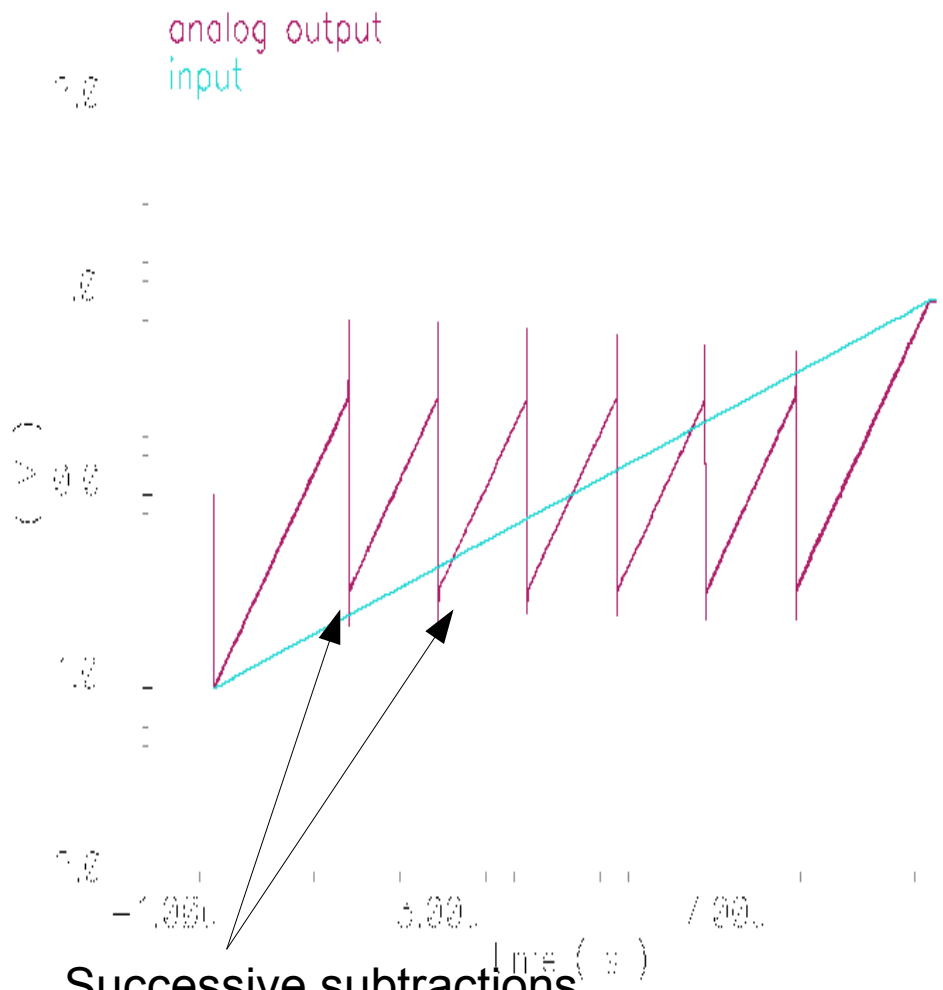


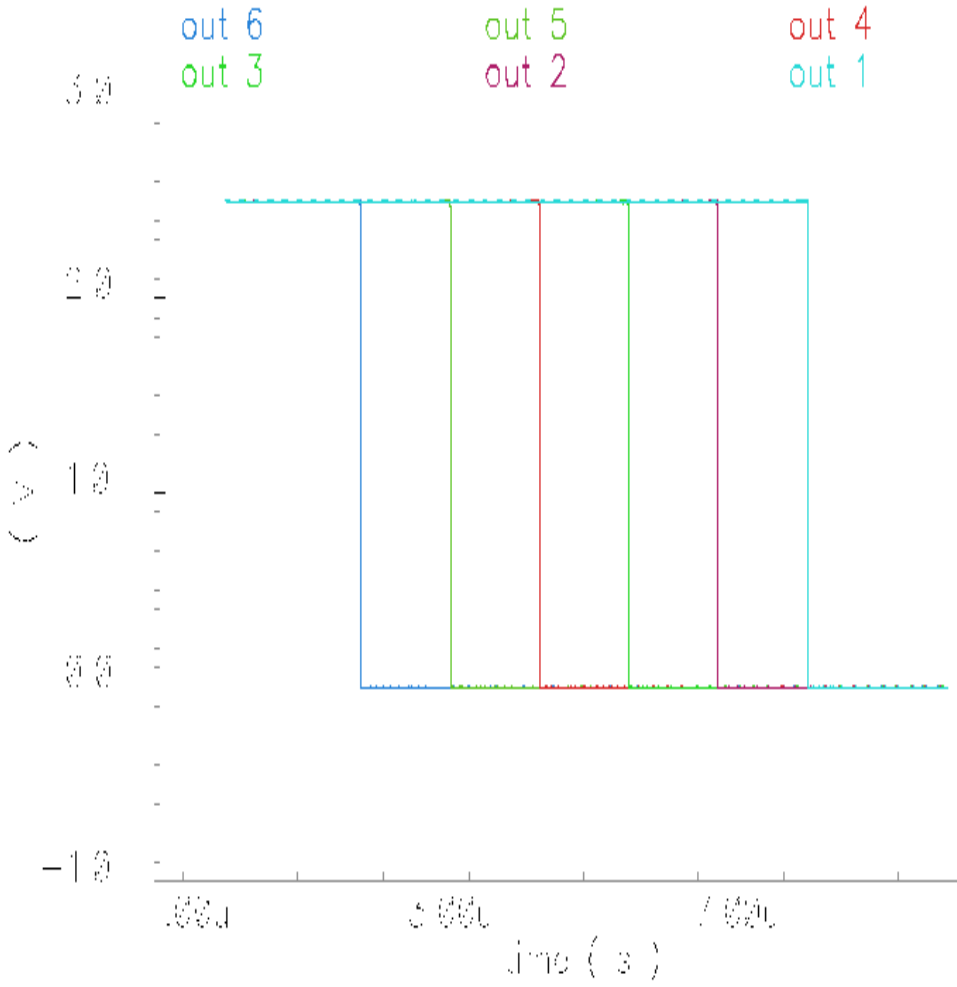


Very simple structure for the amplication, in open-loop.

A current DAC is used instead of a voltage DAC: very simple structure, the block works at constant current, the charge injection errors are limited and it eliminates the voltage dynamic problems.

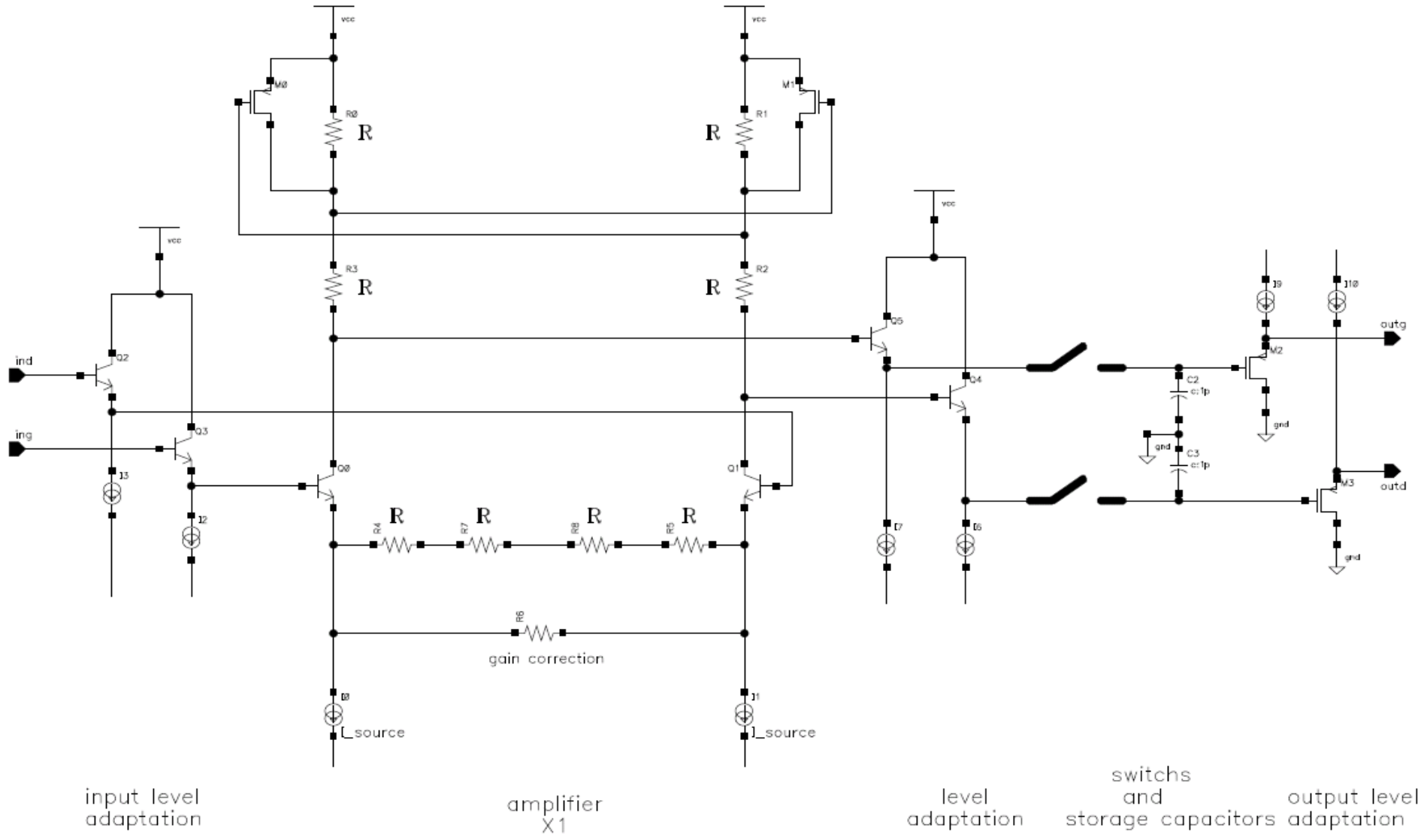
Some results





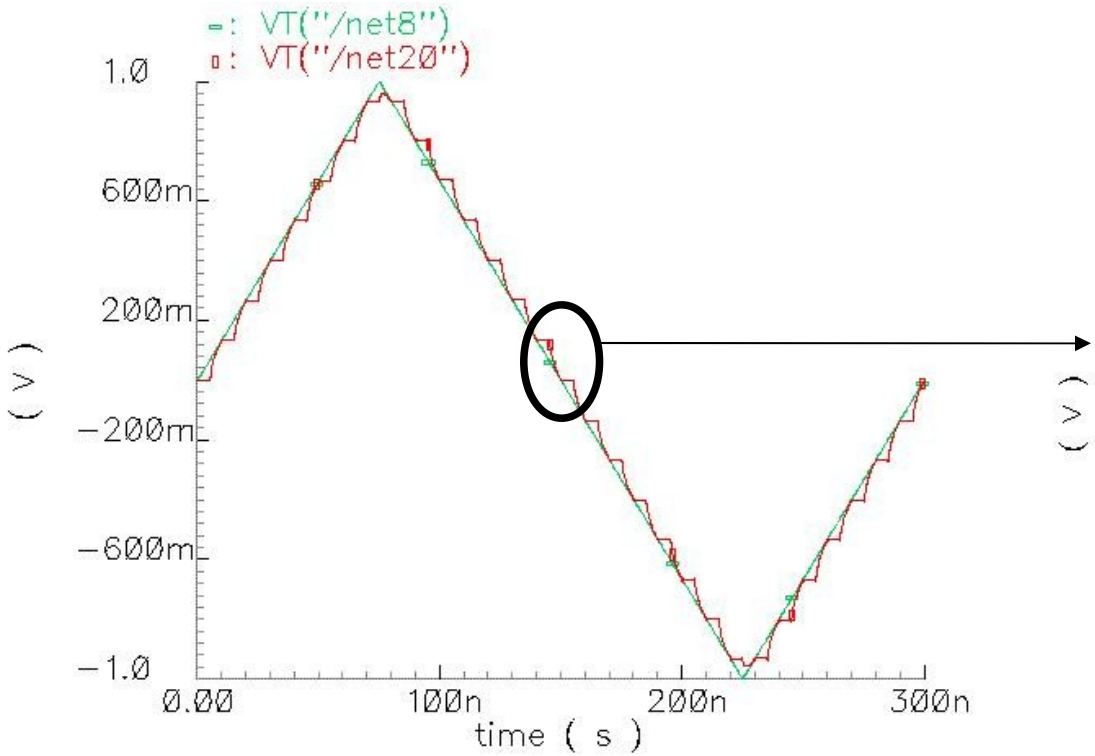
Successive subtractions

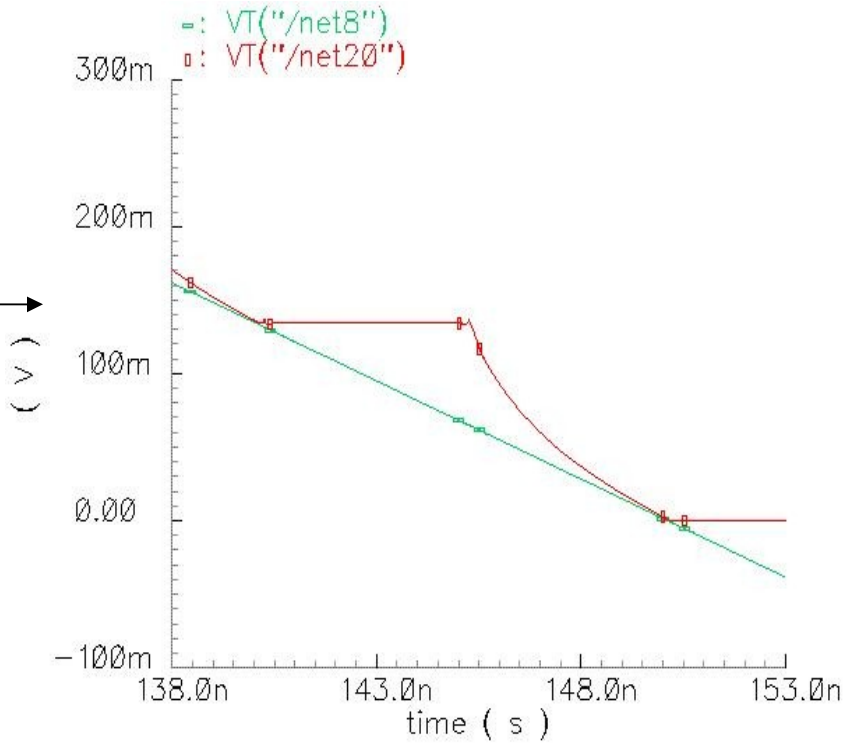
Track/hold


vcc
M0
R0
R
M1
R1
R
R3
R
R2
R
ind
ing
Q2
Q3
Q0
Q1
Q5
Q4
I3
I2
R4
R7
R8
R5
R
R
R
R
R6
gain correction
I0
I1
I_source
I_source
I7
I6
C2
c:1p
C3
c:1p
gnd
I9
I10
M2
M3
outg
outd
input level adaptation
amplifier X1
level adaptation
switchs and storage capacitors
output level adaptation

Track/hold

Simulations results:

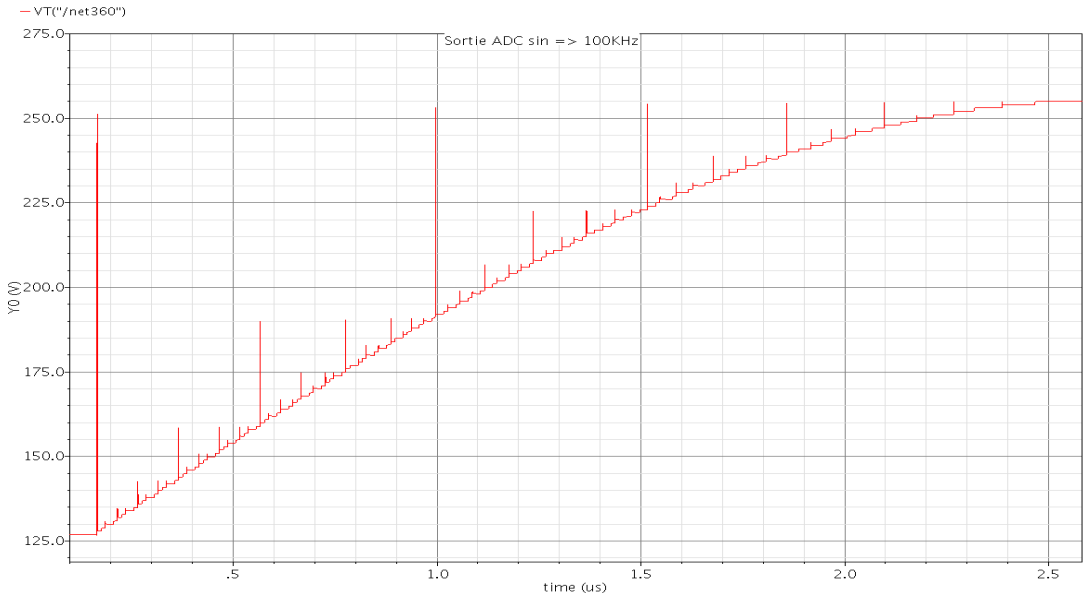




Structure contributions

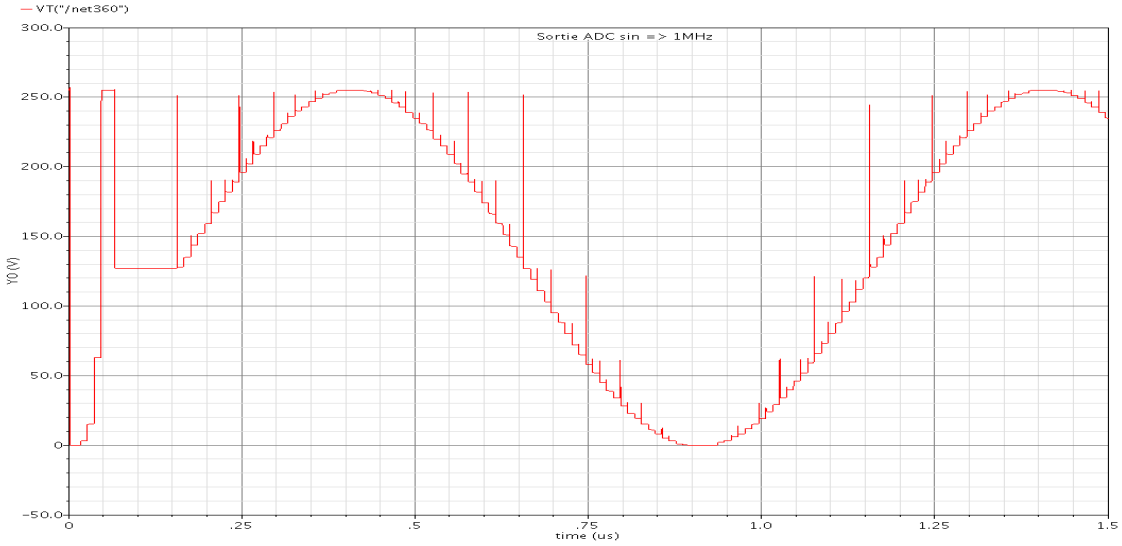
Voltage driven	Current driven
6 Voltage references in input	Only 1 Current source
All kick back noise acting on the same pair	Kick back noise absorption in six differentia pairs and in a low impedance
Resistor ladder needs «important» supply voltage	Supply voltage less critical
Linearity needed in each point of differential ladder	Linearity needed only at the comparison poi (0V)
Voltage DAC often complexe	Current DAC
Charge injection is critical	Charge injection uncritical

Results



Sinusoïde de 100KHz:

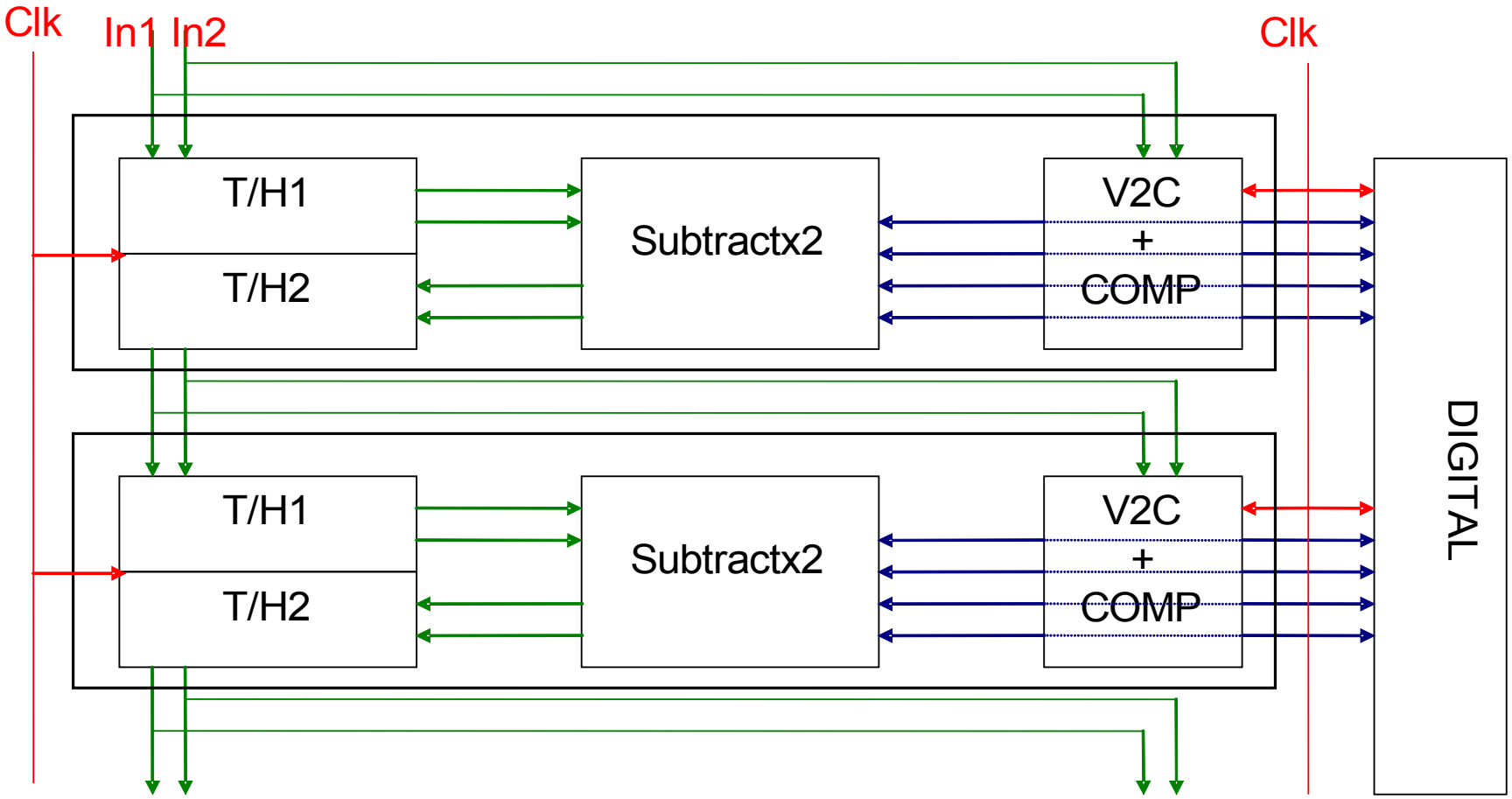
ENOB: 7.89
SINAD: 49.3dB



Sinusoïde de 1MHz:

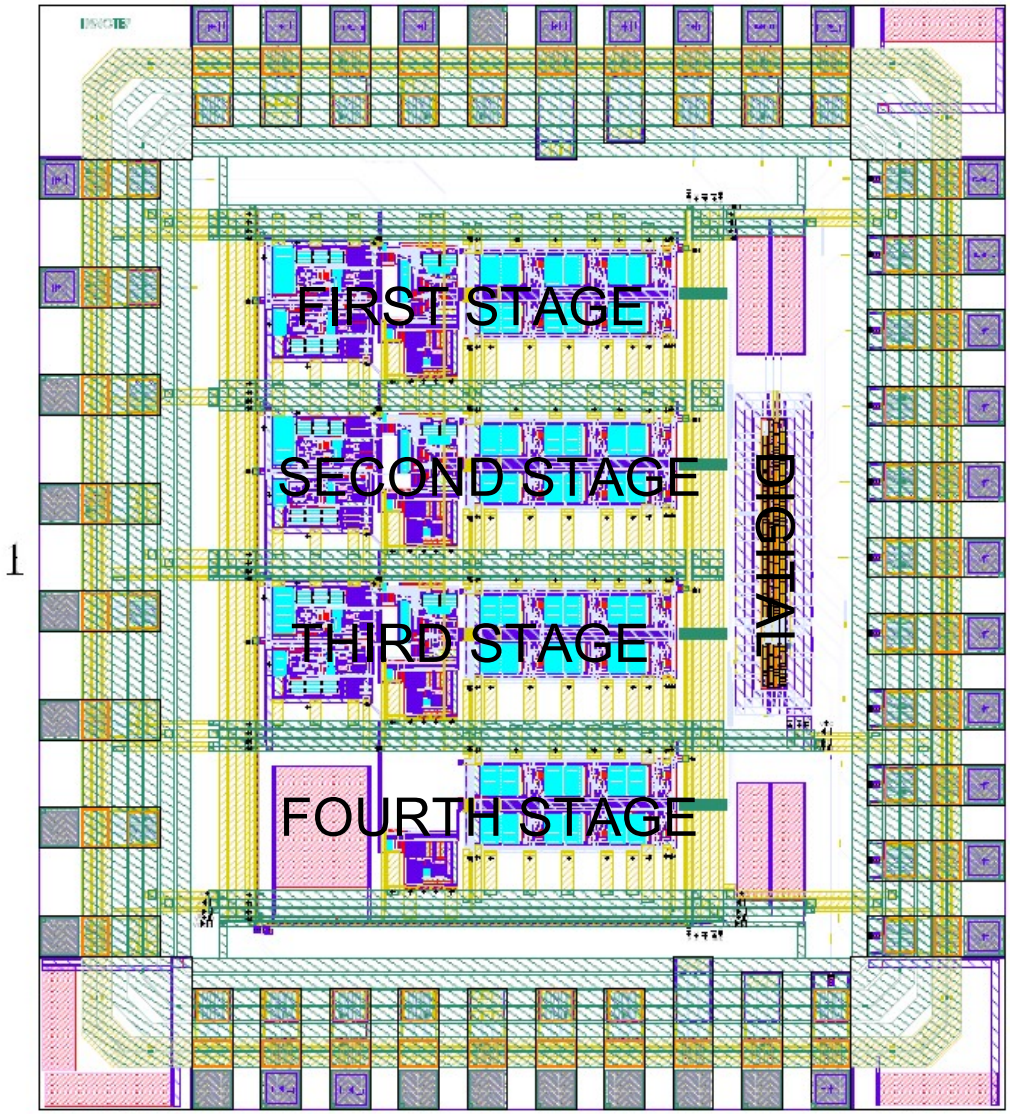
ENOB: 7.78
SINAD: 46.9dB

Layout Design



This design main ideas is to separate the most possible the analogue part from the digital part. And the clock doesn't cross the analogue signals.

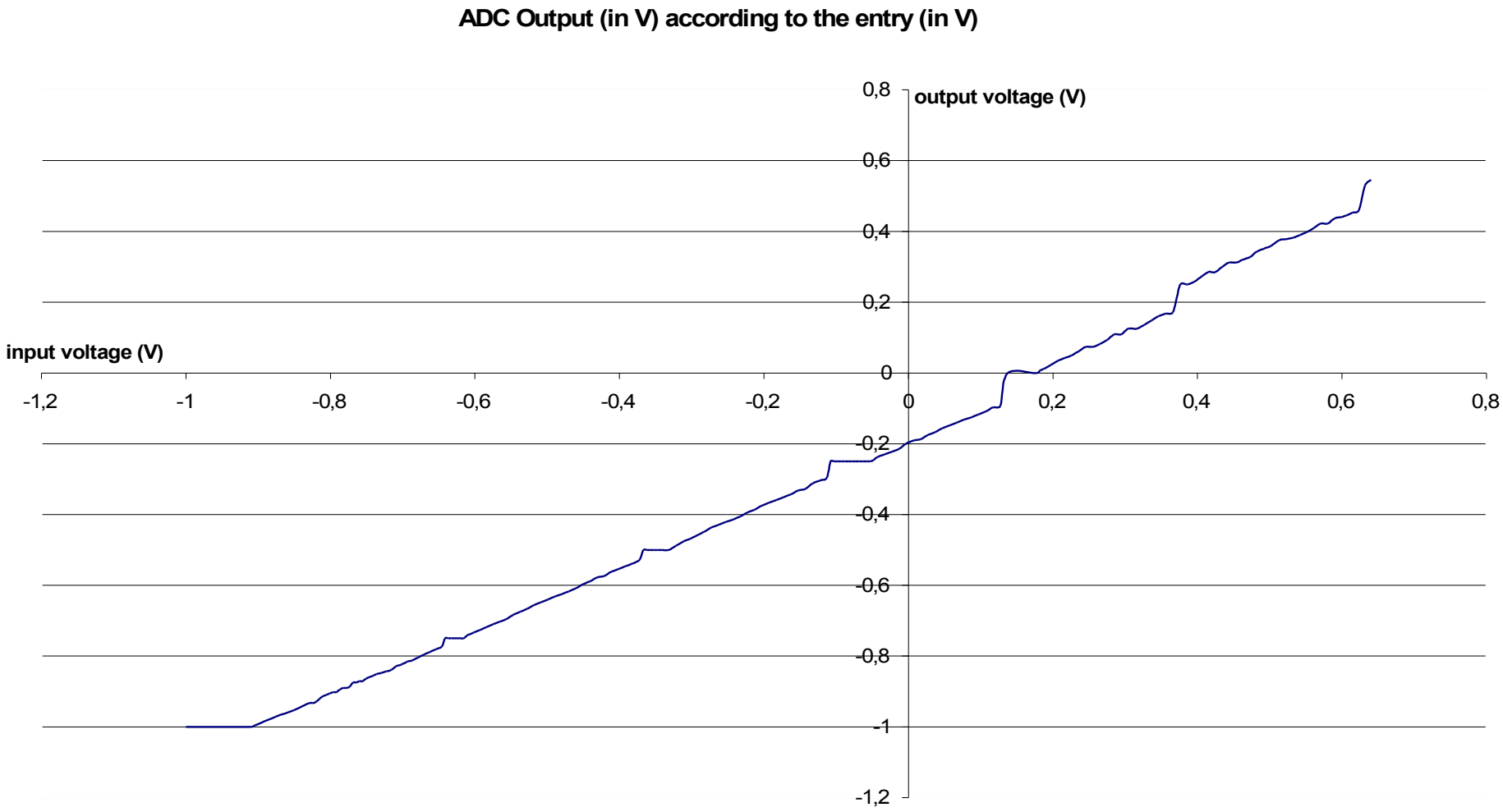
Layout Design



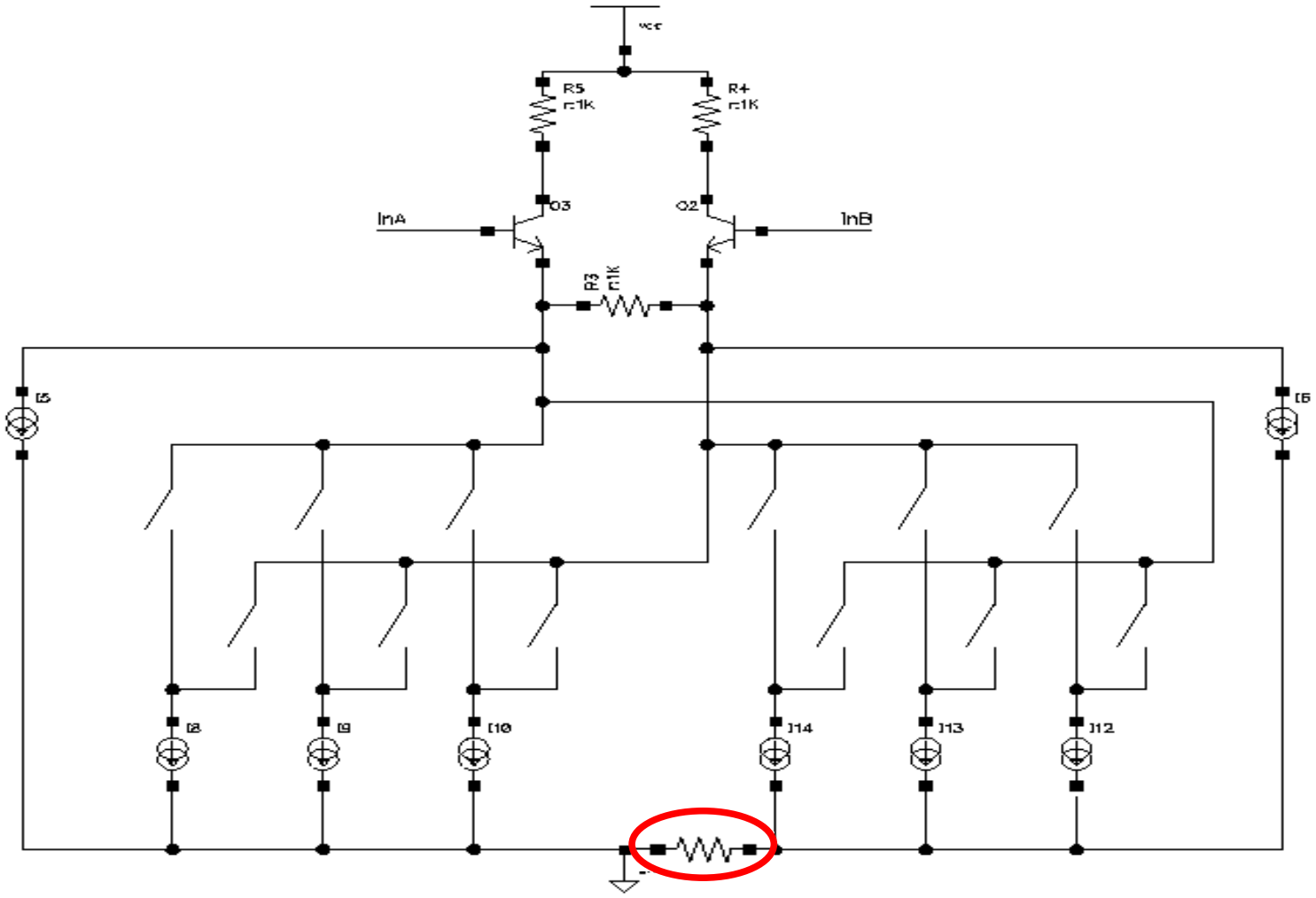
Architecture	2.5-bit/stage
Technology	0.35μm SiGe
Area	2425 µm x 2775 µm
Supply Voltage	3.5 V (Analog), 3.3 V (Digital)
Resolution	8 bits (9 bits possible)
Full Scale	2V differential
Conversion rate	100MS/s
Consumption	240mW

Chip area = 6.7 mm²

Test set up and measurements



New prototype



Conclusion

Currently, this first prototype does not respect the specifications.
The offset error have been corrected and a new prototype will be sent before the end of the year.

This first prototype give us some satisfactions:
It works at 100MHz
Current driven blocks works perfectly (comparison levels errors < 1 LSB)
The yield seems to be good