

# Electronics for HL-LHC

## Challenges and Outlook

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## Thanks and Disclaimer

- I'd like to thank my colleagues from ATLAS and CMS who provided most of the material presented
  - References and acknowledgements on the last slide
- Only the front-end electronics will be presented
  - Because of lack of time
  - Despite the very challenging electronics systems to be developed for the back-end electronics (in particular for the track trigger)
- All presented material is valid today or has been valid until recently
- It might not be valid at the start of HL-LHC...

# Outline

- 1 **HL-LHC vs LHC**
  - Impact on Radiation Hardness
  - Impact on Trigger & Data Rates
  - Summary
- 2 **Electronics Developments for Upgrades**
  - Electronics for Pixel Detector
  - Electronics for Outer Trackers
  - Electronics for Calorimeters
  - Electronics for Muon Detectors
- 3 **Common Issues and Developments**
  - IC Technologies & Radiation Hardness
  - High Speed Links
  - Power
- 4 **Summary**
  - A bit of History

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# LHC and HL-LHC Schedule

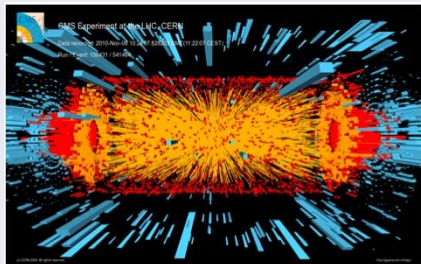
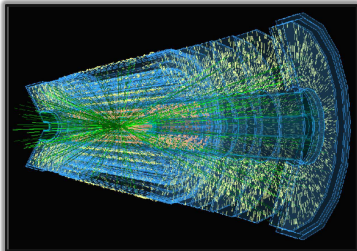


- Main points:
  - Luminosity increase
  - Physics for HL-LHC to start in September 2025
  - **10 years from now**

# Main differences between LHC and HL-LHC

## With impact on the readout electronics

	LHC	HL-LHC
Instantaneous luminosity [ $cm^{-2}.s^{-1}$ ]	$10^{34}$	$7 \cdot 10^{34}$
Number of events per BC at 25 ns	28	$\approx 200$
Number of events per BC at 50 ns	56	$\approx 400$
Integrated luminosity [ $fb^{-1}$ ]	300	3000



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# Impact on Radiation Hardness Requirements

## For Electronics

- Radiation constraints at LHC: 10 years ( $10^8$  s) at  $10^{34}$  i.e. **1000  $fb^{-1}$**
- HL-LHC: **3000  $fb^{-1}$**  i.e. 3 times more radiation (TID and NIEL)
- Electronics qualification for LHC
  - Large safety factor on the simulated values
- Safety factors can be reduced for LH-HLC
  - Good agreement simulation vs measurement

### *ATLAS safety factors for LHC and HL-LHC*

	Tracker	Elsewhere
TID	1.5 / <b>1.5</b>	3.5 / <b>1.5</b>
NIEL	5 / <b>1.5</b>	5 / <b>2</b>
ratio HL-LHC/LHC for TID	<b>3</b>	<b>1.3</b>
ratio HL-LHC/LHC for NIEL	<b>0.9</b>	<b>1.2</b>

# Impact on Radiation Hardness Requirements

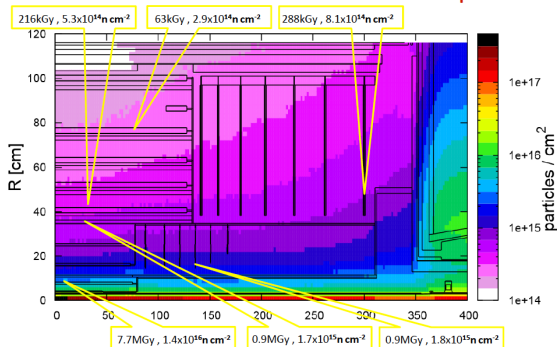
## Outside Tracker

Small increase (20–30%) of  
radiation constraints

## Tracker

$\approx 10$  MGy  
 $\approx 10^{16}$  1MeV.n.cm<sup>-2</sup>

## ITk - Radiation Fluences : 1 MeV n<sub>eq</sub>.cm<sup>-2</sup>



Simulations with FLUKA to 3,000 fb<sup>-1</sup>

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# Impact on Event Size

## High Event Multiplicity

### New tracker for both ATLAS and CMS

Higher granularity

- e.g. silicon strips 2.5 and 5 *cm* vs  $O(10 \text{ cm})$

Higher number of channels

- e.g. in CMS outer tracker  $O(250 \text{ Mch})$  vs 9.3 *Mch*

And occupancy per channel similar to current one

Rest of the detector (almost) unchanged

But higher occupancy leads to higher event size

Event size  $O(5 \text{ MB})$  vs 1–2 *MB*

# Impact on Trigger Rate

Current L1 trigger in ATLAS and CMS based on calorimeters and muon spectrometers only

- 100 kHz rate
- 2.5/3.2  $\mu\text{s}$  latency (ATLAS/CMS)

Maintaining current physics sensitivity at HL-LHC very challenging for the trigger

- Cannot increase  $p_T$  threshold
- Background from pileup reduces capabilities
  - Isolation more difficult
  - Jet  $p_T$  and missing  $E_T$  impacted



# Expected Trigger Rates

## Trigger improvements for HL-LHC

- Using higher granularity for calorimeter trigger
- Using muon precision chambers to improve  $p_T$  cuts
- Using tracking information

## ATLAS

- L0 (calorimeter and muon)
  - 1 MHz and 6–10  $\mu s$
- L1 including tracking
  - 400 kHz and 30–60  $\mu s$

## CMS

- L1 (calorimeter, muon and tracking)
  - 750 kHz and 12.8  $\mu s$

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## High radiation in the trackers

- Up to 10 *MGy* and  $2 \cdot 10^{16} \text{ 1MeV.n.cm}^2$

## Large event size

- Order of 5 *MB*

## High trigger rate

- Up to 1 *MHz*

## Large amount of data to handle

- Up to 5 *PB.s*<sup>-1</sup>

## Common challenges for the electronics of ATLAS and CMS

- Radiation hard IC technology
- High speed links
- Low power design and efficient power distribution

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# New Trackers for ATLAS and CMS

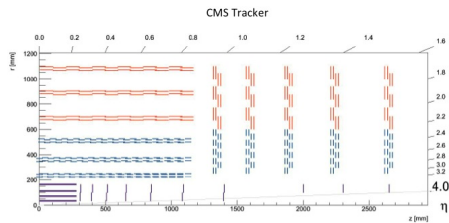
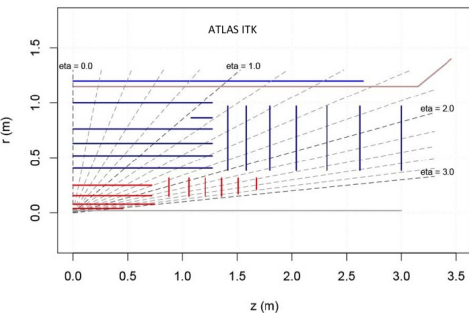
## ATLAS

- Silicon tracker
- Pixel detector
  - 4 barrel layers
  - 6 end-cap disks
  - pixel size  
25x150 and 50x250  $\mu m^2$
  - 8.2  $m^2$  / 638 *Mch*
- Strip detector
  - 5 and 2.5 *cm* strips
  - 5(+ 1 stub) barrel layers
  - 7 end-cap disks
  - 193  $m^2$  / 74 *Mch*

## CMS

- Silicon tracker
- Pixel detector
  - 4 barrel layers
  - up to 10 end-cap disks
  - pixel size  
50x50 or 25x100  $\mu m^2$
  - 4  $m^2$  / O(1 *Gch*)
- Outer tracker
  - 6 barrel layers
  - 7 end-cap disks
  - Strips and pixels-strips
  - 210  $m^2$  / 250 *Mch*

# Trackers Layouts



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# Main Challenges

## Environment

- High radiation levels. Up to **1 Grad** &  **$2 \cdot 10^{16} \text{ 1MeV.n.cm}^2$**
- Extreme particle flux
  - From  $200 \text{ MHz.cm}^{-2}$  in the current system to  $2 \text{ GHz.cm}^{-2}$
  - $50 \text{ kHz}$  per pixel for a  $50 \times 50 \mu\text{m}^2$  pixel

## Data rate

- Data rate  $22 \text{ Gb.s}^{-1}.\text{cm}^{-2}$  for a triggerless system
  - **$1800 \text{ Tb.s}^{-1}$**  for  $8 \text{ m}^2$  !!
- Still  $220 - 550 \text{ Mb.s}^{-1}.\text{cm}^{-2}$  for a  $0.4 - 1 \text{ MHz}$  readout rate

## ATLAS-CMS common effort

### RD53 collaboration



# RD53: ATLAS – CMS Collaboration

- About 20 institutes and 100 collaborators (50% chip designers)
- 6 Working Groups
  - WG1: Radiation tests and qualification
  - WG2: Top level
  - WG3: Simulation/verification framework
  - WG4: I/O
  - WG5: Analog front-end design
  - WG6: IP blocks
- RD53 web site: [www.cern.ch/RD53/](http://www.cern.ch/RD53/)

Design of a prototype chip in 65 nm technology

Availability in 2016

# RD53 Critical Issues

Establish guidelines for radiation hardness of the selected 65 nm technology to 1 Grad

- Or decide the process cannot be used to this level

Develop tools and methodology adequate for  $5 \times 10^8$  transistors mixed signal chip in this technology

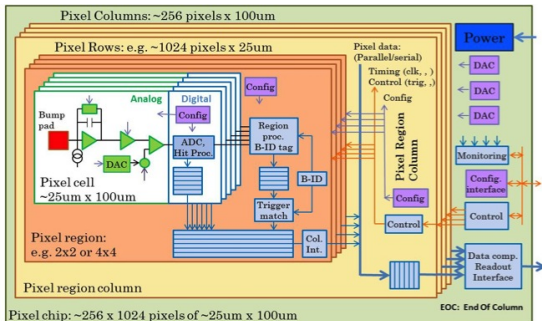
Define pixel size and low threshold operation strategy

- $50 \times 50 \mu\text{m}^2$  chip pixels (sensor aspect ratio can vary)

Develop high bandwidth readout ( $2 - 4 \text{ Gb.s}^{-1}$  / chip) including cable transmission models

# Chip Architecture

- Pixel  $50 \times 50$  or  $25 \times 100 \mu m^2$
- 256 *kchannels* per chip
- Trigger latency  $O(10 \mu s)$
- Trigger rate up to 2 MHz
- Charge digitization (ToT or ADC)
- Buffering within the pixel region
- Data compression at the end of column
- 95% digital chip (as FEI4)
- Output links @  $1 - 4 Gb.s^{-1}$



## Readout Links

Optical devices not radiation hard enough to be installed close to the pixel chips

- Need for a few meters electrical transmission
- Need very low mass cables

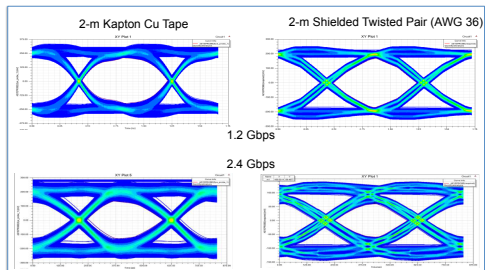
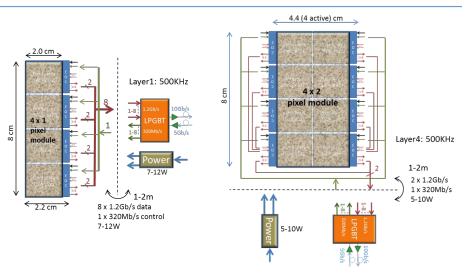
One chip handles 256 *kchannels* and covers  $O(6 \text{ cm}^2)$

- Readout bandwidth  $1 - 4 \text{ Gb.s}^{-1}$
- Aim at electrical links @  $1.2 \text{ Gb.s}^{-1}$

Some measurements

- Twinax cables  $4 - 6 \text{ Gb.s}^{-1}$  over 4 *m*
- PSI very low mass twisted pair:  $400 \text{ Mb.s}^{-1}$  over 1 *m*

# Example: CMS Modules



- Inner barrel layer 4x1 module
- Outer barrel layer 4x2 module

- Trigger rate 500 kHz to 1 MHz
- Output links @ 1.2 or 2.4 Gb.s<sup>-1</sup> with pre-emphasis

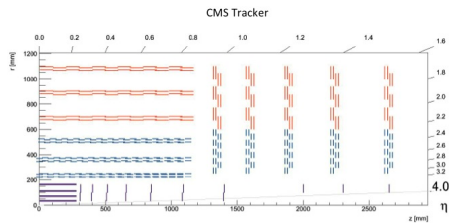
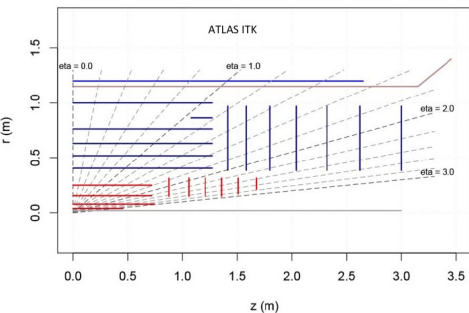
# Pixel ASIC Generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2: HL-LHC
Pixel size	100x150 $\mu\text{m}^2$ (CMS) 50x400 $\mu\text{m}^2$ (ATLAS)	100x150 $\mu\text{m}^2$ (CMS) 50x250 $\mu\text{m}^2$ (ATLAS)	$\sim 50 \times 50 \mu\text{m}^2$
Sensor	2D, $\sim 300 \mu\text{m}$	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, HVCMOS ?
Chip size	7.5x10.5mm $^2$ (ATLAS) 8x10mm $^2$ (CMS)	20x20mm $^2$ (ATLAS) 8x10mm $^2$ (CMS)	<b>&gt; 20 x 20 mm<math>^2</math></b>
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	<b><math>\sim 1\text{G}</math></b>
Hit rate	<b>100MHz/cm<math>^2</math></b>	<b>400MHz/cm<math>^2</math></b>	<b>1-2 GHz/cm<math>^2</math></b>
Trigger rate	100kHz	100kHz	200kHz - <b>1MHz</b>
Trigger latency	2.5 $\mu\text{s}$ (ATLAS) 3.2 $\mu\text{s}$ (CMS)	2.5 $\mu\text{s}$ (ATLAS) 3.2 $\mu\text{s}$ (CMS)	<b>6 - 20<math>\mu\text{s}</math></b>
Hit memory per chip	0.1Mb	1Mb	$\sim 16\text{Mb}$ ( <b>160x</b> )
Readout rate	40Mb/s	320Mb/s	<b>1-4Gb/s (100x)</b>
Radiation	<b>100Mrad</b>	<b>200Mrad</b>	<b>1Grad</b>
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	<b>65nm</b>
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	<b>Digital</b>
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	<b>In Pixel buffering</b>
Power	$\sim 1/4$ W/cm $^2$	$\sim 1/4$ W/cm $^2$	<b>1/2 - 1 W/cm<math>^2</math></b>

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# Trackers Layouts





# Main Challenges

## Environment

- Radiation level up to  $O(100) \text{ Mrad}$  &  $10^{15} \text{ 1MeV.n.cm}^2$

## Data rate

- Data rate  $O(10 \text{ Tb.s}^{-1})$ 
  - Readout @ L1 (or L0) rate
  - Outer tracker part of the L1 trigger. Trigger data:
    - @ 40 MHz for a self seeded trigger
    - @ L0 rate for a region of interest (RoI) based trigger

## Large differences between ATLAS and CMS

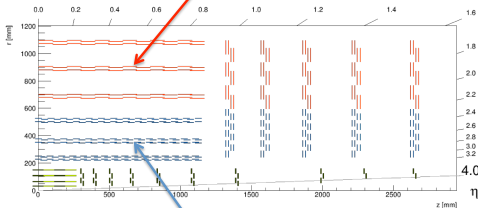
- Mainly for the trigger part

# CMS Outer Tracker

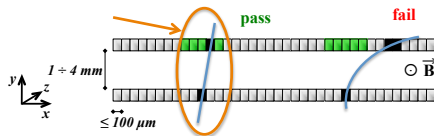
## Two types of modules

- Strip/Strip modules
- Macro-Pixel/Strip modules
- Both participating in the trigger

8400 Strip/Strip Modules



7100 Macro-Pixel/Strip Modules

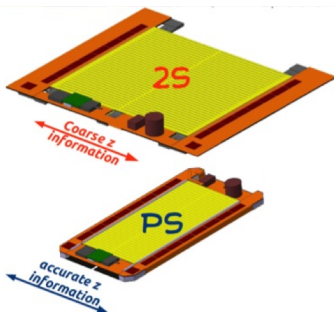


# CMS Outer Tracker Modules

Each module is an independant block with its own services

## 2 Strip sensors

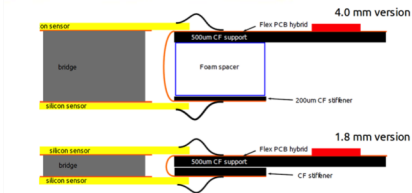
**Strips:**  $5\text{ cm} \times 90\ \mu\text{m}$   
**Strips:**  $5\text{ cm} \times 90\ \mu\text{m}$   
 $P = 2.7\text{ W}$   
 $\sim 92\text{ cm}^2$  active area  
 For  $r > 40\text{ cm}$



## Pixel + Strip sensors

**Strips:**  $2.5\text{ cm} \times 100\ \mu\text{m}$   
**Pixels:**  $1.5\text{ mm} \times 100\ \mu\text{m}$   
 $P = 5.0\text{ W}$   
 $\sim 44\text{ cm}^2$  active area  
 For  $r > 20\text{ cm}$

## 2S Modules

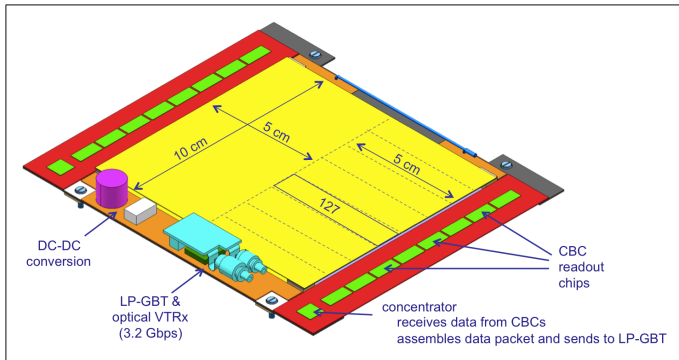


## PS Modules

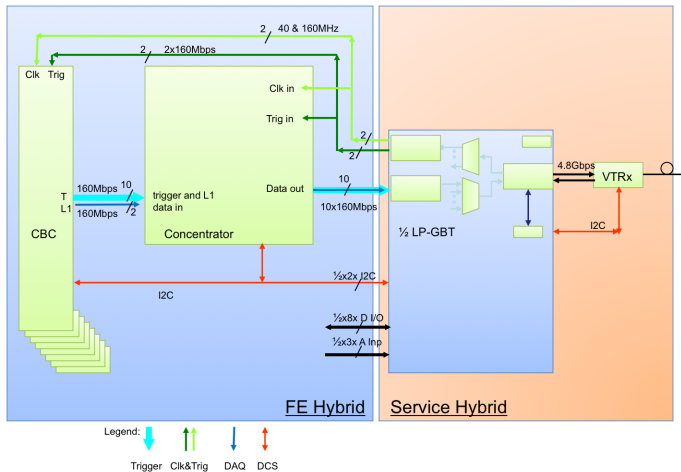


# CMS 2S Modules

- 254-ch readout chip: CBC
- Concentrator ASIC
- 130 and 65 *nm* CMOS
- C4 technology (no bonding)
  - High density hybrid required

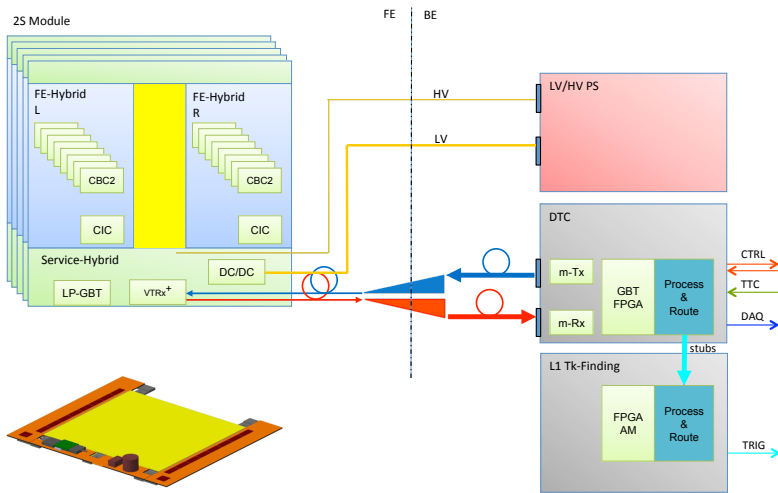


## Simplified Block Diagram



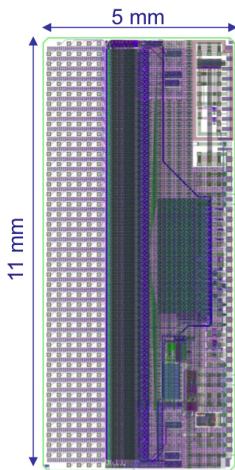
**3.2 Gb.s<sup>-1</sup> per module**

# Simplified Overall Block Diagram

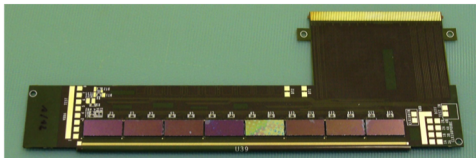
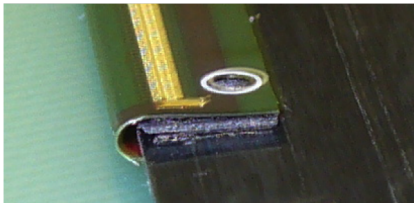
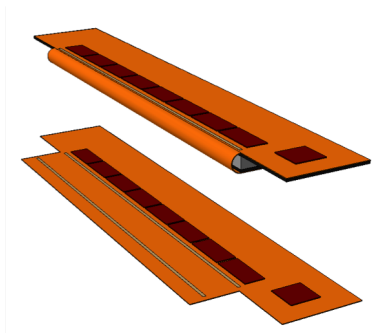
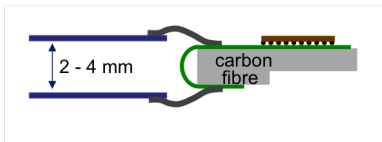


# CMS CBC ASIC

- 254 channels in 130 *nm* CMOS
- Front end designed for up to 5 *cm* strips
  - 1000  $e^-$  *rms* noise
- DC coupled, both sensor polarities
- Binary unparsified readout
- Pipeline length 6.4  $\mu s$
- Bump-bond layout
  - C4 bump-bond layout, 250  $\mu m$  pitch
  - 19 columns x 43 rows
- Includes triggering features
  - 30 interchip signals (15 in, 15 out)
  - top and bottom
- 350  $\mu W$  per channel



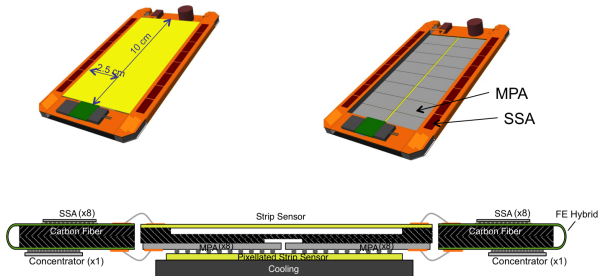
# CMS 2S Hybrid Development





# CMS PS Modules

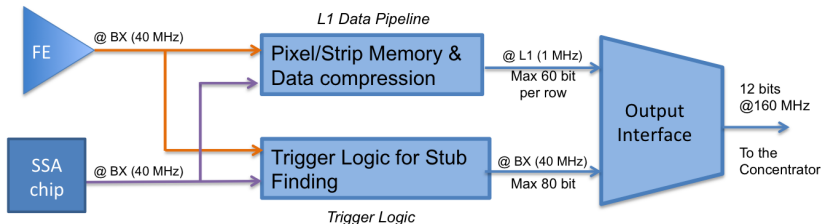
- 3 ASICs in 65 nm CMOS
  - SSA, MPA & Concentrator
- 120 strips per SSA
  - 100  $\mu\text{m}$  strip pitch
- 120 strips and 16 x 120 pixels per MPA
  - Pixel size: 100 x 1446  $\mu\text{m}^2$



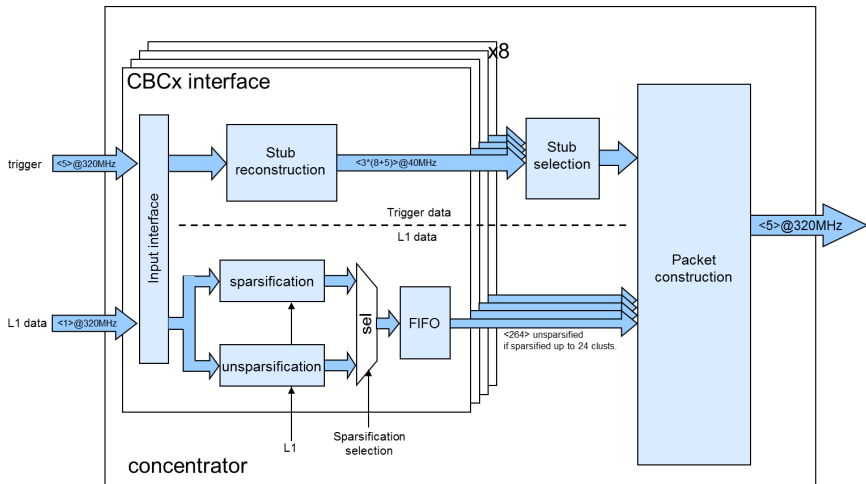
# MPA Readout Data Flow

Input each 25 ns (40 MHz):

- Pixel hits from Front- End: 120 columns x 16 rows = 1920 hits
- Strip hits from SSA chip: 120 hits



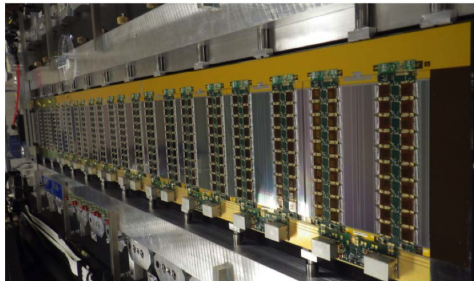
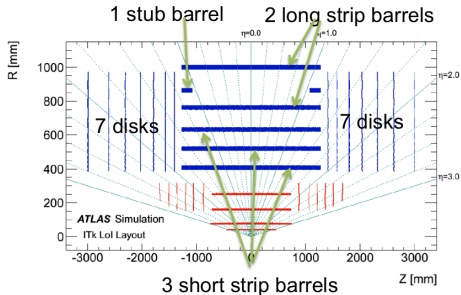
## 2S and PS Concentrator ASIC



# ATLAS Outer Tracker

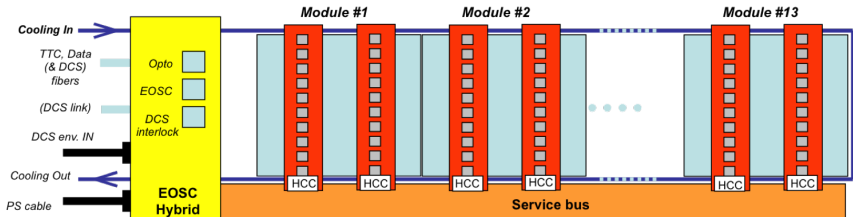
## Two types of modules

- Short strip modules
- Long strip modules
- Organised in double-sided staves with stereo angle



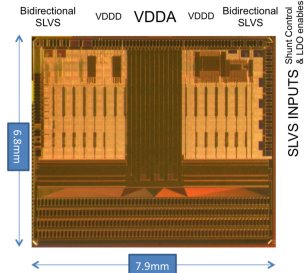
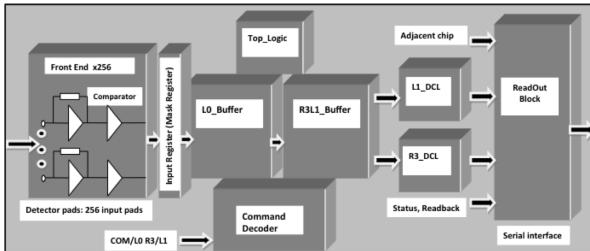
# ATLAS Stave Readout: current prototype

- Two ASICs in 130 *nm* CMOS
  - ABC130 and HCC
- Region of Interest concept
  - L0 (400 *kHz*) delivers region of interest
  - About 10% of the tracker data to be readout for L1 decision
  - L1 (200 *kHz*) used for complete readout
- Buffers in the front-end
  - L0 pipeline (6.4  $\mu\text{s}$ )
  - L1 buffer storing up to 256 events after L0 until L1
- Serial links (e-link) between the HCC's and the End of Stave GBT
  - 160  $\text{Mb}\cdot\text{s}^{-1}$  HCC to EOS
  - 4.2  $\text{Gb}\cdot\text{s}^{-1}$  for the stave



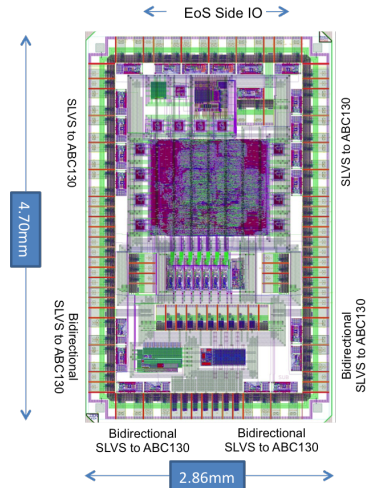
## ABC130

- 256-channel 130 nm CMOS
- Pad frame optimized for hybrid mass reduction
  - Direct sensor bonding
  - All power bonds at back edge
- Support Serial Powering
- 2-level trigger architecture
  - L0 (400 kHz) - L1 (200 kHz)
  - Data retrieved from buffer using L0ID tag
- Programmable LDOs for analogue / digital power



# Hybrid Controller Chip (HCC)

- 130 nm CMOS
- Interfaces between the ABC130s and the EOS card via the stave bus cable
  - SLVS @  $160 \text{ Mb.s}^{-1}$
- Programmable delays to time the ABC130
- Prioritization between RoI and readout data



## Next Steps for the ATLAS Tracker

### New requirements

- New trigger rates: L0 @ 1 MHz, L1 @ 400 kHz and 10% of modules to be part of RoI
  - Equivalent to a full readout @ 500 kHz
- L0 latency up to 10  $\mu$ s, L1 latency up to 60  $\mu$ s

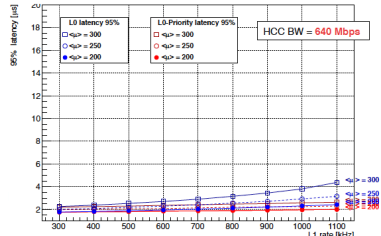
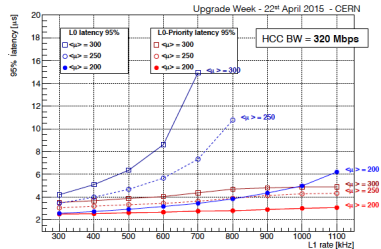
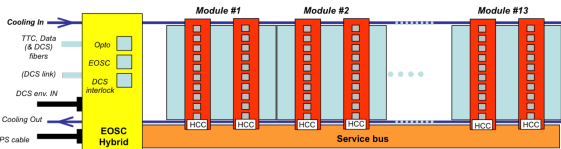
### Next version (being designed)

- Possibility to fully read out at 1 MHz L0
- L1 buffer kept as backup
- "Express" readout for RoI data



# ATLAS Stave Readout: next steps

- Latency is an issue
  - Getting the data for L1 processing
- L0 pipeline ( $12.8 \mu\text{s}$ )
- L1 buffer as back-up
- Serial links (e-link) between the HCC's and the End of Stave GBT
  - $640 \text{ Mb.s}^{-1}$  HCC to EOS
  - $16.6 \text{ Gb.s}^{-1}$  for the stave



# Upgrades of the Calorimeters and Muon Detectors

## No full detector replacement as for the trackers

- Two exceptions:
  - New muon chambers in the end-caps
    - $\mu$ megas and sTGC for ATLAS
    - GEM for CMS
  - New CMS end-cap calorimeter

## Replacement of most of the readout electronics

- Except for some muon chambers

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  - **Electronics for Calorimeters**
  - Electronics for Muon Detectors
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# Upgrade of the Calorimeters Readout Electronics

## Optimisation of the front-end for high pile-up

VFE of CMS Barrel Ecal

ATLAS LAr and Tile calorimeters preamplifier-shaper

ASICs in 130 *nm* CMOS and in SiGe

## Readout @ 40 MHz

Availability of the complete data in the back-end electronics

Simplification of the front-end architecture

Opens some possibilities for future trigger algorithms

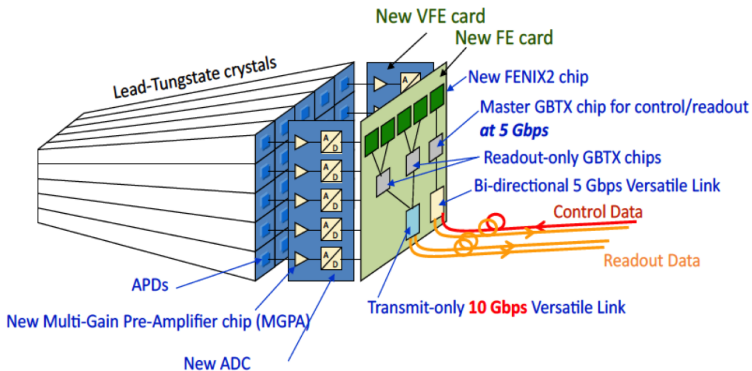
Need for a low power **16-bit – 11-bit ENOB ADC** per channel

Need for **very high bandwidth** links

# CMS ECAL Barrel Upgrade

## Module readout

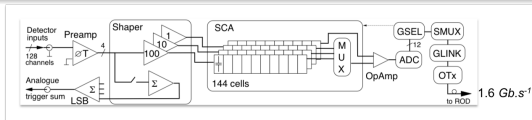
3 readout links @  $5 \text{ Gb.s}^{-1}$  to be compared to  
2 links @  $800 \text{ Mb.s}^{-1}$  in the current system



# ATLAS LAr Calorimeter Upgrade

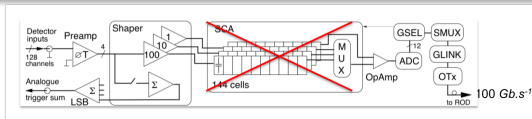
## Current front-end board

Analog to digital conversion of the 128 channels after L1  
1 readout link @  $1.6 \text{ Gb.s}^{-1}$  per FEB



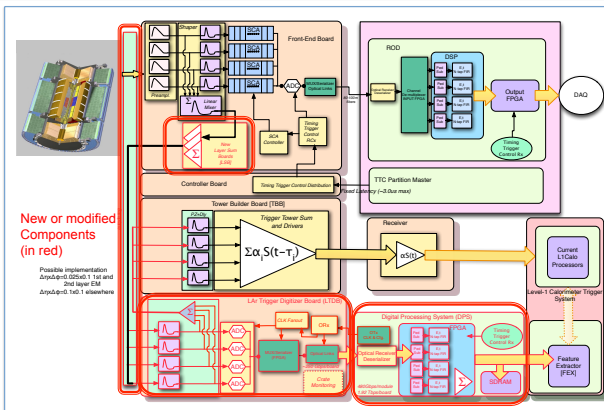
## Upgraded front-end board

Analog to digital conversion of the 128 channels @  $40 \text{ MHz}$   
 $O(100 \text{ Gb.s}^{-1})$  per FEB



# Intermediate Step for the ATLAS LAr Calorimeter

## Level-1 Trigger Upgrade for Phase-1



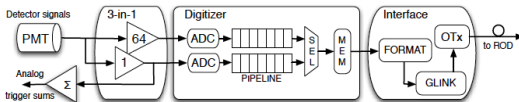
Trigger sum using higher granularity

Analog to digital conversion of up to 320 channels @ 40 MHz

# ATLAS Tile Calorimeter Upgrade

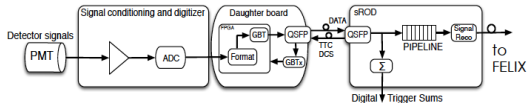
## Current readout

Analog to digital conversion after L1  
 512 links @  $0.64 \text{ Gb.s}^{-1}$



## Upgraded readout

Analog to digital conversion @  $40 \text{ MHz}$   
 8192 links @  $10 \text{ Gb.s}^{-1}$





# Developments for the Calorimeters

## Amplifiers-Shapers

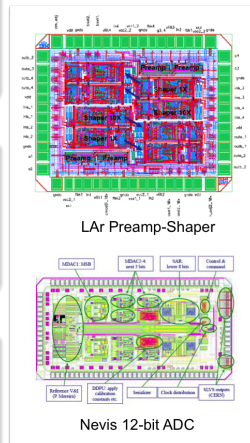
In 130 *nm* CMOS for the ATLAS Tile  
Two SiGe versions for the ATLAS LAr

## ADCs

Several 12-bit 40 *MHz* ADC for the ATLAS Tile and  
LAr (130 *nm* CMOS)  
Assuming a readout based on a multigain shaper

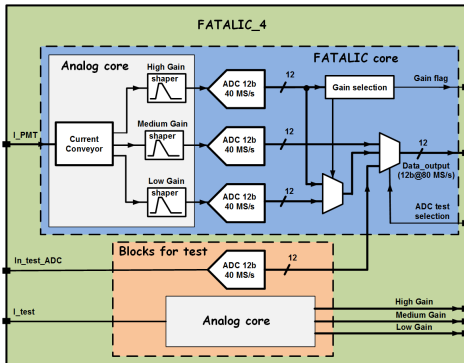
## Serialisers and Links

Alternatives to the GBT and the Versatile Links  
being studied  
Including optical modulators

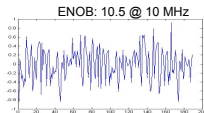


# Specific Development for the ATLAS Tile Calorimeter

- 3 options for the front-end
  - Replica of existing (3in1 board)
  - QIE chip (Fermilab-Argonne)
  - FATALIC ASIC
- FATALIC 130 nm CMOS
- Pre-amplifier-shaper 3 gains
- 3 12-b ADC



Gains	Dynamic range	LSB	Noise (rms)	Linearity error	Peaking time fluctuation
High	up to 14 pC	3.4 fC	0.05% → 7 fC	$< \pm 0.1\%$	$< 1\text{ ns}$
Medium	up to 140 pC	34 fC	0.05%		$< 0.5\text{ ns}$
Low	up to 1200 pC	300 fC	0.05%	$< \pm 1\%$	



## Possible (Highly Desirable) Common Developments

Very similar requirements for the calorimeters

Preamplifier-Shaper specific to each type  
ADC, serialisers and links could be the same

Possible common developments

IP block for a 16-bit, 11–12 ENOB, 40 *MHz* ADC  
IP block for a fast serialiser  
IP block for a laser driver

Special ASIC for each calorimeter

Integrating a number of the previous blocks

# CMS End-Cap High Granularity Calorimeter

## Electromagnetic Calorimeter

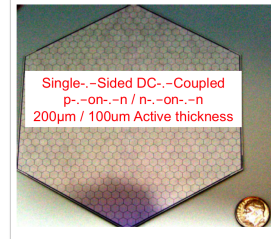
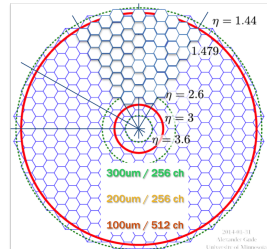
30 samplings of lead/copper – silicon  
420  $m^2$  of silicon pad detectors  
3.7 *Mchannels*

## Front Hadronic Calorimeter

12 layers of brass – silicon  
250  $m^2$  of silicon pad detector  
1.4 *Mchannels*

## Radiation levels

Up to  $10^{16}$   $1\text{MeV}\cdot\text{n}\cdot\text{cm}^{-2}$  & several *MGy*



# Electronics Challenges for HGC

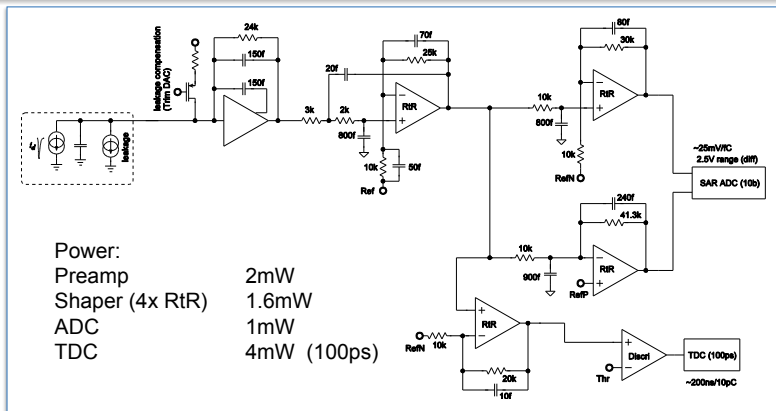
## Requirements

- 5.1 *Mchannels*
- Detector capacitance 40 – 60 *pF*
- Detector leakage up to 10.5  $\mu A$
- ENC below 2500e
- Peaking time 15 – 20 *ns*
- Dynamic range up to 10pC
- Digitisation @ 40 *MHz*
  - Resolution 8 – 10 *bit*
- Time measurement (100 *ps*)
- Less than 15 *mW/channel*

## Proposed Architecture

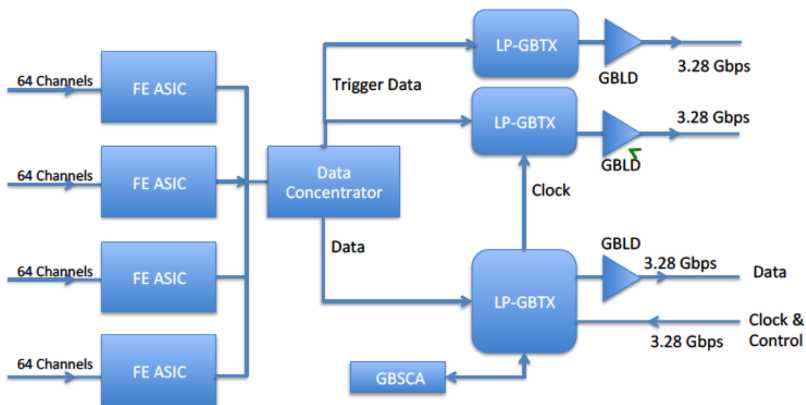
- Preamplifier/shaper with TOT measurement for high charges
- 22 *ns* peaking time
- Gain 25 *mV/fC*, 2.5 *V* range
- Linear range 100 *fC*
- Above 80 *fC* information from TOT

# HGC: Possible Front-end Block Diagram



- TDC (100 ps bin) for TOT for signals above 60 fC (up to 10 pC)
- 10 bit ADC for measurement of pulses up to 100 fC

# Electronics Challenges for HGC cont



## Readout Links

- $\approx 90000$  electrical links &  $15000 \text{ } 5\text{Gb}\cdot\text{s}^{-1}$  optical links

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# Muon Detectors Upgrades

## New chambers in the end-caps

- GEM chambers in CMS
- $\mu$ egas and sTGC in ATLAS (installation during LS2)

## Electronics upgrade for some existing chambers

- Simplified front-end electronics of the CMS DT chambers
- Use of the ATLAS precision chambers in the trigger

## Maintain existing front-end for some chambers?

- Because of access difficulties (time needed)
- Severe constraints on the overall system (latency and trigger rate)

# Developments for the CMS GEM chambers

## 3 layers of GEM chambers in the end-caps

- Trigger improvement
- $O(60 \text{ kchannels})$

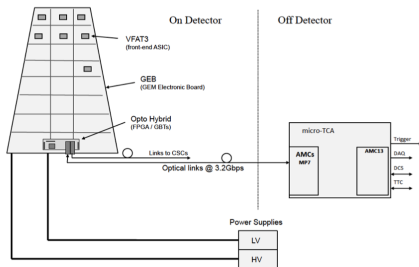
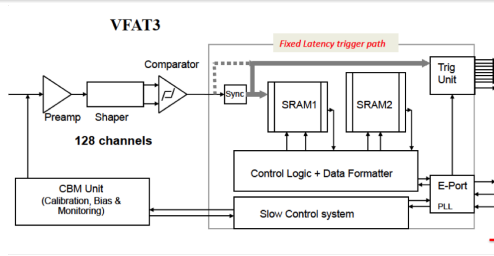
## Front-end ASIC: VFAT3

- 130 *nm* CMOS TSMC
- 128 channels
- Programmable shaping time: 25 – 400 *ns*
- Timing with CFD (no ToT)

## Readout System

Based on the GBT

# VFAT3 and Readout Simplified Block diagrams



# Developments for the ATLAS New Small Wheels

## Sandwiches of $\mu$ megas and sTGC in the end-cap NSW

- Trigger improvement to reduce high rate in the end-caps
- Both chambers participating in the trigger and readout
- $O(2.3 \text{ Mchannels})$

## Front-end ASIC: VMM

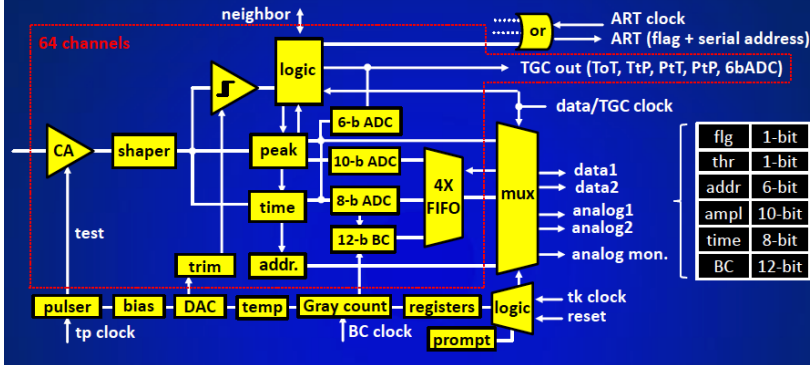
- 64-channel 130 nm CMOS ASIC
- Q meas. up to 2 pC @ < 1 fC rms
- Time meas. 100 ns @ < 1 ns rms

## Readout and Trigger Systems

Three others 130 nm CMOS ASICs

# VMM Block Diagram

## VMM2 Architecture - Complete ASIC



### Next version (VMM3)

- Including L0 pipeline and all missing digital logic

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# IC Technologies

## Used technologies

- So far most of the developments in 130 and 65 *nm* CMOS
- All developments in 130 *nm* using the IBM process
  - At the exception of VFAT3 (TSMC process to be used)

## Expected schedule

Most of the ASICs to be produced until now and 2018

## Some worries about the IBM process

- TSMC 130 *nm* tested against radiation
- Moving from IBM to TSMC is not straight forward
- Strong interest in keeping the investment on IBM
- 6-month end of life warning



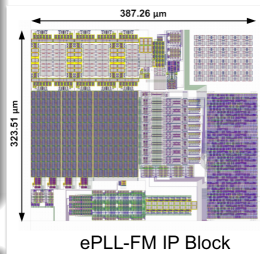
## Sharing Designs

### IP blocks

- RD53 started a full program of IP blocks development (in 65 *nm*)
- List of 30 required IPs defined
- Procedure for making IPs easily integrated into mixed signal design flow
- Repository

### Should be extended to other technologies

- Already some blocks from the GBT available
  - e.g. SLVS I/Os, ePLL-CDR, ePLL-FM, ...



# Radiation Hardness

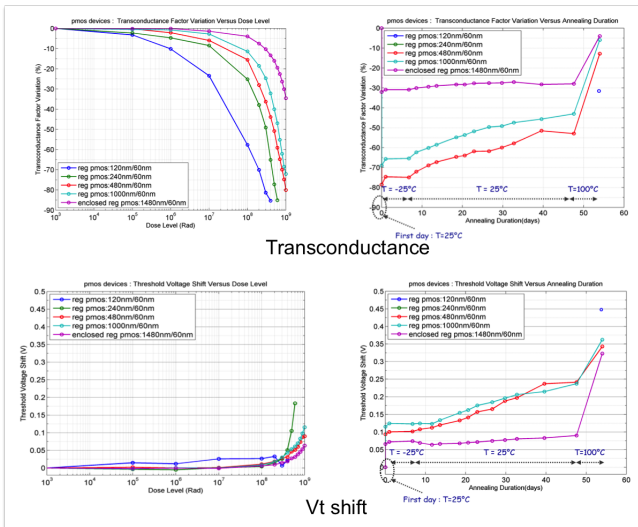
## What seems OK

- IBM 130 *nm* and TSMC 65 *nm* radiation hard enough for outer pixel layers and outer trackers
- TSMC 130 *nm* successfully measured as well for that level

## What seems not OK

- Some problems at very high dose for the 65 *nm*
- Severe issue for the inner pixel layers
  - Might require to come back to a replacement scenario for these layers
  - As it was foreseen for the current inner pixel layers

# Radiation Effect on a 65 nm PMOS Transistor



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## On-going Developments

### Serialisers-Deserialisers and Optical Links

- Several developments mentioned
- Common developments
  - GBT chipset and Versatile Link

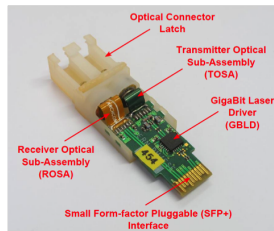
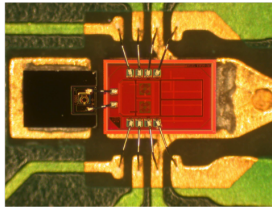
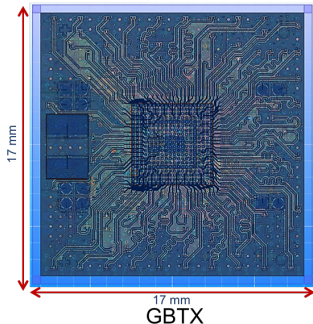
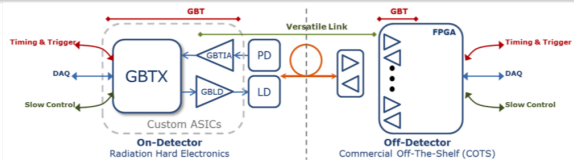
### Status of the GBT chipset

- GBTX, GBT-SCA, GBLD, GBTIA
  - $4.8 \text{ Gb.s}^{-1}$ ,  $130 \text{ nm}$
- Production to start now
- Until end of 2015

### Status of the Versatile Link

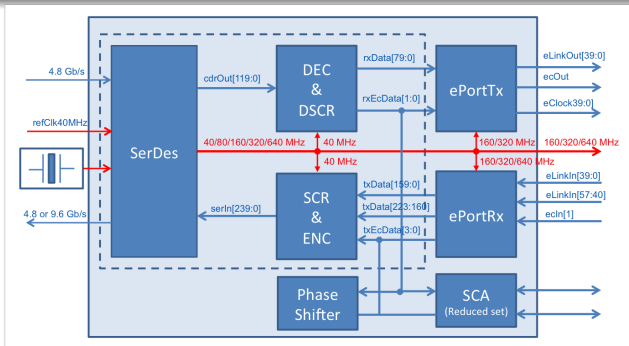
- Transceiver or dual emitter (VTRX and VTTX)
  - $5 \text{ Gb.s}^{-1}$
  - Multi- or Single-mode
- Production starting
- Until end 2016

# GBT chipset and Versatile Link



Smaller, less power hungry or faster version needed for HL-LHC

# The Low Power GBT: IpGBT



- Low power and small footprint
  - 500 mW @ 4.8 Gb.s<sup>-1</sup>
- 2.56 Gb.s<sup>-1</sup> for down links
- 5.12 Gb.s<sup>-1</sup> or 10.24 Gb.s<sup>-1</sup> for up links

- e-Links up to 640 Mb.s<sup>-1</sup> or 1.28 Gb.s<sup>-1</sup>
- Subset of the GBT-SCA
- 65 nm CMOS

## Versatile Link for HL-LHC: the VL+ Project

### Small form factor, high speed needed

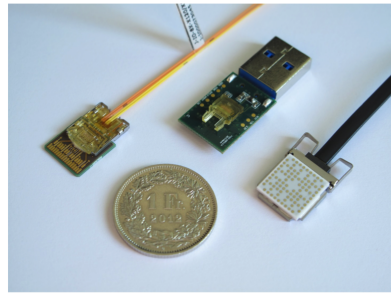
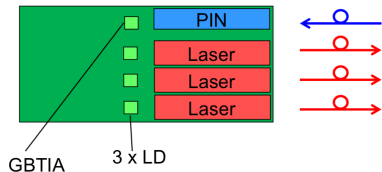
- 5/10  $Gb.s^{-1}$  up/down links
- CMS tracker modules, ATLAS EoS
- High density links for calorimeters

### High versatility

- Number of up/down links

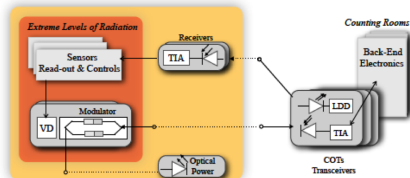
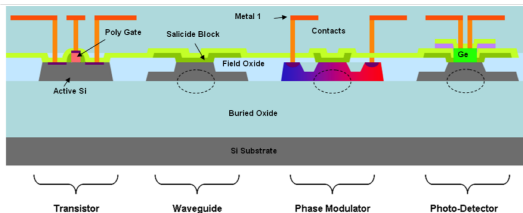
### On-going work

- 10  $Gb.s^{-1}$  tiny single/quad LD
- Package, fibres, connectors
- Feasibility study until fall 2015





# Silicon Photonics: a Dream?



- Si is an excellent optical material
- Could build a photonic circuit in a CMOS Si-wafer
- Huge potential gain
  - Power and integration

- Commercial devices tested
- Collaborations with industrial partners
- Some building blocks under test
- Packaging is challenging
- Assess radiation hardness first!

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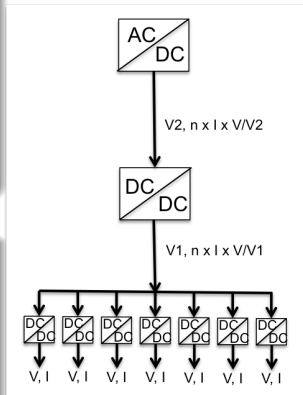
# Common Power Scheme?

## Possible common power structure

- Several stages of converters
  - POL DC-DC and/or Linear VR at the load
- Specifications needed
  - Environmental conditions (radiation)
  - Input/Output voltages and power
  - Common devices possible

## Tracker powering

- DC-DC converters
  - Radiation and magnetic tolerant
- Serial powering scheme
  - Successfully tested on an ATLAS stave
  - Only viable solution for the pixel detectors?



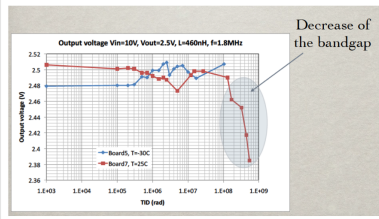
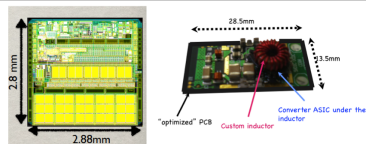
# Radiation and Magnetic Field Tolerant POL DC-DC

## Specific development for the trackers

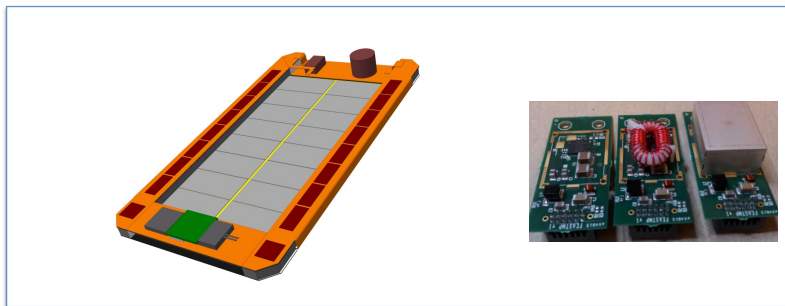
- Started in 2008, now in production
  - ASIC (.35  $\mu\text{m}$ ) and complete module
  - 5 – 12 V  $V_{\text{in}}$ , 0.9 – 5 V  $V_{\text{out}}$ , 4 A
  - $>2 \text{ MGy}$  and  $8 \cdot 10^{14} \text{ 1MeV.n.cm}^{-2}$
- Some limitations for inner layers of trackers @ HL-LHC

## Further developments

- New ASIC needed for higher radiation hardness



## DC-DC for the CMS 2S Module



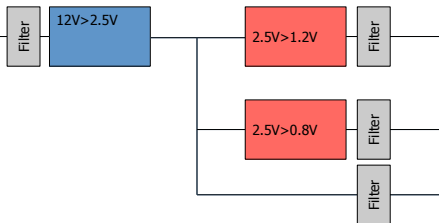
2S module requires 4 W with 2.5 V, 1.2 V, 0.8 V

- FEASTMP example delivers one voltage output only
- Need to fit more power devices (DCDCs or Switched Cap)
- New devices or developments are required

# DC-DC for the CMS 2S Module cont'

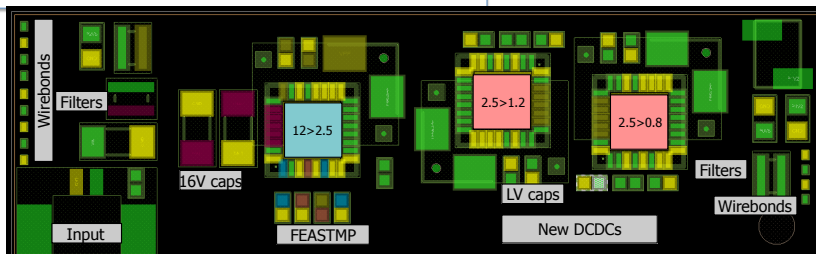
DCDC 12V/2.5V 2A  
FEASTMP

DCDC 2.5V/1.2V and 0.8V 2.3A max  
New development

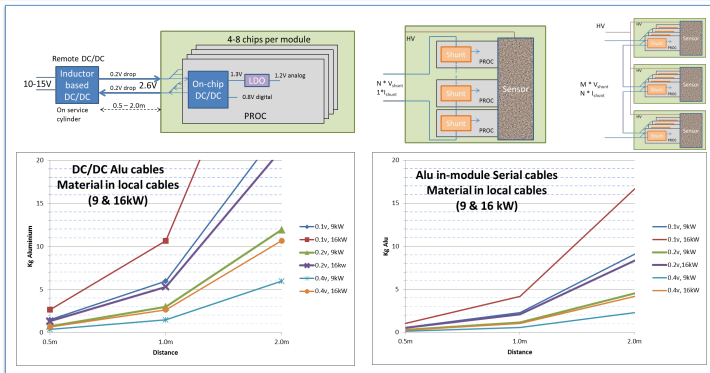


## 2 new DC-DC converters

- Lower inductances
- Lower capacitances
- Smaller foot-print



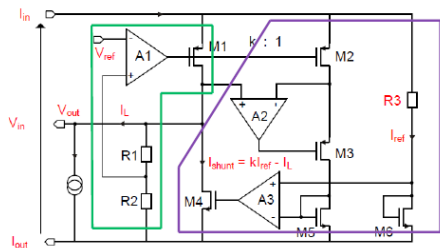
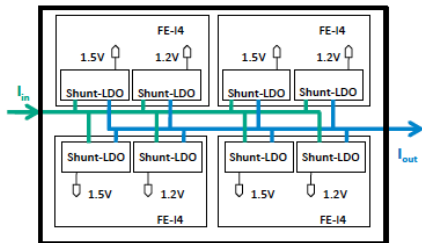
# DC-DC versus Serial Power for Pixel



## Case study for the CMS pixel

- Cable mass is critical
- As well as power dissipation in the cables

## ATLAS Shunt-LDO regulator for Pixel



## Requirements

- Parallel operation with different  $V_{out}$
- Ability to shunt extra current

## Shunt-LDO

- $V_{out} = 2V_{ref}$
- $I_{ref} \approx V_{in} - V_{th} / R_3$
- $R_{in} \approx R_3 / k$



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- 4 Summary
  - A bit of History

# Where were we 11 Years before LHC Start?

## Date of LHC start

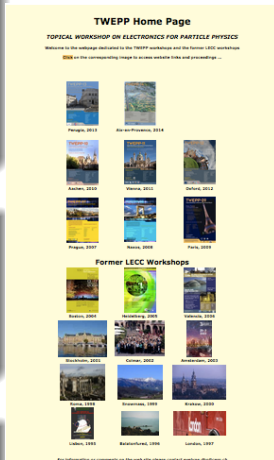
- Moving target however two dates emerge
  - Fall 2006 and Fall 2008
- Information from LERB, LECC Workshops
  - Lisbon 1995 or London 1997

## We were far away from the final systems

- 0.25  $\mu m$  CMOS one poster in 1997
- Optical links using modulators or LEDs
- Massive usage of FPGA barely emerging

## We should keep our eyes opened

- We might be lucky again...



# Summary

- HL-LHC imposes strong constraints on the readout electronics
  - High radiation levels
  - Large amount of data to be handled
- A lot of developments are on-going
  - ASIC developments
  - Trigger architecture
- Common developments on specific topics
  - Pixel electronics
  - "Common projects" (links, DC-DC converters)
- Still space for more common developments
  - IP blocks
  - Common power blocks
- 11 years to go before HL-LHC starts
  - We should keep our eyes opened...

# Sources and Acknowledgements

## Sources

ACES 2014: <http://indico.cern.ch/e/ACES2014>

ECFA workshops on HL-LHC: <https://indico.cern.ch/event/252045/>  
& <https://indico.cern.ch/event/315626/>

ATLAS and CMS Lol, TP, etc.

TWEPP: <http://twepp-workshops.web.cern.ch/TWEPP-Workshops/>

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