

Ecole Microélectronique 2015  
Fréjus – Villa Clythia  
17 mai -22 mai 2015



## Thèmes de cette Ecole 2015 :

- Le futur de la microélectronique :
  - Up-grade LHC,
  - Process 65 nm,
  - Etude de blocs en 65 nm,
  - La microélectronique à l'IN2P3/IRFU (table ronde)
- La micro-cryo-électronique
- Les ADC SAR
- Le High Speed
- Les cellules numériques
- Les outils

Ecole de Microélectronique IN2P3 2015 - 17 mai au 22 mai - Fréjus

<b>Dimanche 17 mai : arrivée des participants</b>		
20h : Dîner		

<b>Lundi 18 mai</b>	08:15	Présentation de l'école	Gisèle Martin-Chassard (OMEGA) Hervé Mathez (IPNL)
	08:30 10:00	Evolution de la microélectronique	Alessandro Marchioro (CERN)
		<b>Café</b>	
	10:30 12:00	Upgrade HL-LHC	Philippe Farthouat (CERN)
	12:15	<b>Déjeuner</b>	
	16:00 17:30	Revue de la technologie 65nm et des blocs développés	Valerio Re (INFN)
		<b>Café</b>	
	18:00	Retour d'expérience en technologie 65 nm dans le cadre de ATLAS/LHC	Moshine Menoumi (CPPM)
	18:30	<b>Posters Building blocks</b>	
	19:30	Remarques : Les posters doivent être techniques et présenter un bloc d'un	Tous
	20:00	<b>Dîner</b>	

<b>Mardi 19 mai</b>	08:30 10:00	Etude de cellules analogiques en technologie fines	Jacques Lecoq (LPC Clerm)
		<b>Café</b>	
	10:30 11:15	Etude de cellules analogiques en technologie fines (suite) Discussion	Jacques Lecoq (LPC Clerm)
	11:30 12:00	Front-end at cryogenic temperature	Edouard Bechetoille (IPNL)
	12:15	<b>Déjeuner</b>	
	16:00 17:30	La microélectronique à l'IN2P3/IRFU	Claude Colledani (IPHC)
		<b>Café</b>	
	18:00 19:30	Table ronde : Evolution de l'électronique à l'IN2P3	Catherine Clerc (IN2P3)
	20:00	<b>Dîner</b>	

<b>Mercredi 20 mai</b>	08:30 10:00	SAR ADC design and calibration techniques	Pr Yun Chiu (Univ.Dallas-Texas)
		<b>Café</b>	
	10:30 12:00	SAR ADC design and calibration techniques	Pr Yun Chiu (Univ.Dallas-Texas)
	12:15	<b>Déjeuner</b>	
	16:00 17:30	SAR ADC design and calibration techniques	Pr Yun Chiu (Univ.Dallas-Texas)
		<b>Café</b>	
	18:00 19:30	Méthodologie de caractérisation des cellules numériques	Xavier Llopert (CERN)
	20:00	<b>Dîner</b>	

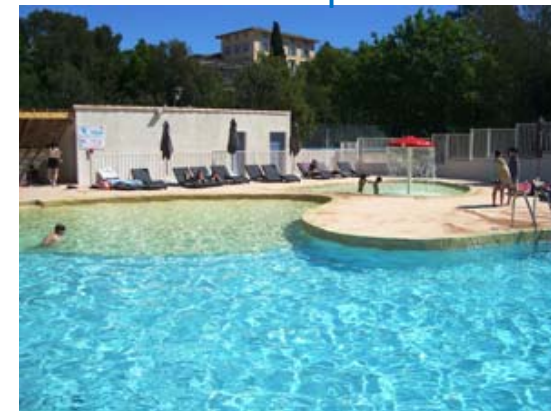
<b>Jeudi 21 mai</b>	08:30 10:00	Aspects on high speed and radiation tolerance I/O	Roberto Beccherle (CERN)
		<b>Café</b>	
	10:30 12:00	Aspects on high speed and radiation tolerance I/O	Roberto Beccherle (CERN)
	12:15	<b>Déjeuner</b>	
	16:00 17:30	Front-end & Multiplexage at cryogenic temperature	Damien Prêle (APC)
		<b>Café</b>	
	18:00 19:30	Outils CAO : PVS Voltus Tempus	Frédéric Morel (IPHC)
	19:30 20:00	Bilan de la formation	Tous
	20:00	<b>Dîner</b>	

<b>Vendredi 22 mai : Départ des participants</b>		
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## Pour les interventions



## Pour les pauses



← COFIL du réseau Microélectronique

← Remplir le questionnaire de fin d'école

Session Posters  
Fréjus – Villa Clythia  
17 mai -22 mai 2015



# LPSC Grenoble

1) Very High speed redundant SAR ADC,  
designed for ATLAS

2) High resolution column ADC for CMOS Image  
sensors

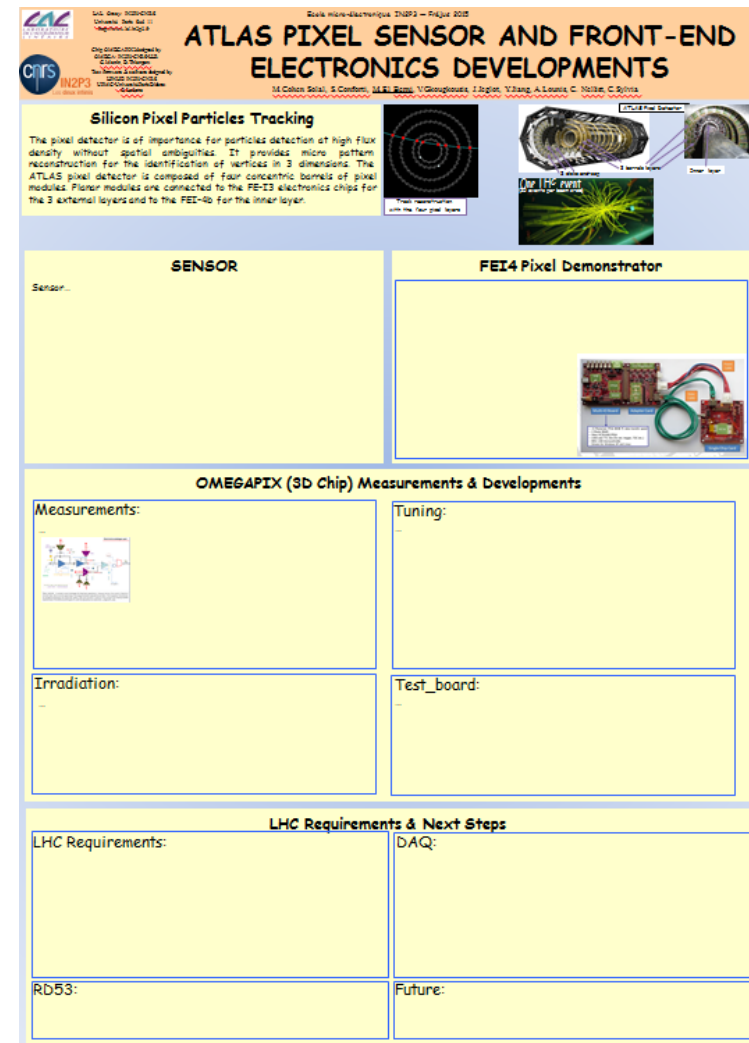
Daniel Dzahini, Fatah Rarbi, Mohamed Zeloufi

# ATLAS PIXEL SENSOR AND FRONT-END ELECTRONICS DEVELOPMENTS

## LAL ATLAS Pixel

M. Cohen Solal, S. Conforti, M. El Berni,  
V.Gkougkousis, J.Jeglot, Y.Jiang, A.Lounis,  
C. Nellist, C.Sylvia

- Chip Omegapix2 designed by OMEGA (G.Martin-Chassard, D.Thienpont)
- Test Firmware and Software designed by LPNHE (O. Le Dortz)



**ATLAS PIXEL SENSOR AND FRONT-END ELECTRONICS DEVELOPMENTS**

**Silicon Pixel Particles Tracking**

The pixel detector is of importance for particles detection at high flux density without spatial ambiguities. It provides micro pattern reconstruction for the identification of vertices in 3 dimensions. The ATLAS pixel detector is composed of four concentric barrels of pixel modules. Planar modules are connected to the FE-13 electronics chips for the 3 external layers and to the FEI-4b for the inner layer.

**SENSOR**

Sensor...

**FEI4 Pixel Demonstrator**

FEI4 Pixel Demonstrator

**OMEGAPIX (3D Chip) Measurements & Developments**

**Measurements:**

**Tuning:**

**Irradiation:**

**Test\_board:**

**LHC Requirements & Next Steps**

**LHC Requirements:**

**DAQ:**

**RD53:**

**Future:**



Design de mémoires de configuration tolérantes au  
Single Event Upset pour le futur circuit de lecture des  
pixels de ATLAS  
Techno : TSMC 65nm

Denis Fougeron, Mohsine Menouni, Patrick Pangaud, Anging Wang





weeroc

Building blocks en technologie X-FAB SOI 180nm

Jean-Baptiste Cizel : Weeroc/LLR



SPACIROC : chip spatial de lecture MAPMT

Sylvie Blin, Damien Thienpont

*CITIROC : chip de lecture de SIPM*

*Stephane Callier, Ludovic Raux*

techno : AMS SiGe 350nm





"Intégration « rad-hard » d'un protocole I2C en BiCMOS 0,35 $\mu$ m AMS".

*C. Beillimaz, D. Prêle et F. Voisin*



# SamPic: le premier WTDC intégré pour la mesure à la pico-seconde.

(Olivier Gevin)

Développement d'un système multi-canal pour la mesure du temps à la pico-seconde en utilisant la technique (brevetée) du WTDC intégrée dans la puce SAMPIC en technologie **AMS 0,18µm**.


Le principe consiste à intégrer trois niveaux de précision de la mesure du temps:

- Un compteur.
- Une DLL.
- Une analyse de la forme de l'impulsion (WTDC).

Le chip intègre, dans chaque canal une **DLL** de 64 cellules, et chaque cellule est codée par un ADC 11 bits.

⇒ **1024 ADC dans le chip.**


Un système de test pour 32 canaux a été développé et les tests font état d'une **résolution en temps de 5ps**.



Physique des 2 Infinis et des Origines

**SamPic: the first integrated WTDC with ps-range precision**

E. Delagnes, H. Grabas, M. Sainpert – CEA/Irfu (Saclay)  
D. Breton, O. Lemaire, J. Maalmi, P. Rusquart, P. Valterrand – CNRS/IN2P3/LAL (Orsay)



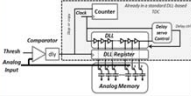
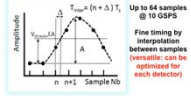
**Goal & Principle:**

Development of a multi-channel scalable acquisition system (ASICs, boards, software) for ps accuracy time picking using the new WTDC (Waveform-based Time to Digital Converter) patented concept integrated in the new SAMPIC ASIC:

- ✓ The analog signal delivered by the detector is sent to both:
  - a discriminator with programmable threshold,
  - an analogue memory driven by a Delay Line Loop which total delay is servo-controlled to the clock period of a timestamp counter.
- ✓ The discriminator output :
  - catches the state of the counter output ⇒ coarse timestamp (6.4ns step)
  - catches the state of the DLL ⇒ medium precision (100 ps precision) timing,
  - stops the waveform sampling ⇒ few ps precision

**Targets: all fast timing detectors**

All the new fast (photo)detectors: MCP-PMT, diamonds, APD, SiPM ..., TOF detectors, particle Identification, pile-up rejection (ATLAS AFP...), TOF-PET scanners.

Up to 64 samples @ 10 GSPS


Fine timing by interpolation between samples (variable: can be optimized for each detector)

**The SamPic0 ASIC**

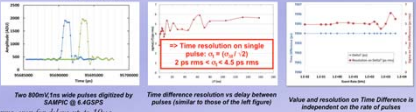
- ✓ 16 independent, self-triggerable channels
- ✓ 1 discriminator, 1 timestamp/channel
- ✓ 64-cell analog memory/channel
- ✓ 3 to 10 Cells/Samples Per Second sampling
- ✓ 11 bits, 1.5 GHz, Wilkinson-ADC full
- ✓ Integrated smart readout (400 MHz)
- ✓ Parameter settings (threshold, ...) by SPI
- ✓ 1.5 µs or less dead time/ event
- ✓ Several trigger modes available

**The SamPic acquisition system**

- ✓ Mother board housing 2 mezzanines
- ✓ SAMPIC mezzanines: 16 channels
- ✓ 32-channel system available today
- ✓ Portable data acquisition software
- ✓ Windows & Linux libraries
- ✓ GUI interface for measurements, calibration & data display,
- ✓ Includes timing extraction algorithms
- ✓ 5 modules manufactured
- ✓ 2 used in test beam @CERN



**Test Results**



✓ The chip fulfills the initial requirements :
 

- > 1.5 GHz analog bandwidth
- 3-10 GSps sampling
- Low power: < 15mW/channel
- ~10 bit RMS dynamic range / 1V
- < 2µs dead time / event
- ...

✓ Timing measurements in self-triggered mode prove resolution on time difference between pulses < 10 ps rms, even for delays up to 10µs

Time difference resolution vs delay between pulses (similar to those of the left figure)

Value and resolution on Time Difference is independent on the rate of pulses

**As of today, the SAMPIC0 prototype is the only multichannel, unlimited dynamic range, integrated timing system available worldwide !!!**

**Ongoing and futureWork**

- ✓ Improvement of the software
- ✓ Test beam with the present chip
- ✓ Software for ETH/UDP
- ✓ Submission of the 2nd chip prototype with
  - Few more corrections
  - Enhanced functionalities (triggering, ...)
  - Reduced deadtime
- ✓ Design of a 64/128-channel board for scalable D/LQ
- ✓ Study of a chip version optimized for TOF-PET.

Contacts : [eric.delagnes@cea.fr](mailto:eric.delagnes@cea.fr)  
[breton@lal.in2p3.fr](mailto:breton@lal.in2p3.fr)

P2IO Scientific Council  
17-18/12/2014



# ADC 13-bit 32 voies pour applications spatiales

CEA, IRFU F-91191 Gif sur Yvette Cedex,

Florent Bouyjou

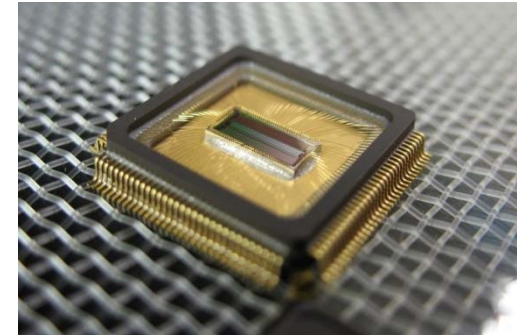
Présentation d'un ADC 32 voies, 13-bit, 2,56  $\mu\text{s}$  de temps de conversion, 2V de plage d'entrée appelé OWB-1. L'architecture est basée sur une architecture de type Wilkinson à base de DLL. La technologie utilisée est la CMOS 0,35  $\mu\text{m}$  d'AMS.

## Performances mesurées :

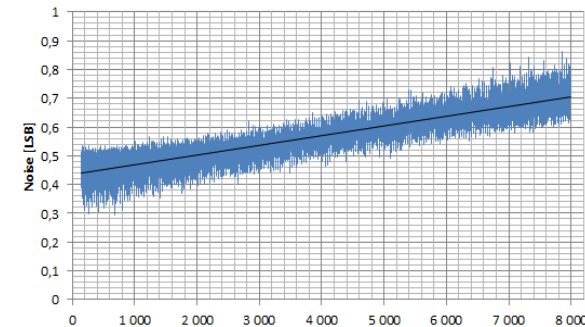
Nb voies	32 //
Bits	13 bit
Plage d'entrée	2 V
Temps de conversion	2,56 $\mu\text{s}$ (2,7 $\mu\text{s}$ de temps d'échantillonnage)
LSB	244 $\mu\text{V}$ (DLL : 312,5 ps)
Bruit RMS	[0,29 à 0,87 LSB] : 71 à 212 $\mu\text{V rms}$
NLD	+0,31 à -0,28 LSB
NLI	+2,1 à -1,3 LSB
Puissance/canal	0,8 mW en statique et dynamique par voie TOTAL : 57mW
Fréquence d'horloge	1 MHz LVDS en entrée d'ASIC 100 MHz en sortie de PLL 3,2 GHz pour la DLL
Température	-40 à 40 °C
Layout	50 * 2000 $\mu\text{m}$ par voie : TOTAL 18 mm <sup>2</sup>

Un système d'autocompensation en température est aussi intégré et permet de compenser les effets de la température entre -40°C et +40°C.

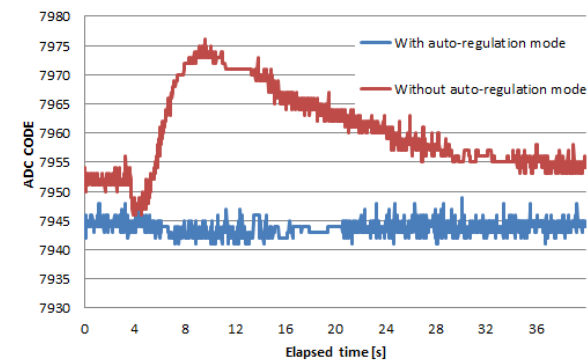
Des techniques de dessin du layout sont utilisées afin d'augmenter la tolérance de l'ASIC aux Single Event Latchup (SEL)



## Mesure du bruit :




## Autorégulation en température :



# IPHC:CMOS Digital Pixels

## Design Study for Low-Noise and Power Efficiency

- Presented by WANG Tianyang,
  - PhD student
- Context: ALICE ITS upgrade
- Building Block: Digital pixel
  - Allow for low power and high speed
  - Main Constraint
    - Small area ( $22 \times 33 \mu\text{m}^2$ ) & Low Noise
- Two AROM-1 prototypes presented
  - AROM-1 B
    - Static current:  $\sim 33 \mu\text{A}/\text{pixel}$
    - In-pixel discriminator noise:  $\sim 0.98 \text{ mV}$
    - ENC:  $\sim 25 \text{ e}^-$
  - AROM-1 E
    - Static current:  $\sim 18 \mu\text{A}/\text{pixel}$
    - In-pixel discriminator noise :  $\sim 0.35 \text{ mV}$
    - Promising in-pixel discriminator design



### CMOS Digital Pixels

#### Design Study for Low-Noise and Power Efficiency

T. Wang, H. Pham, A. Dorokhov, M. Goffe, I. Valin, A. Himmi, F. Morel, C. Hu-Guo, Y. Hu  
IPHC (Institut Pluridisciplinaire Hubert Curien), Strasbourg

#### Introduction

- Full CMOS capability inside the pixel can be achieved for CMOS pixel sensors (CPS) fabricated in a  $0.18 \mu\text{m}$  quadruple well CMOS process. The additional deep P-wells prevent the N-wells hosting the PMOS transistors from collecting signal charge (see Fig. 1).
- Various prototypes of CPS, featuring the in-pixel signal discrimination, were designed and fabricated in this  $0.18 \mu\text{m}$  CMOS process [1, 2].
- Each pixel consists of a sensing diode, a pre-amplifier and a discriminator. The pixel pitch is chosen to be  $22 \times 33 \mu\text{m}^2$ , and a spatial resolution  $\sim 5 \mu\text{m}$  is expected.
- As compared to the column-level signal discrimination, formally used in the CMOS pixel sensors, the in-pixel discrimination offers the opportunity for fast and power efficient operation.
- These new CMOS pixel sensors were developed within the framework of the ALICE-ITS upgrade.
- This work presents some of the most recent achievements.

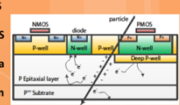


Fig. 1 Cross section view of a CMOS pixel sensor in a quadruple-well process

#### Column-level discrimination vs. in-pixel discrimination

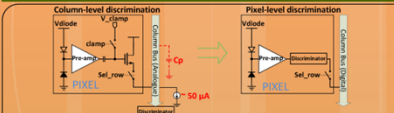


Fig. 2 Illustration of column-level discrimination and in-pixel discrimination

The in-pixel discrimination removes the power consuming source follower, which is required in the column-level discrimination to drive the large parasitic capacitance ( $C_p$ ) on the column line

- In-pixel discrimination has the potential for fast and power efficient operation
- Performance of a small area discriminator in a dense pixel needs to be verified

#### AROM-1 prototypes

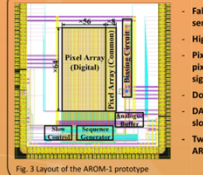


Fig. 3 Layout of the AROM-1 prototype

- Fabricated in the TowerJazz  $0.18 \mu\text{m}$  CMOS image sensor process, featuring the quadruple wells
- High-resistivity epitaxial layer ( $> 1 \text{ k}\Omega \cdot \text{cm}$ )
- Pixel array of  $64 \times 64$ , including 8 columns of modified pixels which are capable of providing the analogue signal
- Double-row rolling shutter readout
- DACs (reference & biasing), sequence generator, slow control via JTAG registers ....
- Two chip versions are presented in this work, i.e. AROM-1 B and AROM-1 E

#### 2 PIXEL DESIGNS

#### AROM-1 B

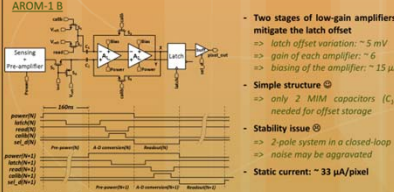


Fig. 4 Pixel schematic and timing sequence of AROM-1 B

- Two stages of low-gain amplifiers to mitigate the latch offset
  - latch offset variation:  $\sim 5 \text{ mV}$
  - gain of each amplifier:  $\sim 6$
  - biasing of the amplifier:  $\sim 15 \mu\text{A}$
- Simple structure
  - only 2 MIM capacitors ( $C_p, C_s$ ) needed for offset storage
- Stability issue
  - 2-pole system in a closed-loop
  - noise may be aggravated
- Static current:  $\sim 33 \mu\text{A}/\text{pixel}$

#### AROM-1 E

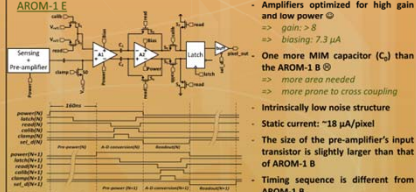


Fig. 5 Pixel schematic and timing sequence of AROM-1 E

- Amplifiers optimized for high gain and low power
  - gain:  $> 8$
  - biasing:  $7.3 \mu\text{A}$
- One more MIM capacitor ( $C_s$ ) than the AROM-1 B
  - more area needed
  - more prone to cross coupling
- Intrinsically low noise structure
- Static current:  $\sim 18 \mu\text{A}/\text{pixel}$
- The size of the pre-amplifier's input transistor is slightly larger than that of AROM-1 B
- Timing sequence is different from AROM-1 B

#### Measurement results

#### Measurements with a $^{55}\text{Fe}$ X-ray source

Measurements were performed on the 8 columns of modified pixels. The calibration peak corresponds to the full collection of  $1640 \text{ e}^-$  generated by a  $5.9 \text{ keV}$  photon, in case the interaction point is close to the sensing diode.

Fig. 6 Analog response to a  $^{55}\text{Fe}$  X-ray source for AROM-1 B

AROM-1 B (measured spectra presented in Fig. 6)

- charge-to-voltage factor (CVF):  $\sim 50 \mu\text{V/e}^-$
- charge collection efficiency (CCE):  $40\%$  for the seed pixel

AROM-1 E

- low CVF ( $\sim 30 \mu\text{V/e}^-$ ) not consistent with experience obtained from previous prototypes (expected to be  $\sim 50 \mu\text{V/e}^-$ )
- design issue at the pixel-level is excluded, since a similar pixel structure implemented in a former prototype has a reasonable CVF [1]
- the "CVF" buffer driving capability is most suspect.

#### Discriminator characterization

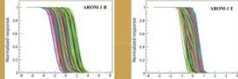


Fig. 7 "S" curves of the in-pixel discriminators

- Each "S" curve was plotted by calculating the probability of "1" at the output of a discriminator, as a function of threshold voltage.
- slope indicates temporal noise (TN)
- width indicates fixed pattern noise (FPN)

Results in Fig. 7 were measured at  $160 \text{ ns}/\text{rows}$

	TN	FPN	Total noise
AROM-1 B	0.75 mV	0.63 mV	0.98 mV
AROM-1 E	0.29 mV	0.19 mV	0.35 mV

#### Full in-pixel circuitry characterization

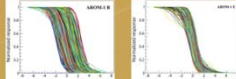


Fig. 8 "S" curves of the full in-pixel circuitry

- Results measured at  $160 \text{ ns}/\text{rows}$
- Equivalent charge noise (ENC) is  $\sim 25 \text{ e}^-$  for AROM-1 B
- Despite lower noise voltage, ENC of AROM-1 E is not a good indicator for the pixel noise performance due to the low CVF
- BUT, it contains a very promising in-pixel discriminator design

	TN	FPN	Total noise	ENC
AROM-1 B	1.1 mV	0.66 mV	1.28 mV	$\sim 25 \text{ e}^-$
AROM-1 E	0.94 mV	0.23 mV	0.97 mV	

#### Conclusion

- Promising noise performance can be achieved with small-area in-pixel discriminators (e.g. pixel area of  $22 \times 33 \mu\text{m}^2$ ).
- ENC of  $\sim 25 \text{ e}^-$  has been achieved by AROM-1 B. And it can be further improved by optimizing the sensing system (diode + pre-amplifier) for a larger CVF.
- AROM-1E represents a very promising in-pixel discriminator design with very low power consumption (static  $I \sim 15 \mu\text{A}$ ) and noise ( $\sim 0.35 \text{ mV}$ ). And we are confident to reproduce a similar CVF as AROM-1 B for AROM-1 E in the future.

#### REFERENCES

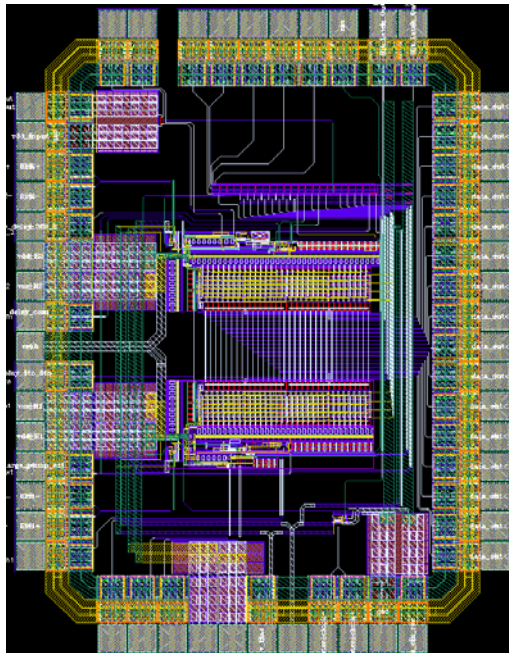
- T. Wang et al., Development of CMOS Pixel Sensor Featuring Pixel-Level Discrimination for the ALICE-ITS Upgrade, Proceedings of science, 2014
- T. Wang et al., Development of CMOS Pixel Sensors with digital pixel dedicated to future particle physics experiments, TWEPP 2013

[tianyang.wang@iphc.cnrs.fr](mailto:tianyang.wang@iphc.cnrs.fr)





## Poster: Interpolateur de temps à haute résolution (50ps)



Dans le cadre d'une R&D sur le codage en temps, le LPC Caen a développé un interpolateur de temps haute résolution comportant 2 voies. Ce interpolateur est basé sur une boucle à verrouillage de retard (DLL) et une ligne à retard contrôlée par un deuxième DLL verrouillé sur la première.

Cette architecture a été optimisée dans le but d'éviter la mise en œuvre d'un système d'étalonnage compliqué.

Ce bloc de base a été conçu pour fournir une mesure de l'intervalle de temps entre le signal d'horloge ( $F_{in}=160\text{MHz}$ ) et le signal de « hit » entrant sur la voie.

La taille minimum de cet intervalle de temps correspond de la période d'horloge divisée par 128 (environ 50 ps) et la résolution de temps est d'environ 40 ps RMS.

Le signal d'horloge est commun aux deux voies et une mesure différentielle (temps de vol) peut être faite avec une résolution de temps d'environ 60 ps RMS.

Les données temporelles sont disponibles par l'intermédiaire d'un bus de données 16 bits.

Contact : Laurent LETERRIER

Email: [leterrier@lpccaen.in2p3.fr](mailto:leterrier@lpccaen.in2p3.fr)



# "Buildings blocks for FATALIC Asic" ATLAS upgrade

Contact :  
L.Royer  
MICRHAU-L@in2p3.fr



Building Blocks pour FATALIC

Démarré en 2010 en tant que R&D s'appuyant sur la technologie IBM 130nm recommandée par le CERN, le projet FATALIC a pour objectif de proposer une électronique de lecture intégrée pour la mise à jour du calorimètre hadronique TileCal de l'expérience ATLAS. FATALIC sera utilisé sur le démonstrateur lors des tests en faisceau à l'automne.

**Circuit FATALIC: upgrade de l'électronique de lecture du TileCal d'ATLAS**

**Convoyeur de courant MOS**  
Lecture du courant du PMT  
Large gamme dynamique (12nC à 1200pC)  
Gamme dynamique divisée en 3 (sortie courant)

**Shaper:**  
- Amplif. Transimpédance  
- Intégrateur

**FATALIC:**  
Techno: IBM CMOS 130nm  
Surface (core): 2.3mm<sup>2</sup>  
Conso: 205mW@1.6V

**Bloc numérique:**  
- Sélection automatique des données de sortie (2 voies sur les 3)  
- Multiplexage 12-bit @ 80 MHz

**3 ADC 12-bits @ 40MS/s**  
Architecture pipeline 1.5bit/étape

**Convoyeur de courant**

Simu IR Drop à 50mA de courant d'entrée: ΔV=200mV !!  
Non Linéarité Simu-mesures

Structure différentielle  
Étage d'entrée Grille-Commune (non boosté)  
I bias: 1.5mA - Courant d'entrée pic jusqu'à 75mA  
Recopie de courant pour les 3 gammes

**Convertisseur Analogique-Numérique**

Archit. Pipeline 1.5 bit /étape  
Simu IR Drop alim des 4 ADC: ΔV< 10mV

Consommation totale ADC (non optimisée): 30mA@1.6V  
INL = ± 2LSB (mesures complémentaires à voies)

Comparateur différentiel

OTA différentiel

Structure différentielle  
- GBW: 485MHz - Conso: 1.7mA@1.6V  
- Marge Phase: 83° - SR: 220V/μs  
- Gain BO: 84 dB (16k)

**Bruit en sortie (ADC counts)**

Haut Gain Moyen Gain  
ENC < 10FC

Linéarité Haut Gain

Signaux après shaping

Synoptique bloc numérique

Layout FATALIC

Structure totalement différentielle  
- Isolation substrate (étage entrée (SPM/DMAT)  
- Allen, séparateurs, découplages, low IR drop  
- Blocs de test (swing, core & ADC)

**Ecole de microélectronique de l'IN2P3**  
Contact : MICRHAU-L@in2p3.fr